# High Performance Narrow-Band Transceiver IC

## Silicon Anomaly Sheet

# ADF7021-N

This anomaly sheet describes the known bugs, anomalies, and workarounds for the ADF7021-N narrow-band transceiver. This relates to Silicon Revision 1, which has a corresponding silicon revision readback code of 0x2111. See the ADF7021-N data sheet for details on how to perform a silicon revision readback.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

### ADF7021-N SILICON REVISION HISTORY

| Silicon Revision Readback | Chip Marking | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|---|---|---|---|---|
| 0x2111 | ADF7021-NBCPZ | Release | Rev. 0 | 1 |

**Rev. 0**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

## ANOMALIES

### 1. Performing Readback During Packet Reception [er001]

| | |
|---|---|
| **Background:** | An internal timing issue can result in bit errors when performing a readback from the ADF7021-N during packet reception. The timing issue is related to the CDR clock and the SCLK. |
| **Issue:** | If the SCLK edge rises in a 5 ns window before the CDR clock edge, then the envelope detector circuit of the ADF7021-N may experience a reset of its threshold. This results in bit errors if the AFC or linear demodulator is being used for demodulation because both these circuits use the envelope detector. If the correlator demodulator is being used without AFC, then this issue is not present. |
| **Workaround:** | There are three possible workarounds; see Table 1. |
| **Related Issues:** | None |

**Table 1. Workarounds for Readback During Packet Reception**

| Workaround | Description |
|---|---|
| 1 | Ensure that a readback is not performed during packet reception. |
| 2 | Ensure that the SCLK edge does not rise in a 5 ns window before the CDR positive clock edge. The CDR clock signal is available via the CLKOUT pin using the CLK_MUX test modes (R15_DB[17:19]). |
| 3 | Use the lock threshold mode (LOCK_THRESHOLD_MODE (R12_DB[4:5])) for packet reception. This locks the threshold of the envelope detector (as well as the AFC and AGC circuits). It can be set to lock on reception of a valid SWD (LOCK_THRESHOLD_MODE = 1 or LOCK_THRESHOLD_MODE = 2) or manually set at any time (LOCK_THRESHOLD_MODE = 3). Once the threshold has locked, a readback can be performed without any bit errors. |

## AD7021-N ANOMALIES STATUS

| Reference Number | Description | Status |
|---|---|---|
| er001 | Performing readback during packet reception | Refer to the workaround described in the Anomalies Section |