ANALOG DEVICES
ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

AN-248
APPLICATION NOTE

ADG201A/202A and ADG221/222 Performance with Reduced Power Supplies

by John Reidy

The ADG201A/202A and ADG221/222 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process and feature 44V supply maximum rating, a signal handling capability that extends to the supply rails, low R_{ON}, low leakage and low power dissipation. The ADG221/222 are latched versions of the ADG201A/202A.

The LC²MOS fabrication process enables these switches to operate over a wide range of supply voltages. They can comfortably operate anywhere in the 10V to 15V single or dual supply range, with only a slight degradation in performance. This application note discusses the variation in switch characteristics over this power supply range and contains graphs showing all the relevant performance curves. All test circuits and test conditions used to generate these curves are contained in the data sheets.

SWITCH ON-RESISTANCE, R_{ON}

The switch R_{ON} is defined by the parallel combination of the P and N channel devices of the output switch (See Figure 1). The gates of these devices are connected to the supply rails. Variations in the supply voltage will vary the gate drive and affect the switch R_{ON}. The R_{ON} sensitivity is about 5Ω/V for single supply and 3Ω/V for dual supply in the 10V to 15V supply range. See Figures 2 to 5.

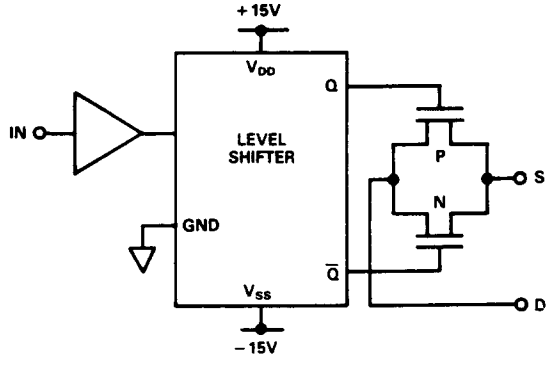

Figure 1. Output Switch Schematic

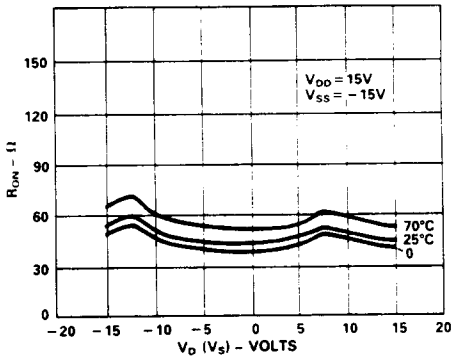

Figure 2. R_{ON} as a Function of V_D (V_S): Dual ± 15 Supplies

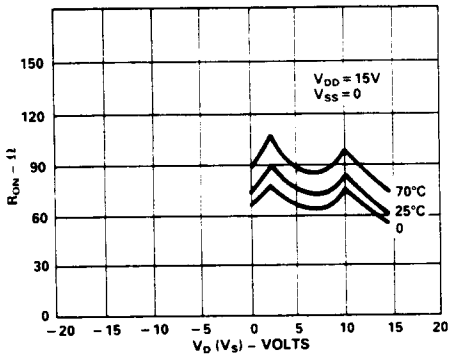

Figure 3. R_{ON} AS A Function of V_D (V_S): Single + 15V Supply

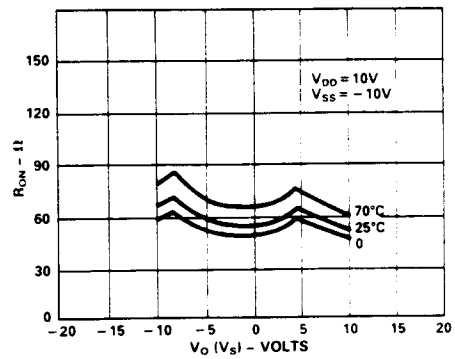

Figure 4. R_{ON} as a Function of V_D (V_S): Dual ± 10V Supplies

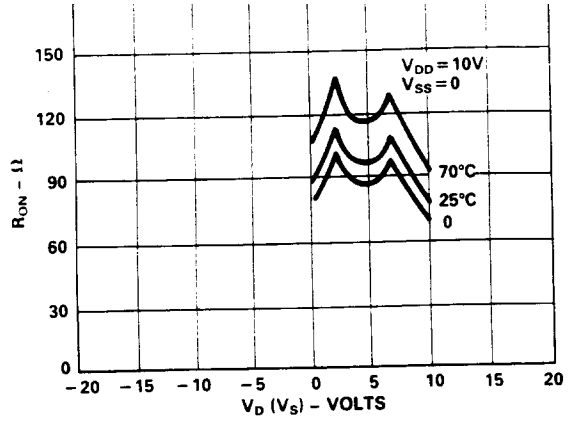

Figure 5. R_{ON} as a Function of V_D (V_S): Single +10V Supply

LEAKAGE CURRENTS I_S(OFF), I_D(OFF), I_D(ON)

I_S(OFF), I_D(OFF) and I_D(ON) are caused by reverse bias diode leakage. Worst case conditions occur at maximum stress voltages, and therefore, leakage currents reduce as the supply voltages reduce. The data sheet specified values at ±15V are 100nA for I_D(OFF) and I_S(OFF) and 200nA for I_D(ON) over the 0 to +70°C temperature range. In reality, these leakage currents are much lower, and are in the 1nA region in the 0 to +70°C temperature range. Since they improve with reduced supply voltages, actual leakage values are very small and difficult to measure precisely. The data sheet specification is a very conservative one and all these leakage currents remain well within this ecification over the 0 to +70°C temperature range with duced supplies.

DIGITAL INPUT TRIGGER LEVELS

Figure 6 shows the digital input schematic. An internal 5V generator provides a reference for all the digital inputs. This generator is immune to any variations in V_{SS}, and exhibits only very minor variations with V_{DD}. Typical changes in the input thresholds is 80mV, for 10V to 15V power supply variation. They remain well within standard TTL levels (<0.8V = Logic Low; >2.4V = Logic High). See Figure 7.

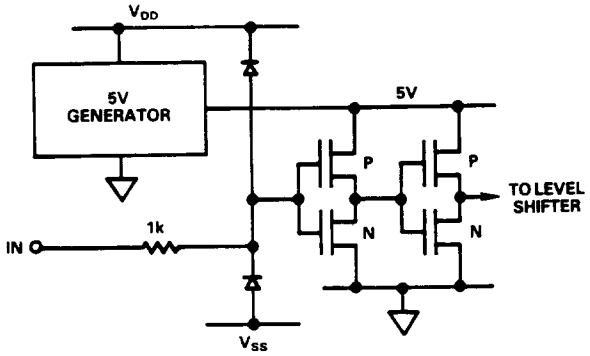

Figure 6. Digital Input Schematic

WITCH TIMING (t_{ON}, t_{OFF}, t_{OPEN})

hese are determined both by the input logic delays and the switch circuitry delays. The input logic timing versus power supply voltage remains fixed because of the internal 5V generator. Any variation in this timing is due only

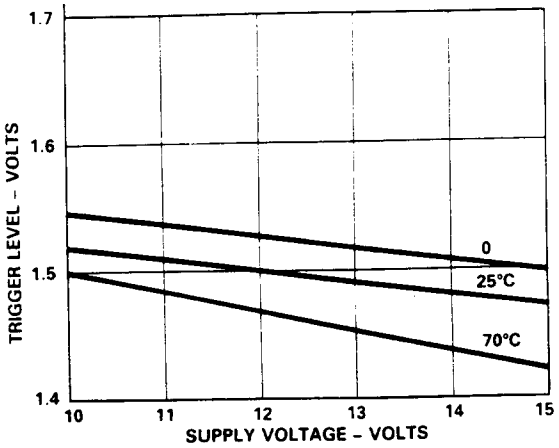

Figure 7. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply Voltage

to the output switch circuitry and is confined to a 40ns change in the 10V to 15V range. See Figures 8 to 11.

LATCH TIMING (t_W, t_S, t_H, ADG221/222 ONLY)

These parameters are determined by the input circuitry only and remain constant over the 10V to 15V power supply variation.

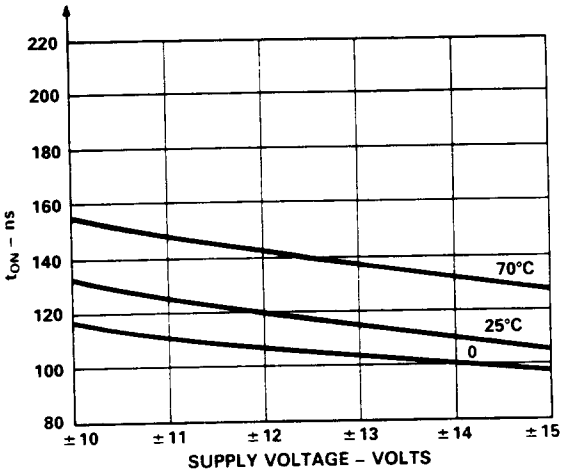

Figure 8. t_{ON} vs. Supply Voltage, (Dual Supply)

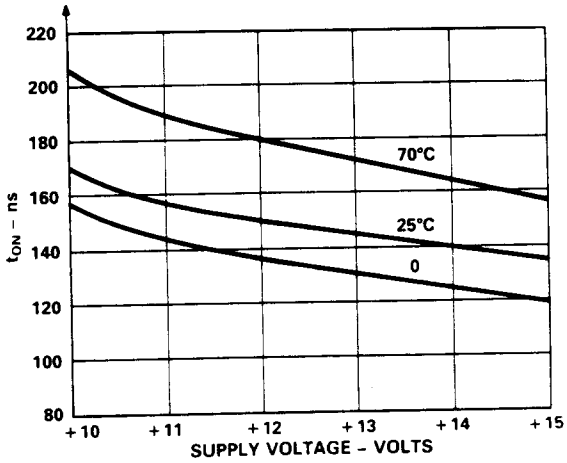

Figure 9. t_{ON} vs. Supply Voltage, (Single Supply)

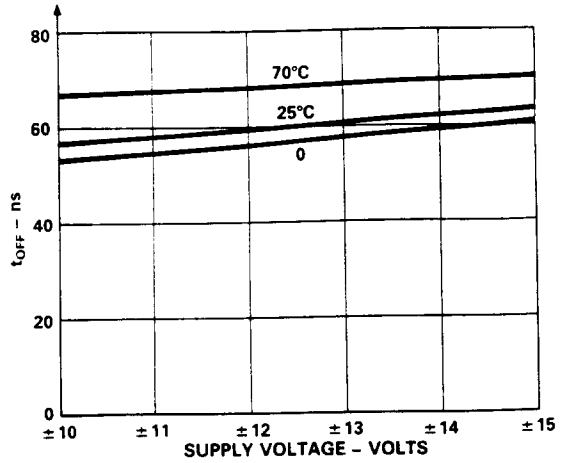

Figure 10. t_{OFF} vs. Supply Voltage, (Dual Supply)

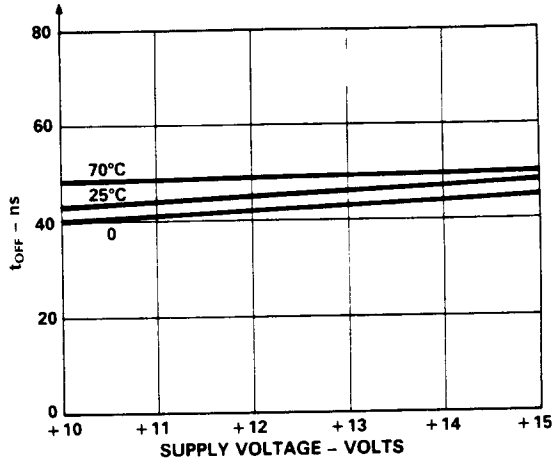

Figure 11. t_{OFF} vs. Supply Voltage, (Single Supply)

DYNAMIC CHARACTERISTICS

Off Isolation and channel-to-channel crosstalk are determined by stray capacitances. Some of these stray capacitances are junction diode capacitances and their values are modulated by the power supply voltage. However, the dominant influence is the package stray capacitance and these are immune to power supply variations. The net effect is that the switch AC performance does not alter with the power supply. See Figure 12.

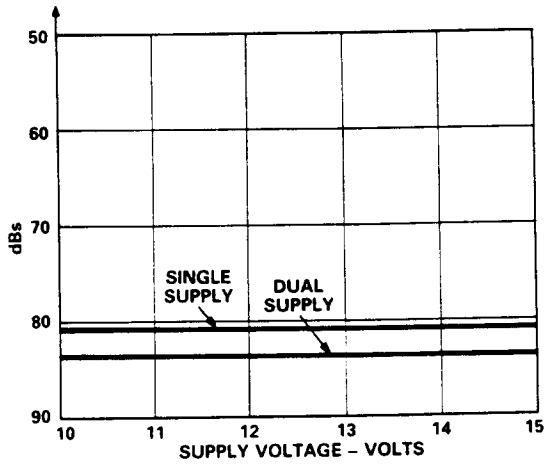

Figure 12. Off Isolation and Channel-to-Channel Crosstalk vs. Supply Voltage

CHARGE INJECTION

Charge Injection is caused by capacitive coupling between the digital control and the source and drain pins. When the digital inputs change, there is a corresponding level shifted change in the gates of the output switches (see Figure 6). This injects charge into the signal line. The amount of charge injected depends on the source voltage (V_S). The data sheet specification is 20 coulombs and is measured for $V_S = 0V$.

Figures 13 and 14 show how charge injection varies with Source Voltage for both 10V and 15V power supplies.

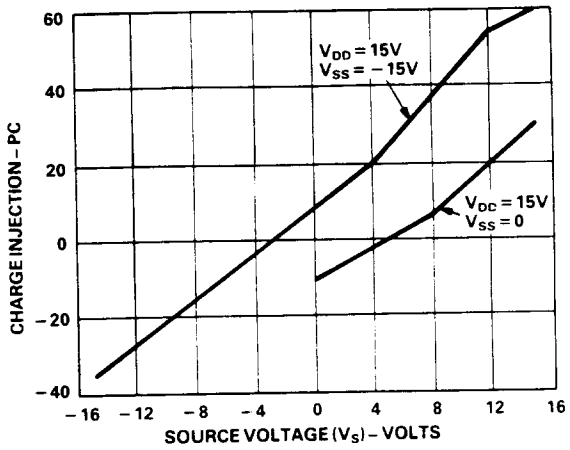

Figure 13. Charge Injection vs. Source Voltage (V_S) for Dual and Single 15V Supplies

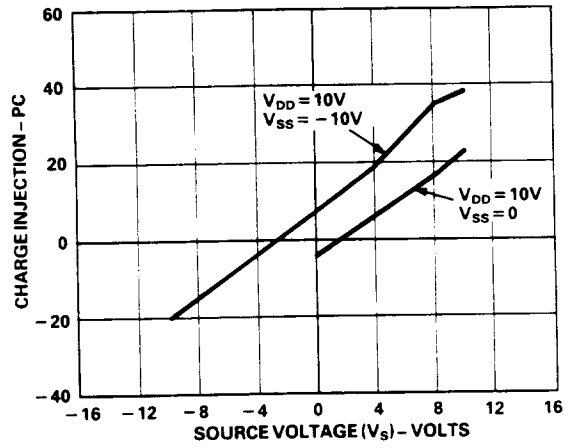

Figure 14. Charge Injection vs. Source Voltage for Dual and Single 10V Supplies

POWER SUPPLY CURRENT

Both I_{DD} and I_{SS} are directly proportional to the supply voltage. The values of these parameters decrease with reduced supply voltages, and thus they remain well within specification for a 15V to 10V power supply range. See Figures 15 to 17.

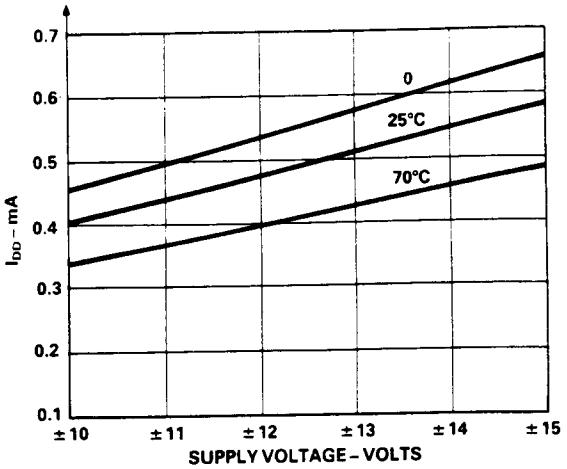

Figure 15. I_{DD} vs. Supply Voltage, (Dual Supply)

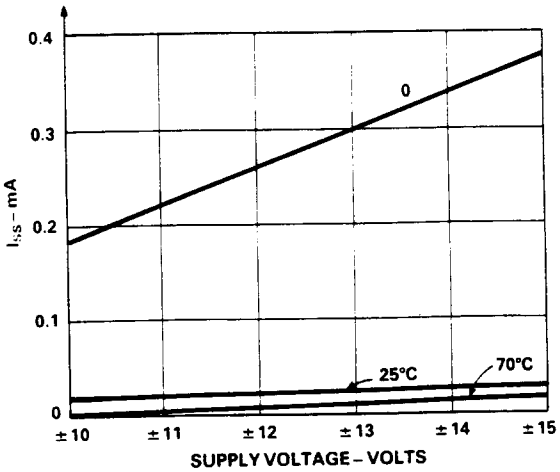

Figure 16. I_{SS} vs. Supply Voltage, (Dual Supply)

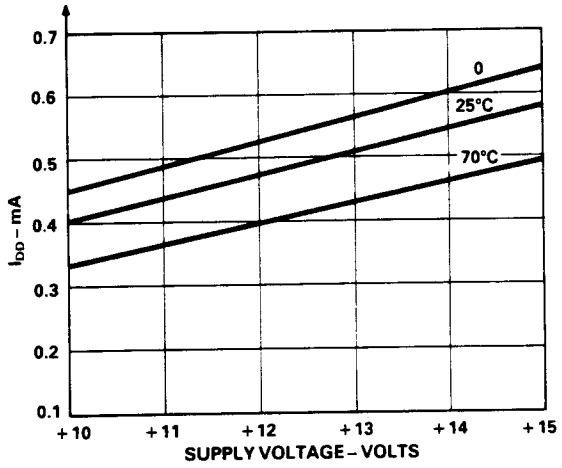

Figure 17. I_{DD} vs. Supply Voltage, (Single Supply)