ANALOG DEVICES

EVAL-ADGM1304SDZ User Guide

UG-1441

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Evaluating the ADGM1304 0 Hz/DC to 14 GHz, Single-Pole, Four-Throw MEMS Switch with Integrated Driver

FEATURES

Single, 3.3 V dc supply voltage
Wide frequency range
SMA connectors for RF signals
SMB connectors for switch control signals
On-board calibration transmission line for analyzer calibration

EVALUATION KIT CONTENTS

EVAL-ADGM1304SDZ evaluation board

DOCUMENTS NEEDED

ADGM1304 data sheet

EQUIPMENT NEEDED

3.3 V dc power supply
PC with Windows® operating system (any version)
EVAL-SDP-CB1Z controller board
USB cable, provided with EVAL-SDP-CB1Z board kit
Vector network analyzer

GENERAL DESCRIPTION

This user guide describes the EVAL-ADGM1304SDZ evaluation board for the ADGM1304, a wideband, single-pole, four-throw (SP4T), microelectromechanical systems (MEMS) switch, and a control chip that are copackaged in a compact, 24-lead, 5 mm × 4 mm × 0.95 mm, lead frame chip scale package (LFCSP). The SP4T switch uses Analog Devices, Inc., MEMS switch technology and provides optimal bandwidth performance, power handling capability, and linearity for radio frequency (RF) applications. The control chip generates the high voltage signals required by the MEMS switch and allows the user to control operation through a flexible, complementary metal-oxide semiconductor (CMOS)-compliant or low voltage transistor to transistor logic (LVTTL)-compliant parallel interface, as well as via a serial peripheral interface (SPI). Multiple ADGM1304 devices can be daisy-chained together to enable the configuration of multiple devices with a minimal amount of digital lines.

For the SPI interface, the evaluation board connects to the universal serial bus (USB) port of a PC via the system demonstration platform (SDP) board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available for order on the Analog Devices website at www.analog.com/SDP-B.

The EVAL-ADGM1304SDZ comes fitted with connectors for RF and control signals, and links to allow the user to control the operation of the switch and evaluate the performance of the ADGM1304.

Consult the ADGM1304 data sheet in conjunction with this user guide when using this evaluation board.

TABLE OF CONTENTS

REVISION HISTORY

1/2020—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

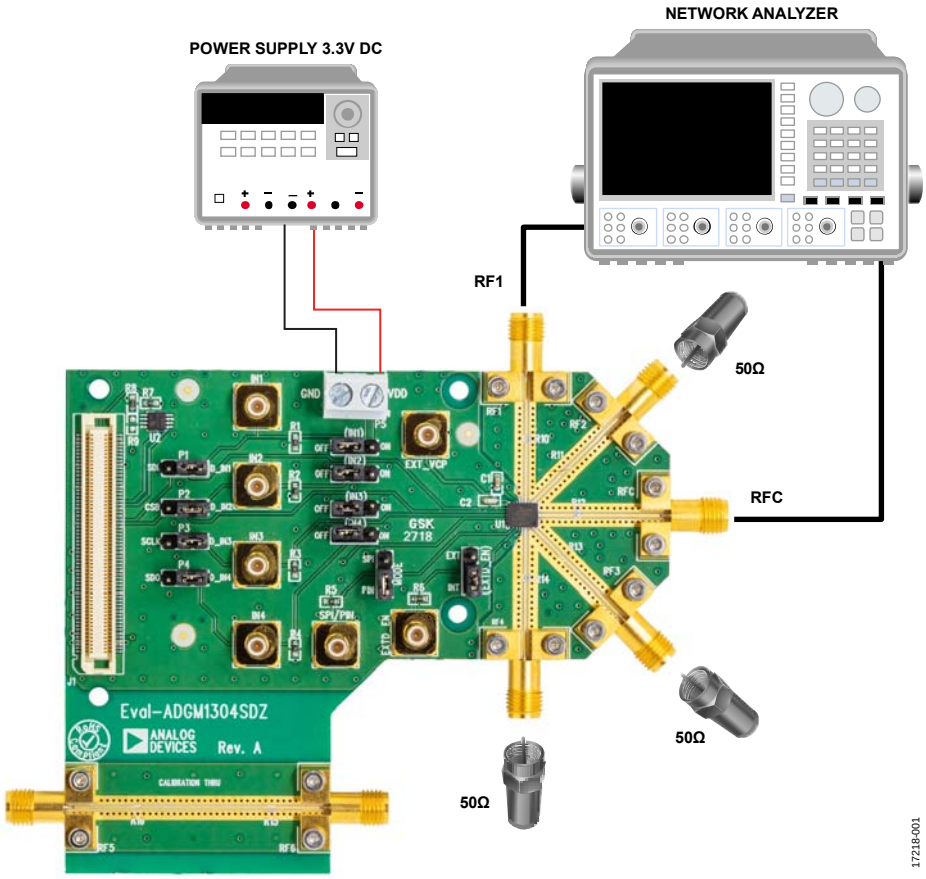

Figure 1. EVAL-ADGM1304SDZ Connection Diagram

EVALUATION BOARD HARDWARE

The ADGM1304 evaluation kit contains a fully fitted, printed circuit board (PCB).

The EVAL-ADGM1304SDZ evaluation board allows the user to connect RF signals to the MEMS switch. The user controls the switch operation using the on-board links or by applying the proper control signals to the appropriate connectors.

The EVAL-ADGM1304SDZ provides an additional transmission line to facilitate the calibration of the network analyzer to minimize the effects of the PCB tracks that connect the RF signals to the MEMS switch. This calibration process is described in the Network Analyzer Calibration Procedure section.

POWER SUPPLY

To operate the EVAL-ADGM1304SDZ, the user must provide an external power supply connected to the power block, P5. The supply voltage is 3.3 V and must be positive with respect to the ground of the PCB. The ground of the PCB is marked as GND on the silkscreen (see Figure 17).

RF CONNECTORS

The SubMiniature Version A (SMA) edge connectors on the EVAL-ADGM1304SDZ (RF1 to RF4 and RFC) connect to each switch in the ADGM1304 for performance evaluation. The RF5 and RF6 connectors connect to a transmission line to estimate the loss associated with the PCB (see the Evaluation Board Software for SPI Interface section). Table 1 describes the RF connectors to the ADGM1304.

Table 1. RF Connectors on the ADGM1304

Connector	Description
RF1	Port RF1 of the ADGM1304
RF2	Port RF2 of the ADGM1304
RF3	Port RF3 of the ADGM1304
RF4	Port RF4 of the ADGM1304
RF5, RF6	CALIBRATION THRU transmission lines used for calibration
RFC	Common RF port of the ADGM1304

SWITCH CONTROL CONNECTORS

The internal control IC, copackaged with the MEMS switch, generates the voltage required to drive the switch. The control IC generates a reference clock signal at 10 MHz. In normal operation, set the EXTD_EN link to the INT position to allow the built in, 10 MHz oscillator to enable the internal driver IC voltage boost circuitry. Setting the EXTD_EN link to the EXT position disables the internal 10 MHz oscillator and driver boost circuitry.

Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough from the switch. With the internal oscillator disabled, the VCP pin must be driven with 80 V dc from an external voltage supply. An external 80 V dc must be applied at the EXT_VCP SubMiniature Version V (SMB) connector, located on the EVAL-ADGM1304SDZ. With the oscillator disabled, the switch can be controlled by parallel logic interface (as shown in Table 4) or via the SPI. With the internal oscillator disabled, the ADGM1304 only consumes a maximum supply current of 50 µA.

R10 to R16 are the place holder locations for the 10 MΩ shunt resistors, which can be placed on all RFx pins (RF1 to RF4, and RFC) to avoid floating nodes. For more details, see the ADGM1304 data sheet.

The ADGM1304 comes with a standard LVTTL parallel interface, consisting of four input pins (IN1 to IN4) controlled by the IN1 to IN4 links. See Table 4 for more details on the logic control when using the parallel interface.

The ADGM1304 also has an SPI interface that can be controlled by the P1 to P4 links. The SPI interface is enabled when the MODE link is at the SPI position. When the MODE link is at the PIN position, the parallel interface is enabled, as detailed in Table 2.

Table 2. Mode Link Position

Position	Description
PIN (Default)	Parallel interface is enabled.
SPI	SPI interface is enabled, parallel interface is disabled.

Table 3. EXTD_EN Link Position

Position	Reference Clock Setting
INT (Default)	Built in 10 MHz oscillator enable.
EXT	Disables the internal oscillator.

RFx to RFC Switch Control

The IN1 to IN4 input pins control the switch state and operation mode of the ADGM1304 in parallel interface mode. The EVAL-ADGM1304SDZ allows the user to control these pins by using the IN1 to IN4 links and P1 to P4 links (see Table 4) or by applying external signals to the SMB connectors (IN1 to IN4, respectively) in parallel interface mode. To apply external digital signals via SMA connectors to the IN1 to IN4 links, headers must be removed so that IN1 to IN4 links are left floating.

Table 4. P1 to P4 and IN1 to IN4 Link Settings for Parallel Interface

Controlled RF Switch	RF Switch Status	Link Name	Link Position
RF1 to RFC	On	P1	D_IN1
		IN1	On
	Off	P1	D_IN1 (default)
		IN1	Off (default)
RF2 to RFC	On	P2	D_IN2
		IN2	On
	Off	P2	D_IN2 (default)
		IN2	Off (default)
RF3 to RFC	On	P3	D_IN3
		IN3	On
	Off	P3	D_IN3 (default)
		IN3	Off (default)
RF4 to RFC	On	P4	D_IN4
		IN4	On
	Off	P4	D_IN4 (default)
		IN4	Off (default)

EVALUATION BOARD SOFTWARE FOR SPI INTERFACE

INSTALLING THE SOFTWARE

The EVAL-ADGM1304SDZ evaluation board uses the Analog Devices Analysis | Control | Evaluation (ACE) software. The ACE software is a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE installer installs the necessary SDP drivers and .NET Framework 4 by default. Install the ACE software before connecting the SDP-B board. The ACE software, as well as installation and operation instructions, can be found on the Analog Devices website at www.analog.com/ace.

After the installation is finished, the EVAL-ADGM1304SDZ evaluation board plug-ins appear when opening the ACE software.

INITIAL SETUP

To set up the evaluation board, take the following steps:

1. Change the position of P1, P2, P3, and P4 links to SDI, $\overline{CS}$, SCLK, and SDO, respectively.
2. Change the position of IN1 to IN4 links to the OFF position.
3. Change the MODE link position from PIN to SPI and keep EXTD_EN link position set at INT.
4. Connect the evaluation board to the SDP-B board and connect the SDP-B board to the computer via a USB cable.
5. Power the evaluation board as described in the Power Supply section.
6. Run the ACE software. The EVAL-ADGM1304SDZ board plug-ins appear in the attached hardware section of the **Start** tab (see Figure 2)
7. Double-click the evaluation board plug-in to open the evaluation board view, as shown in Figure 3.
8. The chip block diagram can be accessed by double-clicking the ADGM1304 chip (see Figure 3). This view provides a basic representation of functionality of the board. The main functions are labeled in Figure 4.

Table 5. SPI Interface Links Description

Links	Position	Description
P1	SDI	Serial data input pin
P2	$\overline{CS}$	Chip select pin
P3	SCLK	Clock input pin
P4	SDO	Serial data output pin

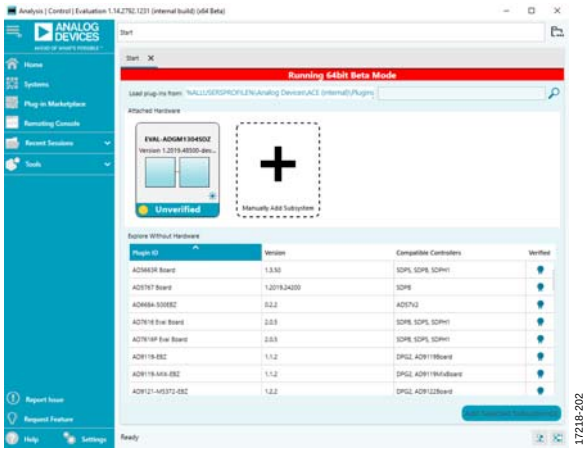

Figure 2 EVAL-ADGM1304SDZ Plug-In Startup Window

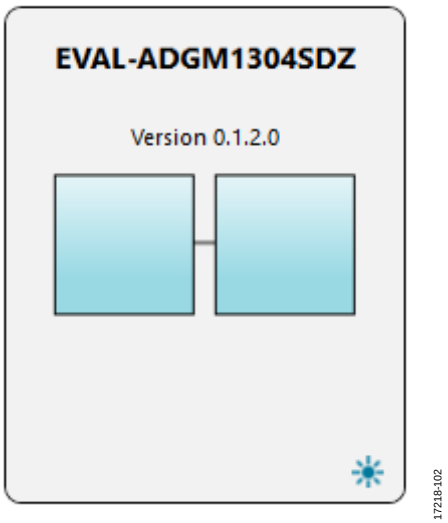

Figure 3. Evaluation Board View of the EVAL-ADGM1304SDZ

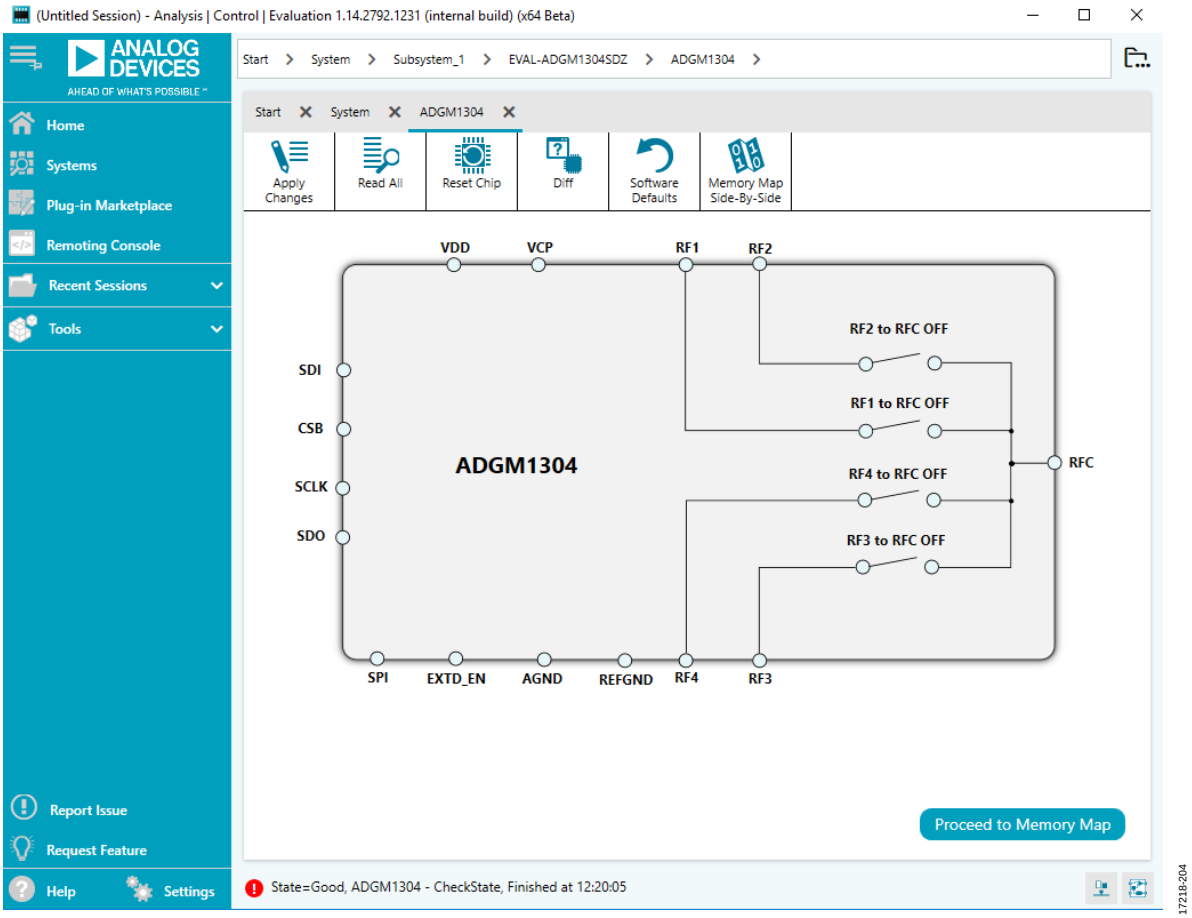

Figure 4. Chip Block Diagram View for the ADGM1304

BLOCK DIAGRAM AND DESCRIPTION

The EVAL-ADGM1304SDZ software is organized to appear similar to the functional block diagram shown in the ADGM1304 data sheet for simplified correlation of the functions on the EVAL-ADGM1304SDZ board with the descriptions in the ADGM1304 data sheet. A full description of each block, register, and their respective settings is given in the ADGM1304 data sheet.

Some of the blocks and their functions are described in Table 6 as they pertain to the evaluation board. The full screen block diagram, shown in Figure 5, describes the functionality of each block.

All changes to the blocks correspond to the block diagram in the software. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are bold are modified values that have not been transferred to the evaluation board. After clicking **Apply Changes**, the data is transferred to the evaluation board.

Table 6. Block Diagram Functions

Label	Function
A	Click the switch symbol to open and close the RF1 to RFC switch.
B	Click the switch symbol to open and close the RF2 to RFC switch.
C	Click the switch symbol to open and close the RF3 to RFC switch.
D	Click the switch symbol to open and close the RF4 to RFC switch.
E	Click **Apply Changes** to apply all modified values to the EVAL-ADGM1304SDZ.

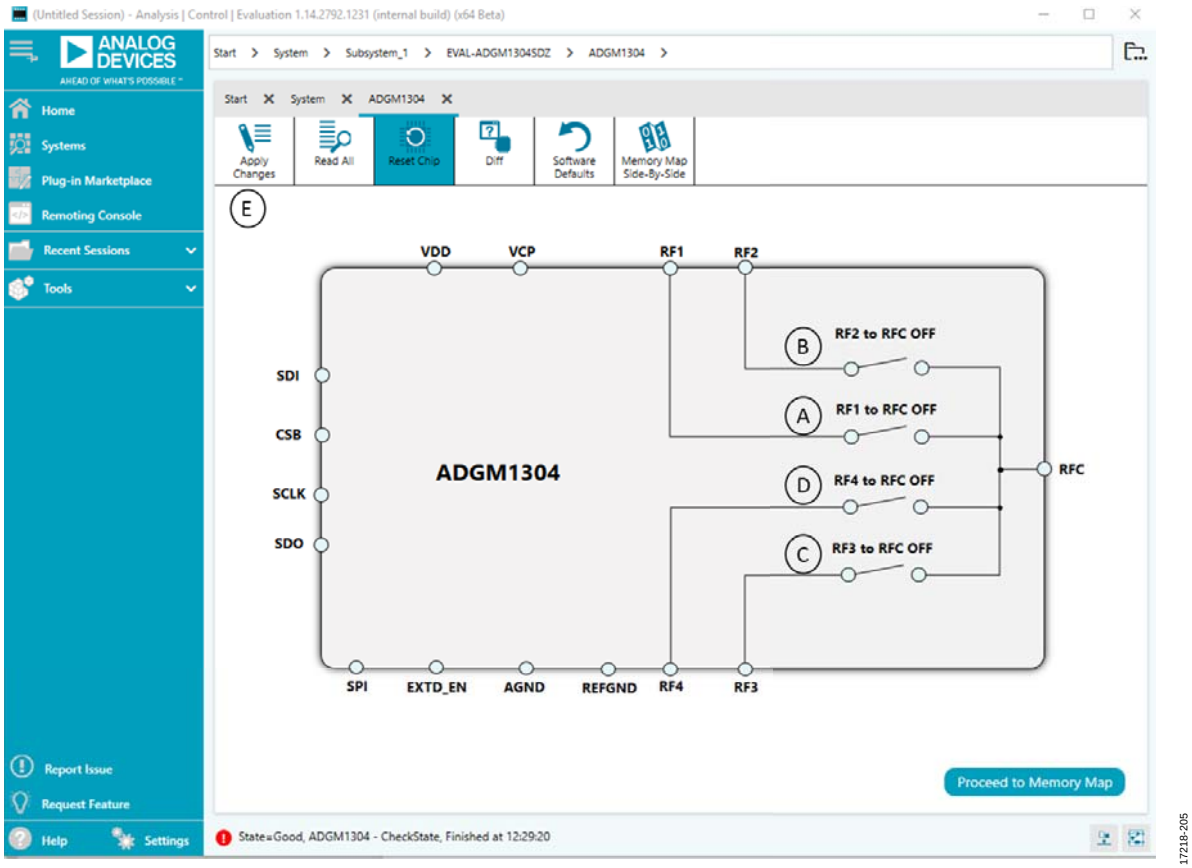

Figure 5. EVAL-ADGM1304SDZ Block Diagram with Labels

MEMORY MAP

MEMORY MAP

All registers are fully accessible from the **ADGM1304 Memory Map** tab, and can be edited at a bit level (see Figure 6). The bits in dark gray are read-only bits and cannot be accessed from the ACE software. All other bits are toggled. The **Apply Changes** button transfers data to the device. All changes made in this tab correspond to the block diagram.

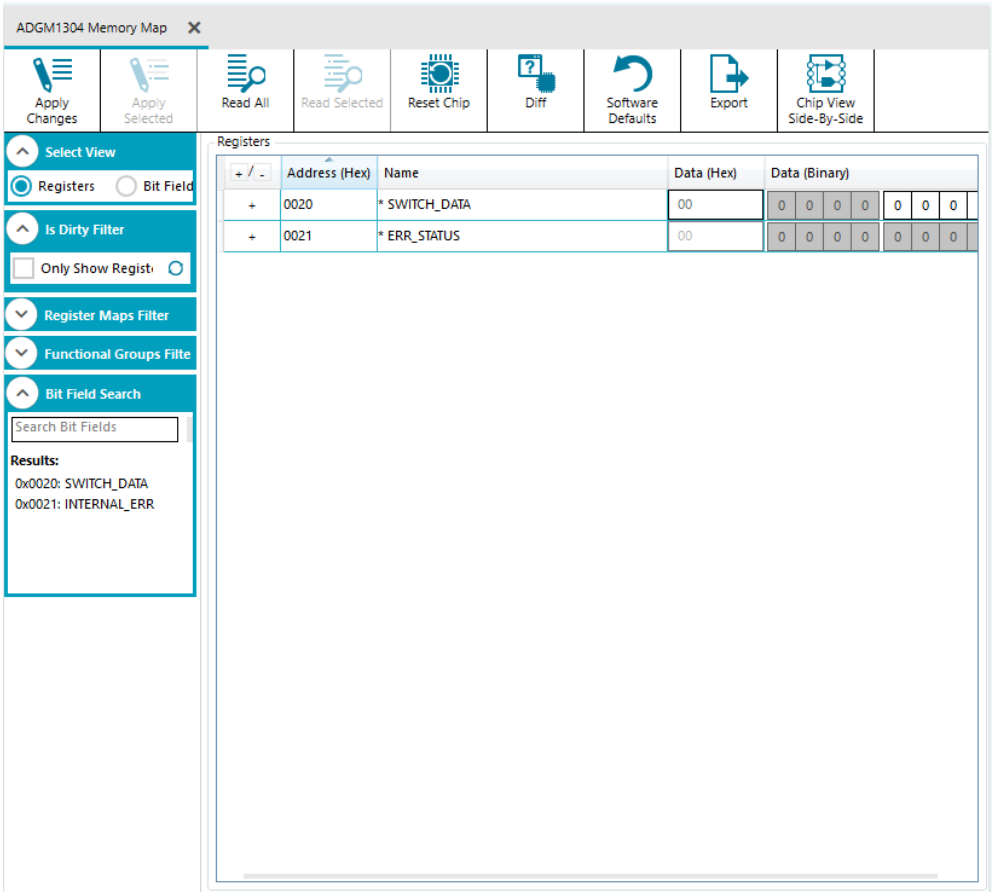

Figure 6. ADGM1304 Memory Map

MEASUREMENT

Figure 1 shows the EVAL-ADGM1304SDZ evaluation board of the ADGM1304. Apply a VDD supply (V_{DD}) to the EVAL-ADGM1304SDZ to measure the performance of the switch. The links are set according to the switch under test (see Table 4). After selecting the desired channel and its state, a network analyzer can collect the switch performance data. Terminate the RF edge connectors of unused switch channels into 50 Ω loads to achieve the full performance of the channel under test.

The EVAL-ADGM1304SDZ comes with a calibration transmission line (CALIBRATION THRU) on the PCB to remove the insertion loss and phase offset of the PCB transmission lines that connect to the switch from the measurement. Figure 8 shows the calibration line and its insertion loss and return loss up to 16 GHz. The calibration line is exactly the same length as the distance from any one RFx connector to the switch pin, plus the distance from the RFC connector to the switch pin. Figure 7 illustrates the definition of the calibration line length. All RF traces connecting to the ADGM1304 are of equal length.

To de-embed the PCB transmission line insertion loss from the entire switch insertion loss board measurement (RF1 to RFC path), the measurement S(2, 1) data must be divided by the |S(2, 1)| of the CALIBRATION THRU. Perform this de-embedding with the network analyzer at the time of the measurement, or after the measurement using individual measurement data files. Refer to the Network Analyzer Calibration Procedure section for more information.

Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct the phase. Enter the time delays into the port extension menu on the network analyzer that correspond to the phase offset introduced from an RF edge connector to the switch pin. Figure 7 shows an example of these phase offsets on a typical switch measurement, labeled as A and B. Both A and B are identical in length and can be calculated by measuring the time delay of the calibration line and dividing it by two.

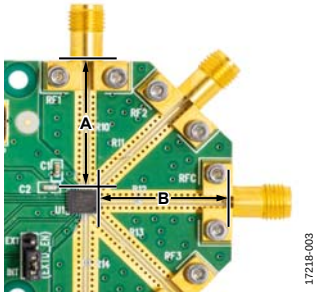

Figure 7. Calibration Transmission Line Length (Equal to A + B)

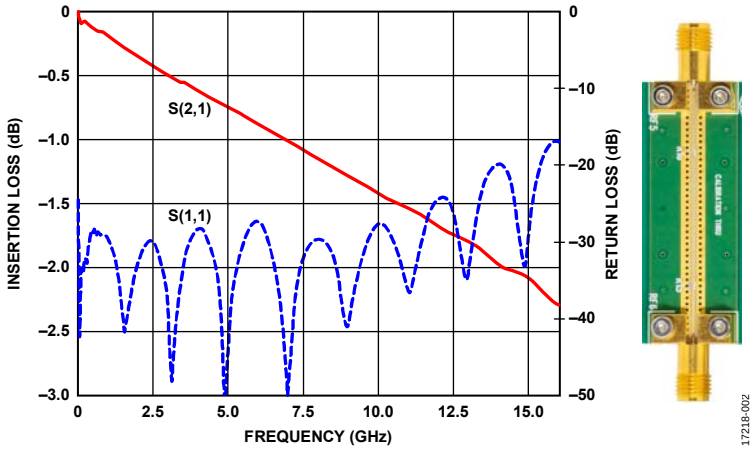

Figure 8. EVAL-ADGM1304SDZ Evaluation Board Calibration Transmission Line Used for PCB Insertion Loss and Phase Offset Correction

Figure 9 shows the ADGM1304 switch insertion loss (network analyzer two port S(2,1) measurement) measurement results that were de-embedded with respect to the PCB transmission line losses. The blue trace is the RF2 to RFC switch channel and the red trace is the RF1 to RFC switch channel. The dashed traces are the respective return loss traces. The performance of the RF2 switch is identical to the RF3 switch, and the performance of the RF1 switch is identical to the RF4 switch.

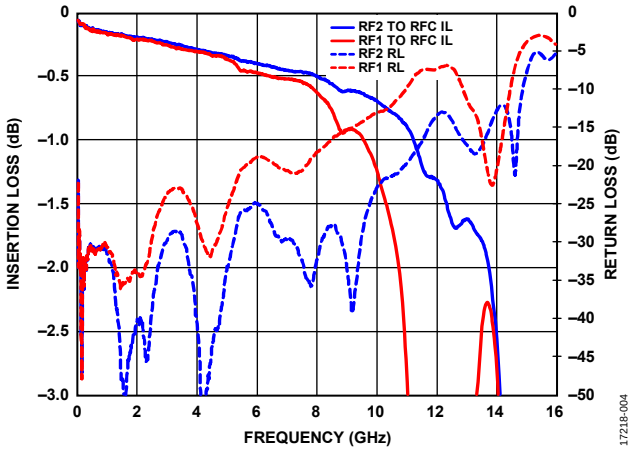

Figure 9. ADGM1304 Insertion Loss Performance, PCB De-Embedded

Figure 10 shows the ADGM1304 switch off isolation performance measurement results for two channels. The blue trace is the RF2 to RFC switch channel, and the red trace is the RF1 to RFC switch channel. The performance of the RF2 switch is identical to the RF3 switch, and the performance of the RF1 switch is identical to the RF4 switch.

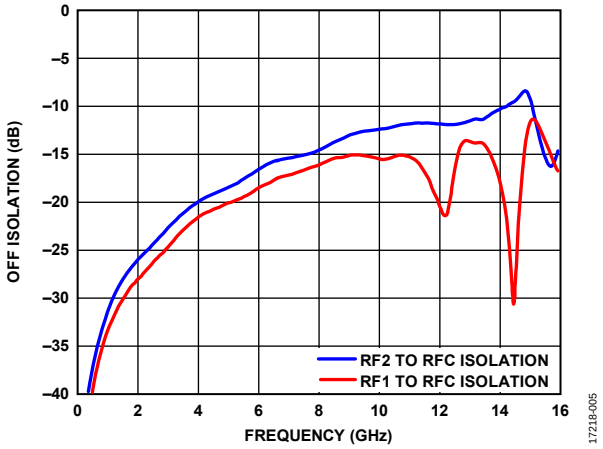

Figure 10. ADGM1304 Off-Isolation Performance

NETWORK ANALYZER CALIBRATION PROCEDURE

Use the following procedure in conjunction with the EVAL-ADGM1304SDZ evaluation board for two port measurements. Two port measurements require the user to have a set of manual calibration standards or an electric calibration type unit to perform a short, load, open, through (SLOT) calibration of the network analyzer. The maximum value of the network analyzer frequency sweep for the EVAL-ADGM1304SDZ PCB can be up to 16 GHz.

1. Perform a full, two-port standard SLOT calibration of the network analyzer.
2. Connect the CALIBRATION THRU calibration line (Connector RF5 and Connector RF6) to the analyzer and measure its insertion loss S(2, 1).
3. Save the measured data to the network analyzer memory for later use.
4. Configure the EVAL-ADGM1304SDZ links and power up the EVAL-ADGM1304SDZ with a 3.3 V dc power supply.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals, if needed.
6. Measure the complete insertion loss of the EVAL-ADGM1304SDZ. Include the insertion loss of the MEMS switch and test fixture (PCB transmission lines and RF connectors).
7. De-embed the PCB losses from the complete evaluation board measurement using the data saved at Step 3 and the measured data at Step 6. The extraction method is dependent on the network analyzer, so the user must consult the documentation of the network analyzer in use before performing the extraction. Typically, the divide function is used to divide the complete S(2, 1) measurement data by the CALIBRATION THRU line S(2, 1) data stored in memory.
8. Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delay values into the port extension menu on the network analyzer for each RF edged connector to switch the pin path equal to the electrical length of the calibration line divided by two.

HANDLING GUIDELINES

Adhere to the following handling guidelines when using the EVAL-ADGM1304SDZ:

- Always treat the ADGM1304 as a static sensitive device and observe normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps, and using other electrostatic discharge (ESD) control devices.
- Take care when connecting signals. Hold the EVAL-ADGM1304SDZ from the edges to avoid any damage to the device under test (DUT).
- Avoid connecting live signal sources to the EVAL-ADGM1304SDZ. Ensure that outputs are switched off (preferably grounded) before connecting to the DUT. Ensure that all instrumentation shares a common chassis ground.
- Avoid running measurement instruments such as digital multimeters (DMMs) in autorange modes. Some instruments generate large transient compliance voltages when switching ranges.
- Use the highest practical range (lowest resolution) setting for resistance measurements to minimize compliance voltages.
- Physically handle the EVAL-ADGM1304SDZ with care.

EVALUATION BOARD SCHEMATIC AND ARTWORK

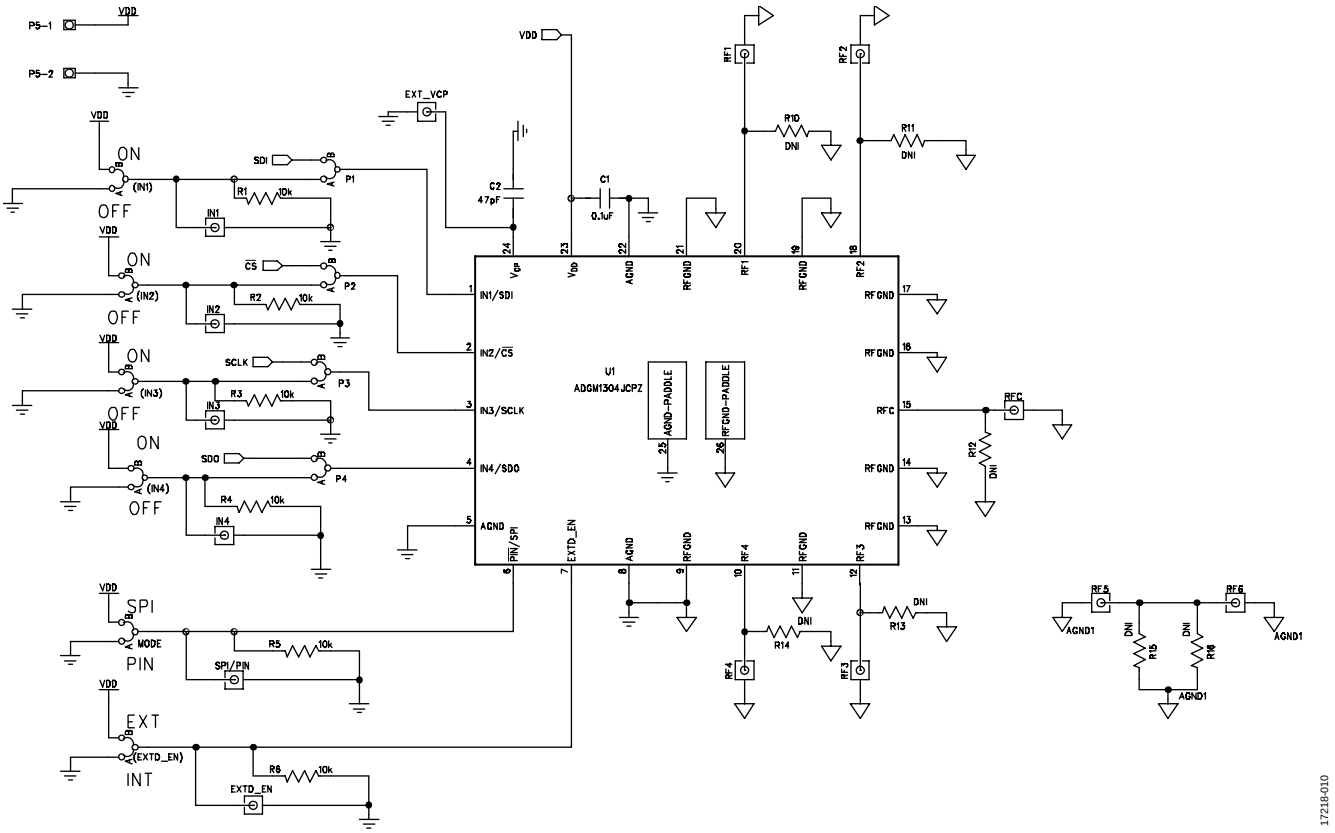

Figure 11. Schematic of the EVAL-ADGM1304SDZ

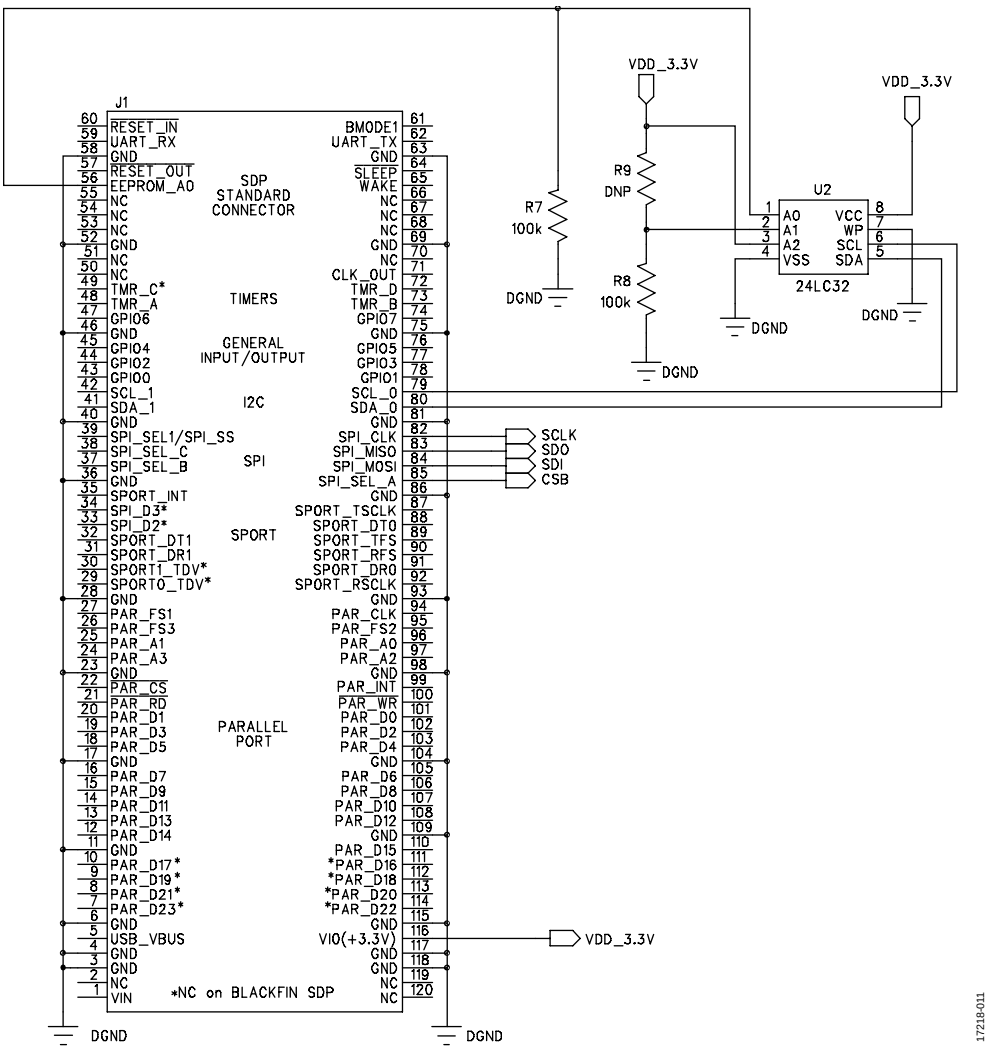

Figure 12. Schematic of the EVAL-ADGM1304SDZ Showing SDP Connector

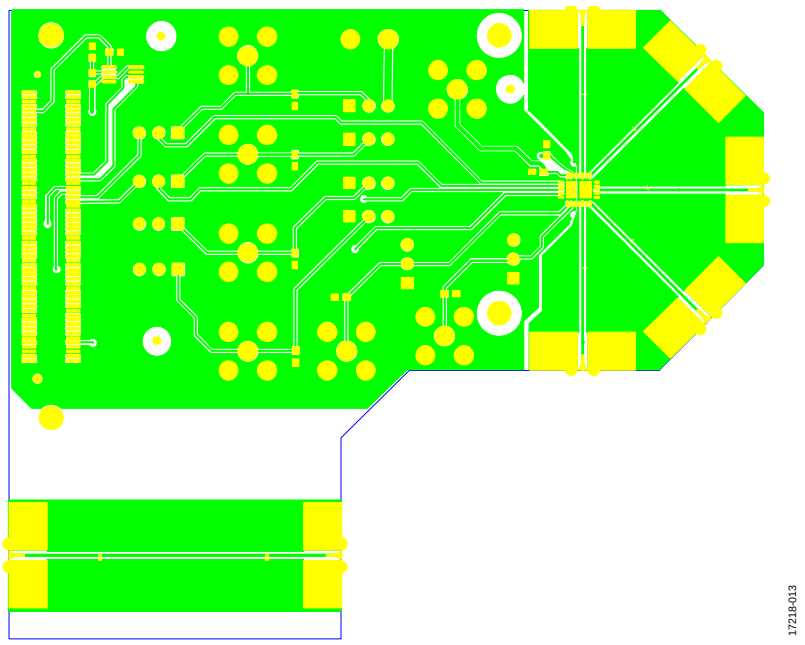

Figure 13. EVAL-ADGM1304SDZ Component Side PCB Drawing (Layer 1)

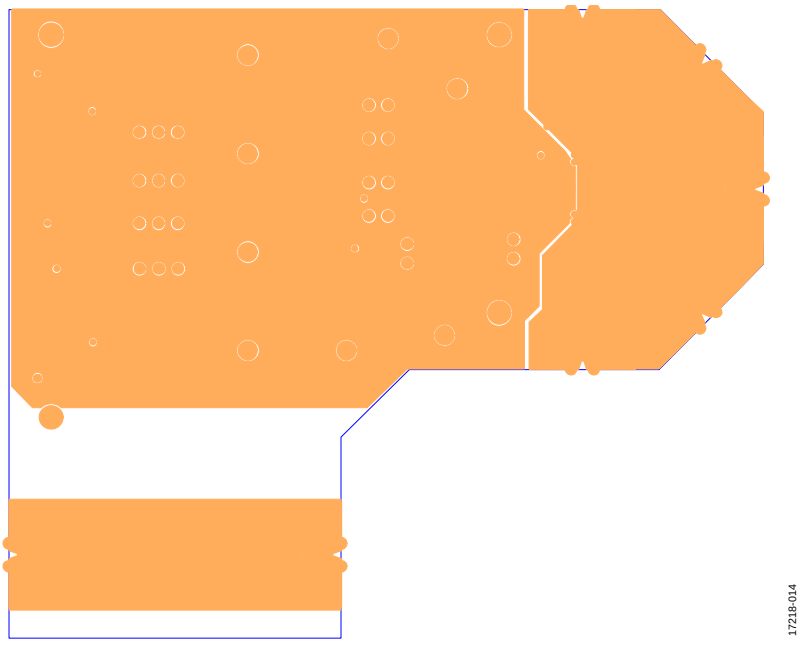

Figure 14. EVAL-ADGM1304SDZ Component Side Ground Plane PCB Drawing (Layer 2)

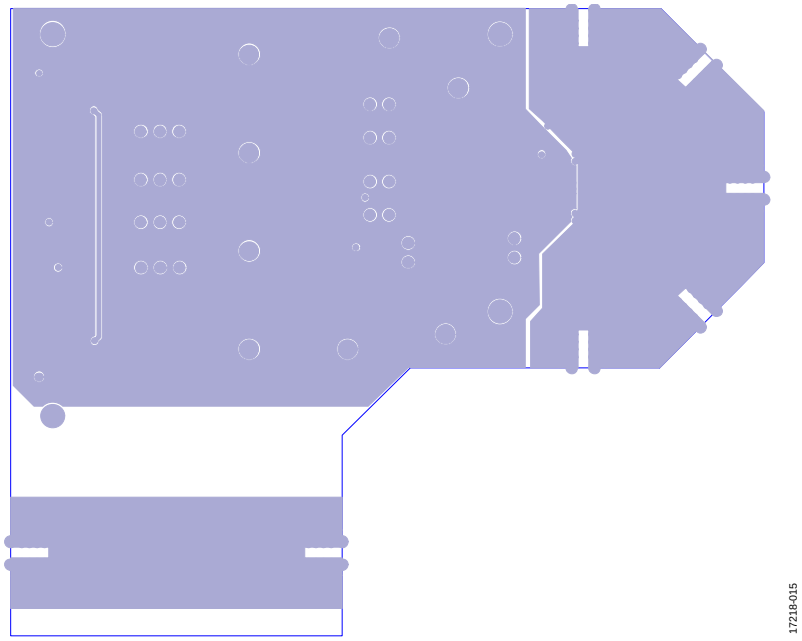

Figure 15. EVAL-ADGM1304SDZ Component Side Ground Plane PCB Drawing (Layer 3)

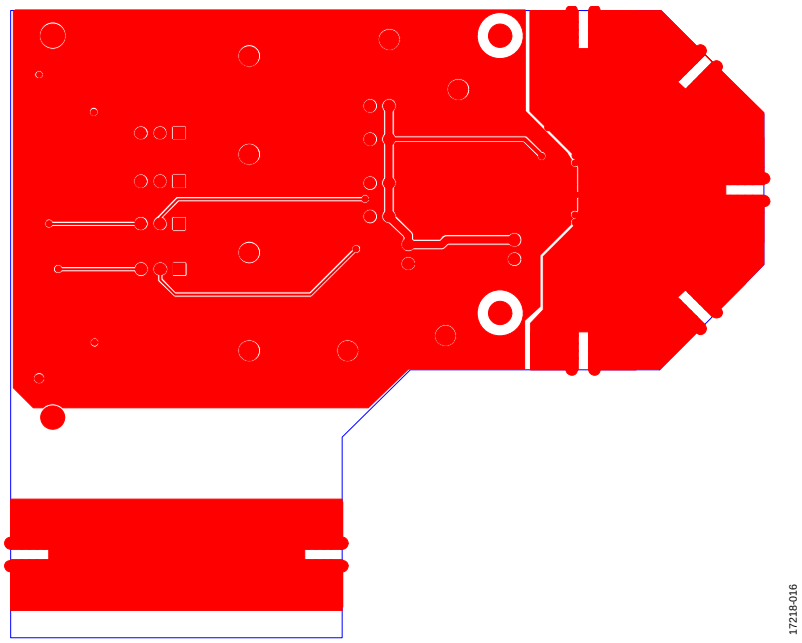

Figure 16. EVAL-ADGM1304SDZ Component Side, Bottom Side PCB Drawing (Layer 4)

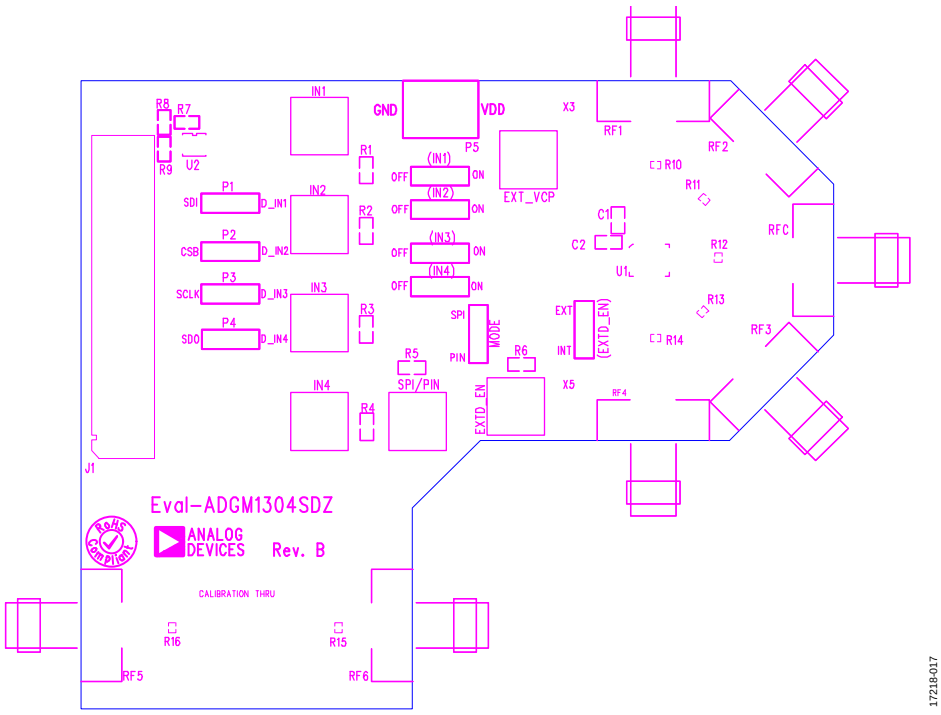

Figure 17. EVAL-ADGM1304SDZ Component Side Silkscreen PCB Drawing (Top)

Metal 1	Finished Copper Plating: 1.5 oz (2.1 thou/53 µm)
	Rogers RO4003C: 8 thou laminate, Er 3.38 starting copper weight 0.5 oz/0.5 oz
Metal 2	Copper Weight: 1 oz (1.4 thou/35 µm)

~37.2 thou FR4

Metal 3	Copper Weight: 1 oz (1.4 thou/35 µm)
	Rogers RO4003C: 8 thou laminate, Er 3.38 starting copper weight 0.5 oz/0.5 oz
Metal 4	Finished Copper Plating: 1.5 oz (2.1 thou/53 µm)

CPWG RF trace width:	15 thou
CPWG RF trace to ground gap:	12.2 thou
Final overall PCB thickness:	62 thou
Final copper plating thickness on top and bottom layers:	1.5 oz

11963-012

Figure 18. EVAL-ADGM1304SDZ PCB Stack Up with Coplanar Waveguide with Ground (CPWG) Dimensions

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Quantity	Reference Designator	Description	Part Number	Manufacturer
1	C1	0.1 µF, 0603 package, 16 V, X7R, surface mount device (SMD) ceramic capacitor	MCB0603R104KCT	Multicomp Pro
1	C2	47 pF, 0603 package, 100 V, C0G/NP0 capacitor	06031A470JAT2A	AVX Corporation
7	IN1 to IN4, EXT_EN, EXT_VCP, SPI/PIN	50 Ω SMB connector through holes	SMB1251B1-3GT30G-50	Amphenol
6	(IN1) to (IN4), (EXTD_EN), MODE, P1 to P4	3-pin silicone headers and shorting links	M20-9990345 and M7566-05	Harwin
1	P5	2-pin terminal block (5 mm pitch)	KRM 02	Lumberg
1	J4	FX8-120S-SV(21), 120-way connector, 0.6 mm pitch	FX8-120S-SV(21)	Hirose(HRS)
6	R1 to R6	10 kΩ (0603 package) SMD resistors	MC0063W0603110K	Multicomp
2	R7 to R8	100 kΩ (0603 package) SMD resistors	MC0063W06031100K	Multicomp Pro
1	R9	Not populated	Not applicable	Not applicable
7	R10 to R16	10 MΩ (0201 package) SMD resistors, not populated	Not applicable	Not applicable
9	RF1 to RF6, RFC	50 Ω side launch SMA connectors	32K243-40ML5	Rosenberger
1	U1	0 Hz/dc to 14 GHz, single-pole, four-throw MEMS switch with integrated driver	ADGM1304	Analog Devices
1	U2	24LC32A-I/MS, 32 kΩ, I²C serial electronically erasable programmable read-only memory (EEPROM)	24LC32A-I/MS	Microchip
3	Not applicable[1]	Wideband 50 Ω termination SMA loads	PE6081	Pasternack

[1] Screwed on at measurement time (see Figure 1).

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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