Interfacing the ADL5382 Quadrature I/Q Demodulator to the AD9262 16-Bit Continuous Time Sigma-Delta ADC as an RF-to-Bits Solution

CIRCUIT FUNCTION AND BENEFITS

This two chip solution consisting of the ADL5382 and AD9262 provides an RF-to-bits solution with optimized performance, low cost, and minimal board space. This two chip combination uses a single frequency translation step to convert the RF channel directly to the baseband without intermediate frequency translations. The frequency translation is accomplished by the ADL5382, a broadband quadrature I/Q demodulator that covers the RF input frequency range from 700 MHz to 2.7 GHz. The ADL5382 is followed by the AD9262, which is a 16-bit dual continuous time sigma-delta (Σ-Δ) analog-to-digital converter (ADC). The characteristics of the continuous time Σ-Δ architecture allow the demodulator to connect directly with the ADC, relaxing the ADC drive and antialiasing requirements. This circuit is easy to use and requires minimal supporting circuitry and board space.

Two chip solutions are ideal for the following applications: quadrature receivers supporting CDMA2000, W-CDMA, WiMAX, and LTE; quadrature sampling instrumentation; medical equipment; and radar. Especially in quadrature receiver systems, the ADL5382 offers the RF bandwidth, while the AD9262 offers ease of integration and an integrated dc and quadrature error correction algorithm. In direct conversion or other quadrature systems, mismatches between the real (I) and imaginary (Q) signal paths cause frequencies in the positive spectrum to image into the negative spectrum and vice versa. These mismatches may occur from gain or phase mismatches in the ADL5382 or in any components in the ADC signal chain itself. The integrated quadrature error correction (QEC) algorithm of the AD9262 attempts to measure and correct the amplitude and phase imbalances of the I and Q signal paths to achieve higher levels of image suppression than are achievable by analog means alone. As part of the AD9262 QEC function, the dc correction applies a notch filter at dc to remove LO-to-RF leakage and dc offsets in the baseband signal.
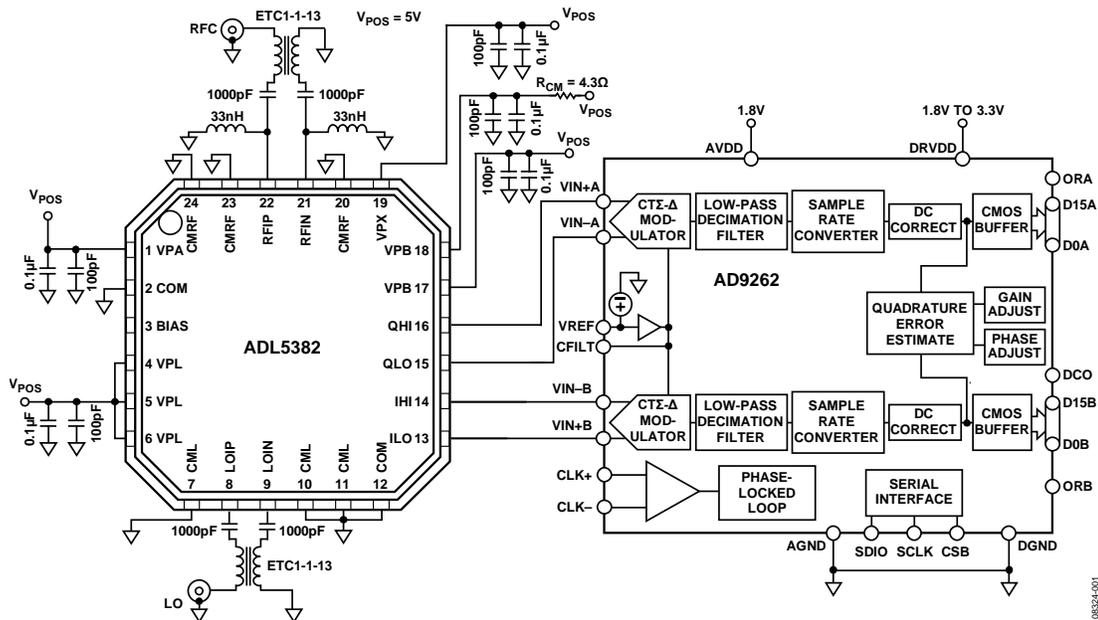

Figure 1. Interface Between the ADL5382 and AD9262 in a Direct RF-to-Bits Application (Simplified Schematic, All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

Table 1. Devices Connected/Referenced

Product	Description
ADL5382	700 MHz to 2700 MHz quadrature demodulator
AD9262	16-bit dual continuous time sigma-delta ADC

Figure 1 shows this two chip solution, which performs direct downconversion from RF-to-bits with minimal supporting circuitry. The ADL5382 supports LO and RF frequency ranges of 700 MHz to 2.7 GHz. Drive the LO and RF ports differentially through a balun, and the recommended balun is the Mini Circuits TC1-1-13+. The LO and RF inputs are designed for a broadband 50 Ω match and must be ac-coupled with 1000 pF capacitors. Ground-referenced choke inductors must also be connected to RFIP and RFIN (the recommended value is 33 nH Coilcraft 0603CS-33NX) for appropriate biasing. The purpose of the choke inductors is to provide a very low resistance dc path to ground and a high ac impedance at the RF frequency so as not to affect the RF input impedance.

The I/Q outputs of the ADL5382 allow direct connection to the ADC inputs of the AD9262. This seamless interface is made possible by the continuous time Σ-Δ input structure. Unlike traditional switched capacitor designs, the AD9262 inputs are resistive. The differential input impedance between VIN+ and VIN− pins is a fixed resistance of 1000 Ω. This high input impedance allows for a more optimized and linear input interface to the ADL5382. In addition, the continuous time Σ-Δ architecture possesses an inherent antialiasing function. Therefore, a filter network between the ADL5382 and AD9262 may not be necessary. Depending on the application and the system design, a low-order roofing filter may be necessary for large out-of-band blockers.

An external clock input or the integrated integer-N phase-locked loop (PLL) provides the 640 MHz internal clock needed for the oversampled continuous time Σ-Δ modulator. On-chip decimation filters and sample rate converters reduce the modulator data rate from 640 MSPS to a user-defined output data rate between 30 MSPS to 160 MSPS, enabling a more efficient and direct interface.

An important consideration when interfacing the ADL5382 to the AD9262 is achieving the proper common-mode level as specified by the Channel A and Channel B inputs of the AD9262. The AD9262 requires a common-mode voltage of 1.8 V at the VINxA/VINxB input pins, while the I/Q outputs of the ADL5382 have a common-mode voltage of VPOS −2.8 V. VPOS is the positive power supply of the ADL5382, and its nominal value is 5 V.

To achieve equivalent common-mode levels between the ADL5382 and AD9262, a series resistor, R_{CM}, is placed between VPOS and Pin 18 of the ADL5382. Pin 18 specifies the common mode of the I/Q outputs and, therefore, it must ideally reside at 4.6 V to achieve a 1.8 V common mode for VPOS = 5 V. Set the series resistor to a low resistance value of 4.3 Ω. This introduces a 0.39 V drop below the 5 V supply due to the 91 mA of current that flows into Pin 18. With Pin 18 at approximately 4.6 V, the output common-mode voltage is the required value of 1.8 V.

The total solution for RF-to-bits using the ADL5382 and AD9262 offers substantial space savings on the printed circuit board (PCB) and ease of use while maximizing dynamic performance. Because a higher order antialiasing filter and a driver amplifier are not required, the overall design is a more compact solution. In addition, the ADL5382 and AD9262 are both offered in small footprint packages, therefore, adding to the space savings on the PCB. The ADL5382 is supplied in a 24-lead, 4 mm × 4 mm LFCSP package and the AD9262 in a 9 mm × 9 mm LFCSP. The complete solution consisting of the ADL5382 and AD9262 supports 33 dBm of input IP3 and better than 70 dBm of input IP2 at 900 MHz. The available system bandwidth is 10 MHz real or 20 MHz complex. The digital outputs of the AD9262 allow a programmable output data rate within the range of 30 MHz to 160 MHz.

The circuit must be constructed on a multilayer PCB with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see MT-031 Tutorial and MT-101 Tutorial).

COMMON VARIATIONS

The ADL538x family of demodulators and the AD926x family of continuous time Σ-Δ ADCs offer a wide selection of RF frequency ranges and digital output configurations. Depending on the application and the performance requirements, one configuration may be better suited than another. The selection of demodulators includes the ADL5380 and the ADL5382. The ADL5380 offers a wider RF frequency range, 400 MHz to 6 GHz, compared to the ADL5382. However, trade-offs must be made in linear performance for bandwidth. Either the ADL5382 or ADL5380 can directly interface with the AD9262 or the AD9267 to complete the RF-to-bits two chip solution. The AD9262 consists of a continuous time Σ-Δ modulator and back-end digital signal processing to allow CMOS outputs at 30 MSPS to 160 MSPS. The AD9267 consists of only the Σ-Δ modulator, and the output data rate is fixed at 4-bit LVDS at 640 MSPS. This allows users who need to perform their own signal conditioning to choose the AD9267. The combination of demodulators and ADCs allow four possible configurations, and each configuration offers their strengths and weakness. Therefore careful system analysis is necessary to determine the configuration that best suits the application.

LEARN MORE

Luu, Qui and Richard Schreier. "Understanding Continuous-Time, Discrete-Time Sigma-Delta ADCs And Nyquist ADCs," *Electronic Design*. February 20, 2009.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-080 Tutorial, *Mixers and Modulators*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets

ADL5382 Data Sheet.

AD9262 Data Sheet.

REVISION HISTORY

5/13—Rev. 0 to Rev. A
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