ANALOG DEVICES

Circuit Note
CN-0239

Circuits from the Lab® Reference Designs

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Devices Connected/Referenced	
ADF4351	3 5 MHz to 4400 MHz, Wideband Synthesizer with Integrated VCO
ADL5801	10 MHz to 6 GHz, Wideband Active Mixer

Broadband 6 GHz Active Mixer with a Glueless Local Oscillator Interface

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

ADL5801 Evaluation Board (ADL5801-EVALZ)
ADF4351 Evaluation Board (EVAL-ADF4351EB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a 10 MHz to 6 GHz wideband active mixer with a direct interface to a frequency synthesizer-based low phase noise local oscillator (LO).

This circuit offers an optimum solution that is attractive in wideband applications that require frequency conversion to higher or lower frequencies. The two-chip circuit covers a broad LO frequency range from 35 MHz to 4400 MHz. The LO interface is simple and glueless, eliminating the need for a balun, matching network, and LO buffer. In addition, the mixer bias adjust function allows optimization of IP3, noise figure, and supply current based on the application requirements or on the size of the input signal.

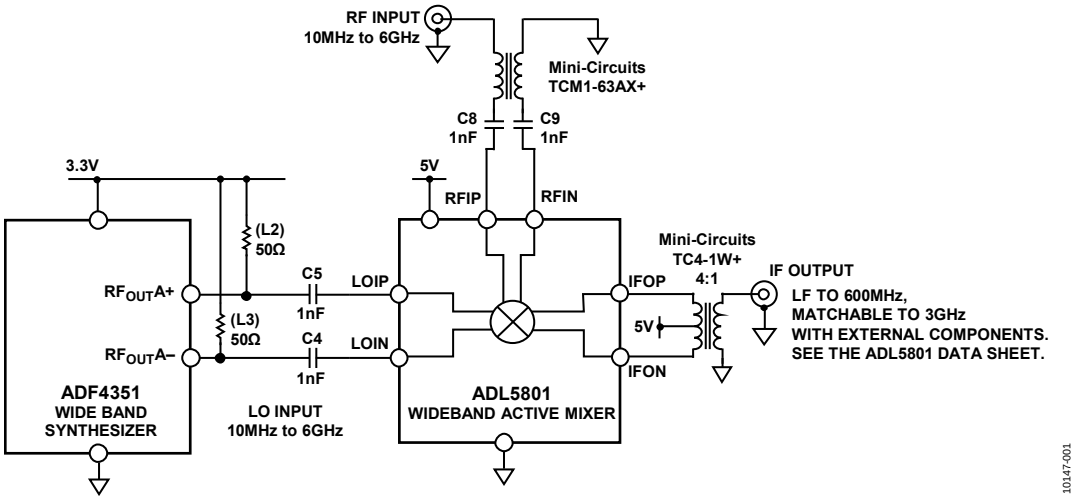

Figure 1. Broadband Interface Between ADF4351 PLL with Integrated VCO and ADL5801 Broadband Active Mixer (Simplified Schematic Showing Only Interface Details)

Rev. A

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CIRCUIT DESCRIPTION

The ADF4351 is a wideband, fractional-N and integer-N phase-locked loop (PLL) that covers frequencies from 35 MHz to 4400 MHz. The device has an integrated voltage controlled oscillator (VCO) with a fundamental frequency range from 2200 MHz to 4400 MHz. Multi-octave operation is achieved through the use of a bank of frequency dividers.

The ADL5801 is a high linearity, double balanced, active mixer with an integrated LO buffer amplifier that supports RF frequencies from 10 MHz to 6000 MHz. The mixer has a bias adjust feature to optimize the input linearity, noise figure and dc operating current. The circuit shown in Figure 1 has a simple LO interface for applications that require broadband up or down conversion. The interface provides coverage for RF frequencies ranging from 35 MHz to 4400 MHz.

The ADF4351 PLL has a differential LO output interface, and the ADL5801 is optimized for differential LO drive. Differential interfaces provide common-mode noise rejection and cancellation of even order harmonics.

Normally, pull-up bias inductors are recommended at the output port of the ADF4351. This solution delivers higher output power but limits the frequency range of the device. The standard evaluation board is equipped with two 7.5 nH pull-up inductors, which is optimal for frequencies above 500 MHz. In the Figure 1 circuit, the bias inductors are replaced with two 50 Ω pull-up resistors to reduce the frequency dependence of the output interface. This change results in lower power delivered at the output; however, the ADL5801 can tolerate this limitation since the device is specified to operate at LO drive levels as low as −10 dBm. Figure 2 is a comparison of the output power delivered by the device with resistive and inductive pull-up networks.

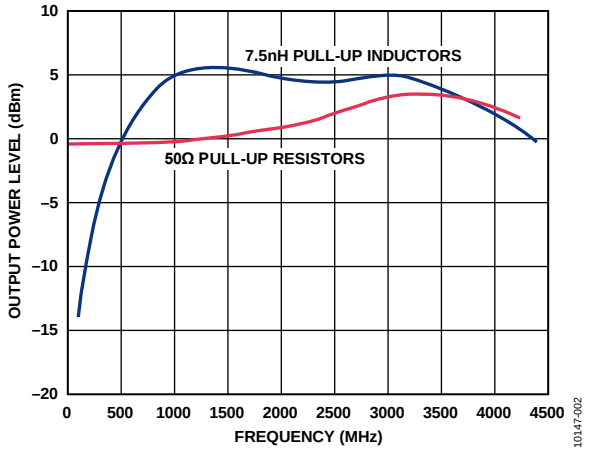

Figure 2. Comparison of the Power Level at the Output of the ADF4351 with Resistive and Inductive Pull-up Networks

The resistive pull-up network presents a nominal differential impedance of 100 Ω at the output, and the differential input impedance of the LO port of the ADL5801 is 50 Ω. The impedance mismatch in the LO path of the mixer does not degrade the circuit performance. However, it is suggested that the length of the traces connecting the devices be kept as short as possible to minimize effects of the impedance mismatch.

The PLL-mixer interface described above exhibits excellent broadband performance as shown in Figure 3 and Figure 4. The circuit maintains an input IP3 of more than 25 dBm at frequencies below 3500 MHz, and 23 dBm up to 4400 MHz. The circuit exhibits conversion gain of more than −0.7 dB and noise figure less than 12.2 dB across the operating frequency band.

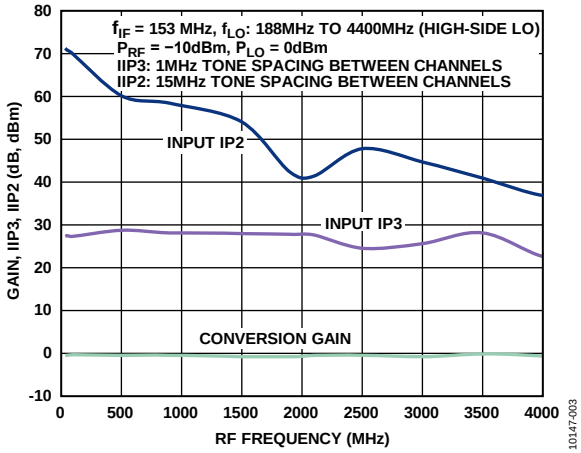

Figure 3. Conversion Gain, Input IP2, Input IP3 vs. RF Frequency

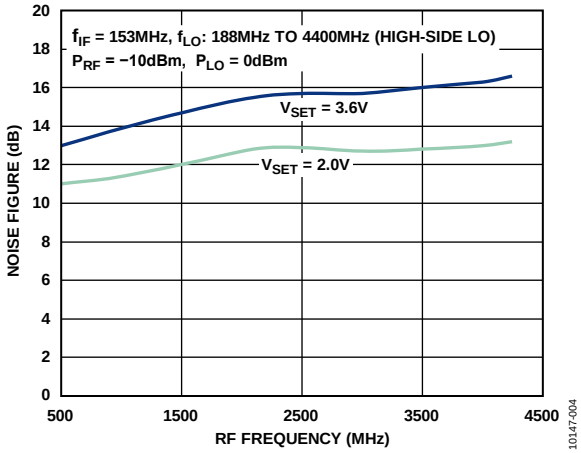

Figure 4. Noise Figure vs. RF Frequency

The power consumed by the circuit depends on the frequency of operation and the bias point of the mixer. The ADF4351 activates a combination of sections in its divider network to generate output frequencies that span multiple octaves. This combination dictates the power consumption of the PLL. For example, when the PLL is programmed to output a frequency of 35 MHz, the device activates all six divider networks and consumes 132 mA of current. This point represents the worst-case power consumption point for the device. Similarly, the bias level of the ADL5801, which can be used to adjust IP3 and noise figure, determines the power consumed by the mixer. The VSET pin is used to adjust the bias level of the device. Figure 5 and Figure 6 show the dc current, input IP3, and noise figure performance of the mixer as a function of the VSET voltage.

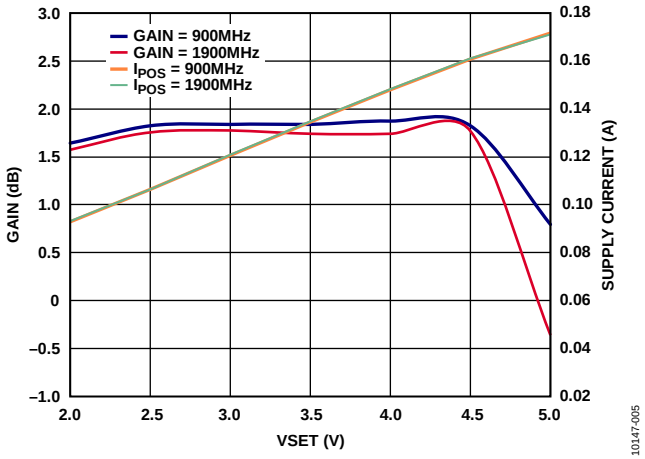

Figure 5. Power Conversion Gain and Supply Current vs. VSET

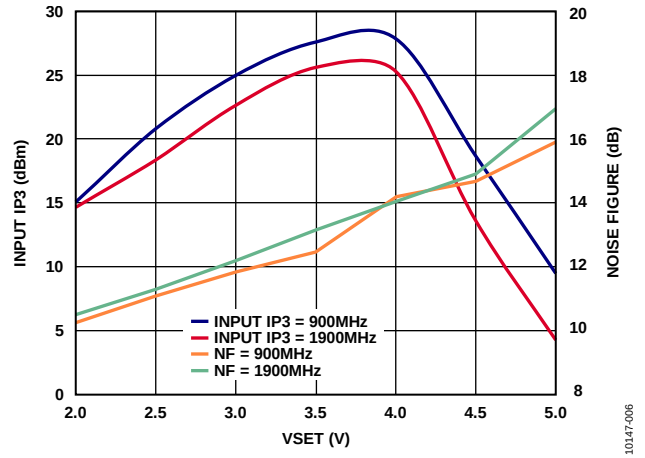

Figure 6. Input IP3 and Noise Figure vs. VSET

The VSET level is directly proportional to the dc operating current and input IP3, while the noise figure is inversely proportional to the VSET voltage. The mixer exhibits the best linearity at a VSET voltage of 3.6 V. At a mixer bias level of 3.6 V and the worst-case power consumption point for the PLL (all dividers on), the circuit consumes approximately 1.14 W.

COMMON VARIATIONS

The interface discussed above is applicable to other PLLs with an integrated VCO and differential outputs such as the ADF4350 or the ADF4360 family of products (ADF4360-0, ADF4360-1, ADF4360-2, ADF4360-3, ADF4360-4, ADF4360-5, ADF4360-6, ADF4360-7, ADF4360-8, and ADF4360-9). The ADF4350, which operates from 135 MHz to 4.4 GHz is pin-compatible with the ADF4351 and exhibits a slightly higher noise figure. The ADF4360 family of integer-N PLLs with integrated VCO is a good fit for applications that require a fixed or narrow range of LO frequencies. These devices help to reduce power consumed by the circuit at the expense of higher phase noise. For applications that require more than one output mixer, the ADL5801 can be replaced with the ADL5802, which is a dual channel active mixer.

CIRCUIT EVALUATION AND TEST

The circuit described was implemented using the standard evaluation boards for the ADF4351 (EVAL-ADF4351EB1Z) and ADL5801 (ADL5801-EVALZ). The EVAL-ADF4351EB1Z evaluation board kit includes a reference crystal oscillator, control software and the programming interface cable required to operate the device. The control software provides options to set the output frequency, power level, reference frequency, and variety of other features.

Table 1 and Table 2 list components modified on the evaluation boards to implement this applications circuit.

Table 1. Component Modifications on EVAL-ADF4351EB1Z

Placeholder	Default Value	New Value
L2, L3	7.5 nH	50 Ω
L1, L4	1.9 nH	0 Ω

Table 2. Component Modifications on ADL5801-EVALZ

Placeholder	Default Value	New Value
T2/T4/T7	Mini-Circuits TCM1-1-13M+	0 Ω
C4, C5	100 pF	1 nF

Test

Figure 8 shows a block diagram of the test setup. The output of the PLL and the LO port of the mixer were bridged using a coaxial thru connector for evaluation. Figure 7 shows a photo of the two connected evaluation boards. The Equipment Needed section lists the equipment used to evaluate the circuit.

Equipment Needed

The following equipment is needed:

- PC running Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit), with USB port
- ADF4351 evaluation board (EVAL-ADF4351EB1Z)
- ADL5801 evaluation board (ADL5801-EVALZ)
- RF signal generator (Rohde & Schwarz SMT06 or equivalent)
- Spectrum analyzer (Rohde & Schwarz FSEA30 or equivalent)
- Power supplies (Agilent E3631 or equivalent)
- EVAL-ADF4351EB1Z: +5.5 V
- ADL5801-EVALZ: +5 V (VPOS), +3.6V (VSET)

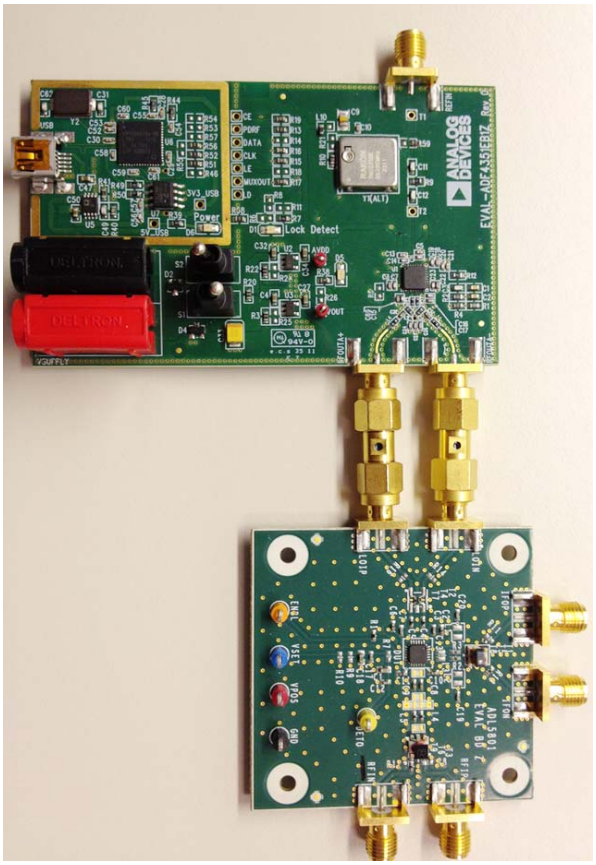

Figure 7. Board Setup Used to Interface the ADF4351 with the ADL5801

The control software was used to program the desired LO frequency and the output power. Figure 9 is a sample screenshot of the software configuration used to drive the ADF4351.

See the UG-435 User Guide, *Evaluation Board for the ADF4351 Fractional-N PLL Frequency Synthesizer* and the UG-476 User Guide, *PLL Software Installation Guide* for further information on setting up the ADF4351.

The ADL5801 was biased with a VSET voltage of 3.6 V using an external power supply. This external bias connection can be replaced with an on-board connection routed through the supply pin using a resistive divider network. Populating placeholder R10 and leaving R7 and R8 open enables this resistive divider network. Table 3 provides the value of R10 required to achieve desired mixer bias level. For additional information, refer to the RF Voltage-to-Current (V-to-I) Converter section in the ADL5801 data sheet.

Table 3. Suggested Values of R10 to Achieve the Desired Mixer Bias Level (I_{POS} is the Corresponding ADL5801 Supply Current)

R10 (Ω)	VSET (V)	I_{POS} (mA)
226	4.5	160
562	4.01	146
568	4	145
659	3.9	142
665	3.89	142
694	3.85	142
760	3.8	139
768	3.79	139
1000	3.6	133
1100	3.53	131
1150	3.5	130
1200	3.47	129
1300	3.4	127
1400	3.35	126
1500	3.3	124
1600	3.26	122
1700	3.21	121
1800	3.17	120
1900	3.14	119
2000	3.1	118
2300	3	114
5900	2.5	98
Open	2.03	82

To demonstrate the capability of the circuit to support RF frequencies from 35 MHz to 4400 MHz, the device was operated in a high-side LO configuration with an IF frequency of 153 MHz.

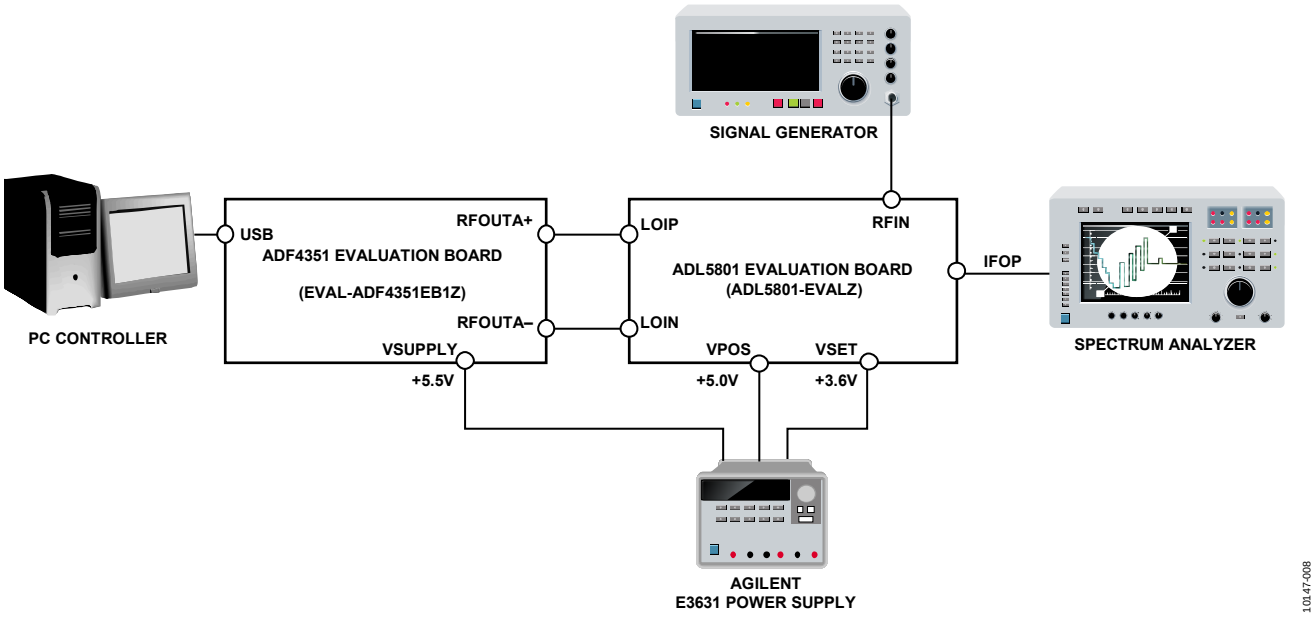

Figure 8. Circuit Evaluation Test Setup Block Diagram

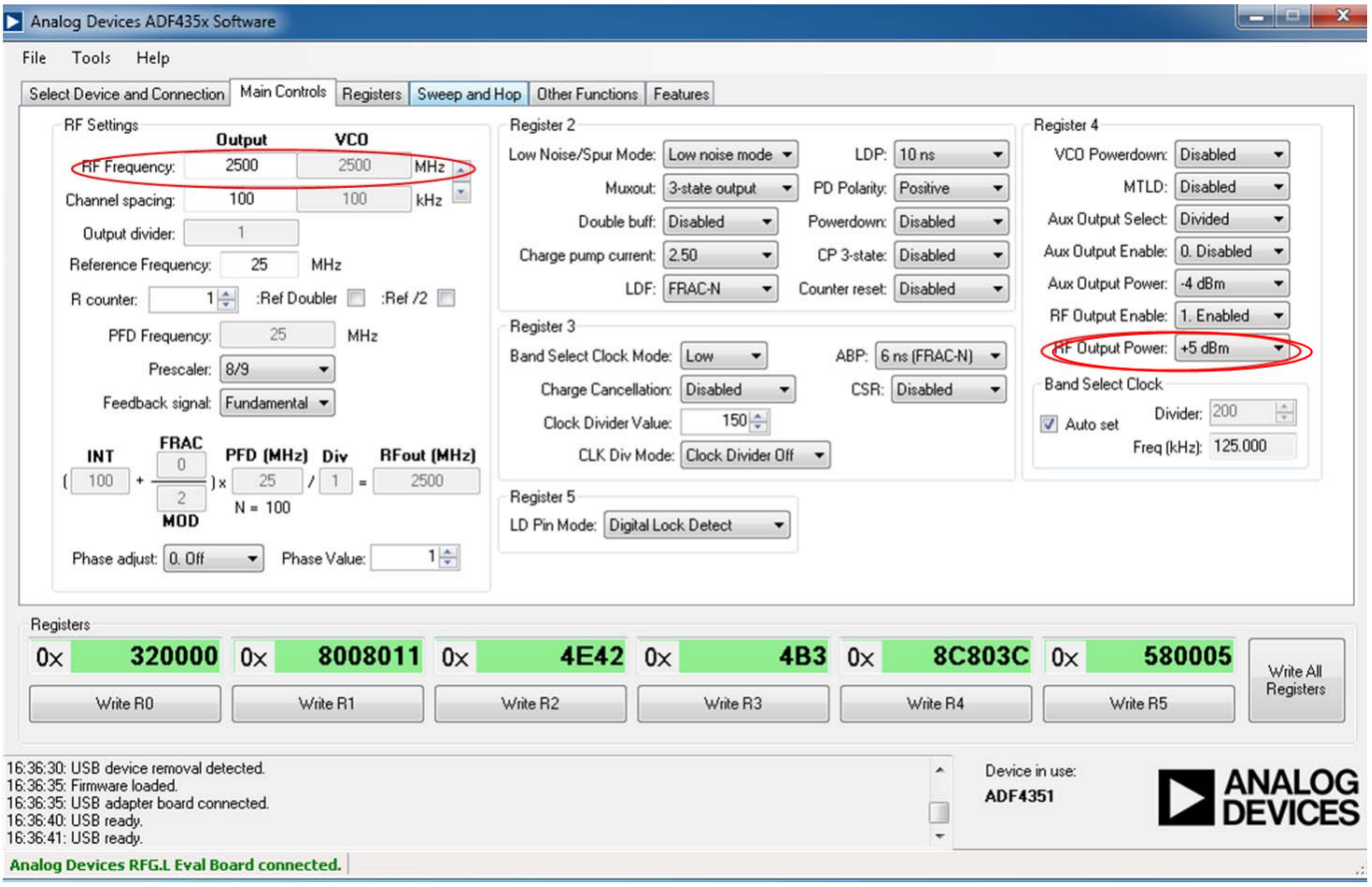

Figure 9. Screenshot of the Software Configuration Used to Drive the ADF4351 (RF Output Frequency and Power Level Settings Highlighted)

LEARN MORE

CN-0239 Design Support Package:
http://www.analog.com/CN0239-DesignSupport

UG-435 User Guide, Evaluation Board for the ADF4351 Fractional-N PLL Frequency Synthesizer.

UG-476 User Guide, PLL Software Installation Guide.

ADIsimRF Design Tool

ADIsimPLL Design Tool

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-086 Tutorial, *Fundamentals of Phase Locked Loops (PLLs)*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

AN-30 Application Note, *Ask the Application Engineer—PLL Synthesizers*, Analog Devices.

Data Sheets and Evaluation Boards

ADF4351 Data Sheet and Evaluation Board

ADL5801 Data Sheet and Evaluation Board

REVISION HISTORY

5/16—Rev. 0 to Rev. A

Changes to Figure 1 1
Changes to Common Variations Section 3
Changes to Figure 9 Caption 5

8/13—Revision 0: Initial Version