
COMPONENTS • TECHNOLOGY • APPLICATIONS
Reed Electronics Group
PCIM EUROPE
POWER ELECTRONICS
JANUARY/FEBRUARY 2003

Single Chip Supervises and Sequences Power Supplies

Have a controlled power-down sequence

Reliability (uptime) has become a major product differentiator in many applications including Internet routers, DSLAMs, base stations, and servers. Systems that must remain operational 99.999% of the time (five nines reliability) are commonplace.

By Peter Canty, Analog Devices

The design of these applications has increased in complexity, however, the chassis used in these applications usually contain a backplane for power and signal distribution, plus multiple daughter cards that plug into it. These printed circuit boards (PCBs)—typically called line cards in routers, DSLAMs and base stations; and blades in servers—are being populated with more DSPs, ASICs, FPGAs,CPLDs and processors, in order to provide customers with greater bandwidth, both in terms of channel count and data rate.

Use of these complex, power hungry devices has created the difficult problem of sequencing the turn-on and turn-off of several power supplies. Many PCBs require multiple supply voltages for operation. DSPs typically require two supplies, one for the core (1.2 V, 1.8 V and 2.5 V are common values), and one for the I/O (2.5 V, 3.3 V or 5 V). FPGAs can require as many as five voltages in order to support multiple I/O protocols such as LVTTL, LVCMOS25, 1.5 V I/O, and HSTL-1. With this proliferation of different voltages, it is common to find as many as six or seven supplies being used to power a board in the applications outlined above.

The sequence in which these supplies turn on can be critical to the reliable operation of the system. A good rule of thumb seems to be to start with the highest supply first and work downwards, but this is not always the case. For instance, some DSP manufacturers recommend that the core of their device be powered up before the I/O, while others recommend the opposite. The truth is that, given the complexity of the PCBs being designed, it may be difficult to determine what the optimal power up sequence is without first designing, building and testing the board. This "trial and error" approach can prove costly, both in terms of manufacturing costs (multiple board spins) and time to market.

As the issue of sequencing becomes more important, power designers are faced with greater design challenges. The current discrete approach to supply sequencing uses reset generators, FET drivers and RCs; a typical implementation is shown below. While this may be adequate for a system requiring two or three supplies, it becomes very cumbersome when that number rises to six or seven. Another problem is that accurate reset generators have fixed threshold voltages. In many ASIC designs, however, a supply voltage must be tweaked to a non-standard value in order to provide maximum performance, but a reset generator with the revised threshold may not exist. Also, with the high level of component interaction, these types of designs require the power designer to guess as to the proper power-up sequence. If this guess (albeit an educated one) proves wrong, it is difficult to rectify the issue without a board spin. Further, as the population density of PCBs increases, real estate becomes an issue and multi-component discrete solutions become unattractive. Further complicating the problem, the power-down sequence, using simple reset generators with fixed timeouts and open drain outputs, is also difficult to design.

The solution, then, is a single IC that provides a total voltage management solution and encompasses all of the functionality of the discrete design shown above. The device needs to go further, however, and provide the flexibility to change its configuration easily, if required. If the alteration of a reset threshold, the power up sequence, the power down sequence, or the watchdog timeout on a processor clock can be

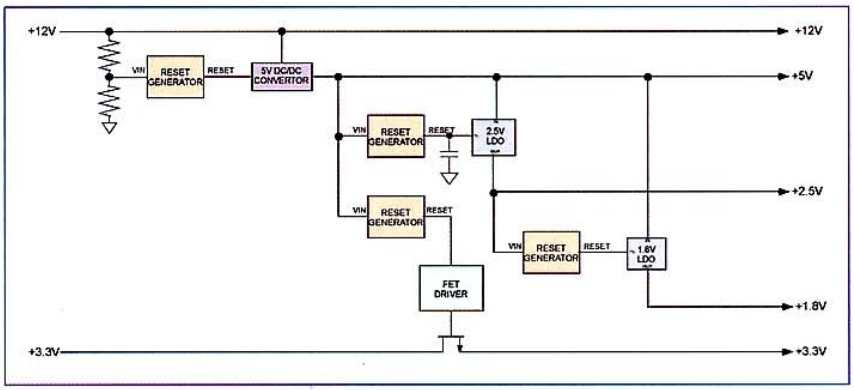

Figure 1. Discrete implementation for sequencing 5 supplies

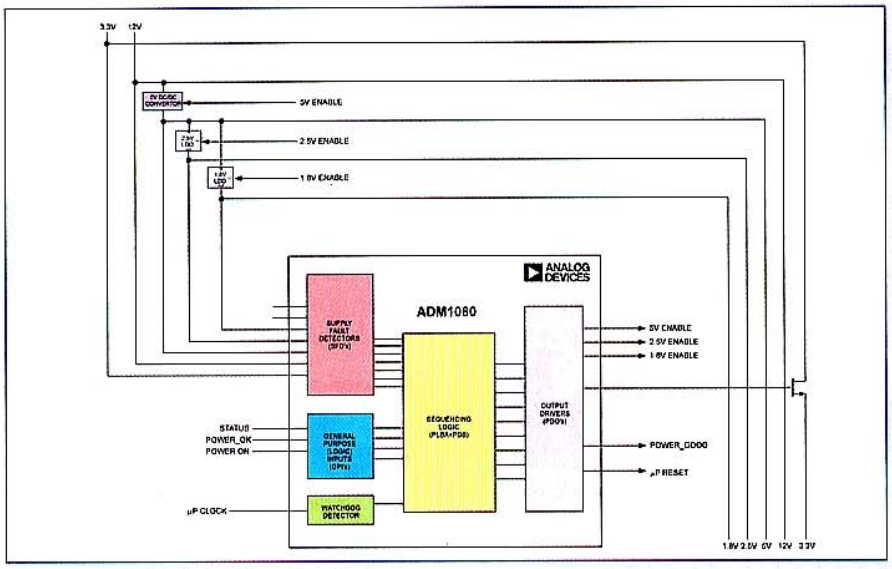

Figure 2. ADM1060 Configuration Software

altered without laying out the hardware again, then the power designer's task is made infinitely easier. A single IC (with minimal external components) also addresses the issue of board real estate. Time to market is also reduced, since the power designer can implement a design quicker, confident in the knowledge that it can be altered later, if necessary, without a change in hardware.

The ADM1060 Multi Supply Supervisory Circuit from Analog Devices is such a device. This is a 28-lead TSSOP voltage management device designed specifically to address the issues outlined above. The device can supervise multiple supplies and sequence the order in which those supplies are applied to the board. It features a flexible architecture that allows the user to alter its configuration quickly and easily. This is done using an intuitive software interface provided with the device.

The device includes seven supply fault detectors (SFDs). These perform the function of reset generators but with a much greater level of flexibility. Firstly, both overvoltage and undervoltage thresholds can be set, such that a fault can also be generated if a supply surges or drifts too high. Secondly, the thresholds are programmable over a wide range. The threshold of one SFD can be programmed from 2 V to 14.4 V. Four of the SFDs can be programmed from 0.6 V to 6 V. Two can also look at negative supplies from –6 V to –2 V.

The ADM1060 also provides four general-purpose inputs (GPIs). These logic inputs (TTL or CMOS compatible) enable the user to apply control signals, such as POWER_OK, RESET or MANUAL RESET, that can control the sequence in which the supplies turn on. A watchdog timer is also included. This circuit is used to ensure that a processor clock continues to toggle (transition from low to high or high to low).

At the logical core of the device is the programmable logic block array (PLBA) and the programmable delay block (PDB). These blocks enable the ADM1060 to sequence the turn-on of the supplies with a programmable time delay between each of them.

The outputs of the device (programmable driver outputs- PDOs) can be used as logic control signals to enable the output of LDOs or simply as a status output signal such as POWER_GOOD. PDOs 1 to 4 can also provide a high voltage output for driving the gate of a NMOS FET that may be placed in to supply path.

Communication with the ADM1060 is via a standard 2-wire SMBus interface. The user can set up the features described above via software (which is provided, or alternatively, can be written by users themselves). Once satisfied with the configuration, the user can store this in non-volatile memory, so that each time the device is subsequently powered up, the same configuration is downloaded and set up in the device.

Using the same five supplies as in the discrete design above, a hardware implementation using one ADM1060 is shown in figure 3.

A very powerful feature of the ADM1060, which cannot be easily replicated in a discrete design, is ability to configure a controlled power-down sequence. Again, using the software provided, a sequence such as that shown in the diagram below can be configured. The turn-on and turn-off sequencing is shown in figure 4.

In conclusion, then, the requirement for multiple voltages on a single PCB has resulted in a difficult supply-sequencing problem for power designers. With six, seven or more voltages required, discrete solutions are unwieldy and impractical. Analog Devices' ADM1060 provides a powerful and flexible alternative, making the configuration of supply thresholds, logic inputs and supply sequencing a simple software experience.

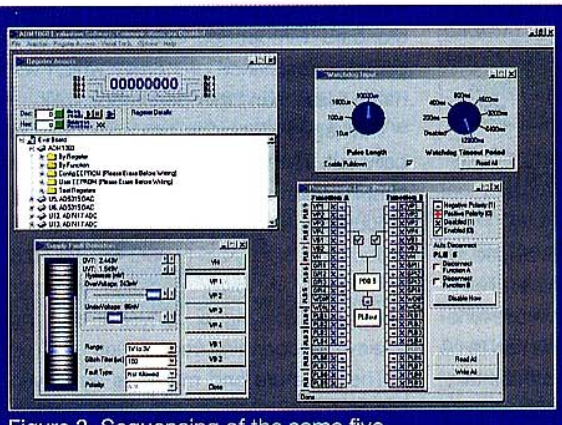

Figure 3. Sequencing of the same five supplies using one ADM1060

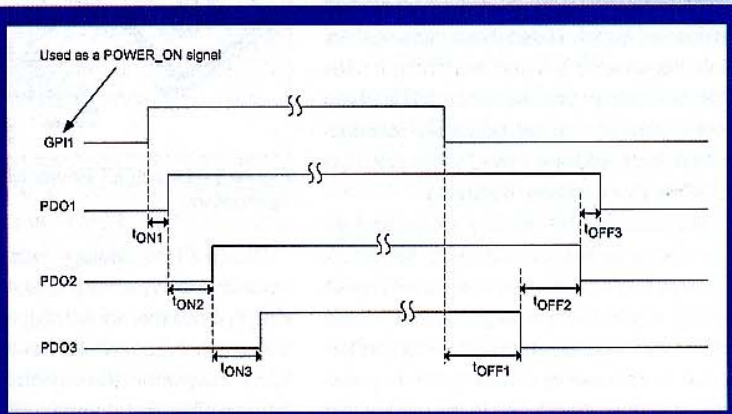

Figure 4.Controlled Power On/Off sequence using the ADM1060