AN-721
APPLICATION NOTE

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ADM1068/ADM1069/ADM1168/ADM1169 Configuration Registers

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INTRODUCTION

The ADM1068/ADM1069/ADM1168/ADM1169 family of fully programmable supply sequencers and supervisors can be used as complete supply management solutions in systems using multiple voltage supplies. Such applications include line cards in telecommunications infrastructure equipment (central office, base stations) and blade cards in servers.

All features of the ADM1068/ADM1069/ADM1168/ADM1169 are programmable through an SMBus interface. The devices also contain nonvolatile memory (EEPROM), allowing the configuration of these features to be stored on-chip and downloaded on each power-up.

This application note briefly outlines the functions of the devices and provides details of the registers required to set up device configuration.

For more information on the features and functions of the ADM1068/ADM1069/ADM1168/ADM1169, see the relevant data sheets.

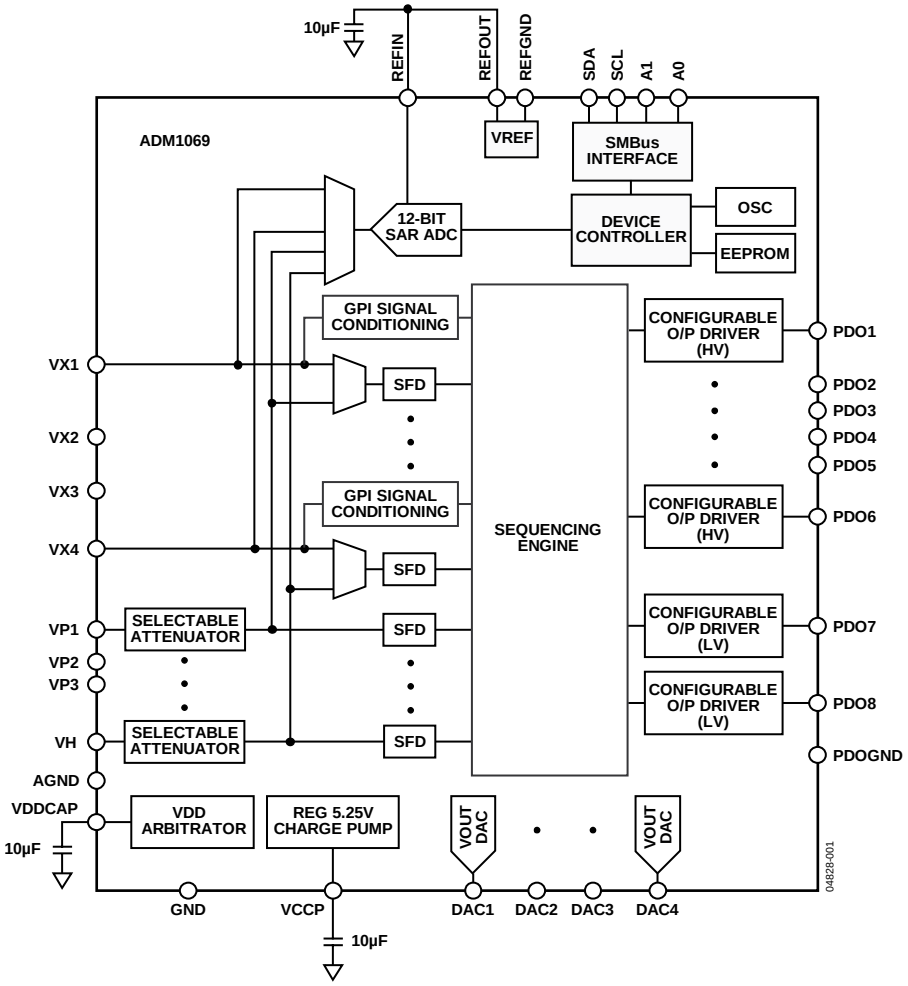

Figure 1. ADM1069 Functional Block Diagram

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REVISION HISTORY

8/13—Rev. A to Rev. B

Change to PDO Pull-Up Column of Table 3 15
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12/10—Rev. 0 to Rev. A

Added ADM1168 and ADM1169 ..... Throughout
Changes to Introduction 1
Deleted Figure 2, Figure 4, Figure 5, and Figure 7 to Figure 10, Renumbered Subsequent Figures ..... Throughout
Separated Table 6 into Table 6 and Table 7, Renumbered Subsequent Tables 20
Added Table 9 to Table 11 21
Separated Table 12 into Table 12 to Table 21 24
Added the Black Box Status Registers and Fault Records on the ADM1168/ADM1169 Section 31
Added the Use of the REVID Register Section 31

2/06—Revision 0: Initial Version

UPDATING MEMORY, ENABLING BLOCK ERASE, AND DOWNLOADING EEPROM

The configuration registers of the ADM1068/ADM1069/ ADM1168/ADM1169 can be updated over the SMBus interface. The devices must be explicitly set up to allow updates to the configuration registers to occur. The details of how to configure the devices are included in Table 1.

The devices contain both volatile and nonvolatile memory, which must be accessed correctly if any alterations to the configuration are to be updated properly in the devices. The volatile memory of the devices is constructed with double buffered latches. For information on this construction, see the relevant device data sheet. Note that none of the ADC readback functions on the ADM1069/ADM1169 are double buffered.

The register/bit map detail in Table 1 shows the bits required to

- Update volatile memory in real time.
- Update volatile memory offline, then update all at once.
- Enable block erase.
- Download EEPROM contents to RAM.

There are 1024 bytes of EEPROM on the ADM1068/ADM1069/ ADM1168/ADM1169. The EEPROM is assigned as follows:

- 256 bytes for device configuration
- 256 bytes for use as a scratchpad area (for example, a board revision number)
- 512 bytes for the sequencing engine configuration

The 256 bytes of device configuration EEPROM are grouped in eight pages of 32 bytes each. These bytes are located at Register 0xF800 to Register 0xF8FF.

For the first five pages, there is a direct one-to-one match between the EEPROM registers and the volatile RAM registers described in this data sheet. For example, if the overvoltage threshold for VP1 resides in RAM at Register 0x00, it is stored in EEPROM at Register 0xF800.

The other three pages are reserved for factory calibration of the device. These cannot be accessed by the user. An attempt to read/write to Register 0xF8A0 through Register 0xF8FF results in a NACK (no acknowledge) from the ADM1068/ADM1069/ ADM1168/ADM1169.

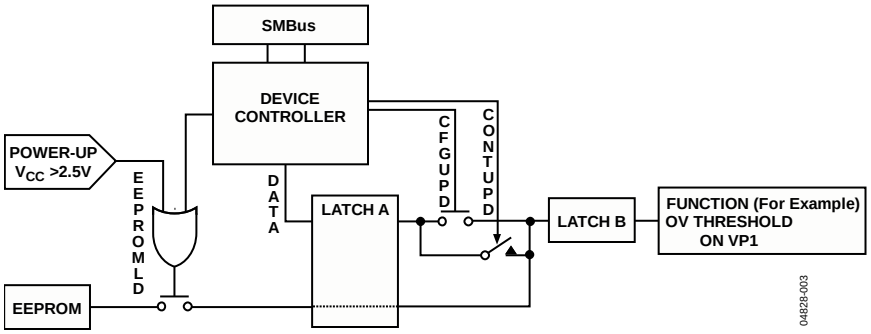

Figure 2. Configuration Update Flow Diagram

Table 1.

Reg.	Reg. Name	Bit No.	Mnemonic	R/W	Description
0x90	UPDCFG	7:3	N/A		Cannot be used.
		2	EEBLKERS	R/W	Enable configuration EEPROM block erase.
		1	CFGUPD	W	Update configuration registers from holding registers (self-clears).
		0	CONTUPD	R/W	Enable continuous update of configuration registers.
0xD8	UDOWNLD	7:1	N/A		Cannot be used.
		0	EEDWNLD	W	Download configuration data from EEPROM. This also happens automatically at power-up. Self-clears on completion.
0xF4	MANID	7:0	MANID	R	Manufacturer's ID, returns 0x41. Can be used to verify communication with the device.

INPUTS

The ADM1068/ADM1069/ADM1168/ADM1169 devices have eight inputs. Four of these are dedicated supply fault detectors, highly programmable reset generators whose inputs can detect overvoltage, undervoltage, or out-of-window faults. With these four inputs, voltages from 0.573 V to 14.4 V can be supervised. The undervoltage and overvoltage thresholds can be programmed to an 8-bit resolution. The comparators used to detect faults on the inputs have digitally programmable hysteresis to provide immunity to supply bounce. Each of these inputs also has a glitch filter whose timeout is programmable up to 100 µs.

The other four inputs have dual functionality. They can be used as analog inputs or as general-purpose logic inputs. As analog inputs, these channels function the same as those described earlier in this section. The major difference is that these inputs do not have internal attenuation resistors and present a true high impedance to the input pin. Their input range is, therefore, limited to 0.573 V to 1.375 V, but the high impedance means that an external resistor divide network can be used to divide down any out-of-range supply to a value within range. Therefore, +48 V, +24 V, −5 V, and −12 V can all be supervised by these channels with the appropriate external resistor network.

As digital inputs, these pins can be used to detect enable signals (such as PWRGD and POWRON) and are TTL and CMOS compatible. When used in this mode, the analog circuitry of these pins can be mapped to one of the dedicated analog input pins (VP1 to VP3 and VH). Therefore, VX1 can be used as a second detector on VP1, VX2 can be used with VP2, VX3 can be used with VP3, and VX4 can be used with VH. With a second detector available, the user can program alarm as well as fault functions.

If the digital inputs are left floating, the ADM1068/ADM1069/ADM1168/ADM1169 provide an internal current sink on each pin so that it can be pulled to GND and, therefore, be a known condition.

Table 2 details all of the registers used to configure the inputs to perform the functions described in this section.

Table 2. Registers Used to Configure Inputs

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description			
VP1	0x08	PS1OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VP1.			
	0x09	PS1OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS1OVTH when OV is true.			
	0x0A	PS1UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VP1.			
	0x0B	PS1UVHYST	7:5			Cannot be used.			
			4:0			5-bit hysteresis to be added from PS1UVTH when UV is true.			
	0x0C	SFDV1CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	FLT1 to FLT0	R/W	**FLT1**	**FLT0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x0D	SFDV1SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Select**	
						0	0	Midrange (2.5 V to 6 V)	
						0	1	Low range (1.25 V to 3 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	
VP2	0x10	PS2OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VP2.			
	0x11	PS2OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS2OVTH when OV is true.			
	0x12	PS2UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VP2.			
	0x13	PS2UVHYST	7:5			Cannot be used.			
			4:0			5-bit hysteresis to be added from PS2UVTH when UV is true.			
	0x14	SFDV2CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	FLT1 to FLT0	R/W	**FLT1**	**FLT0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
	0x15	SFDV2SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Range Select**: 0 0 Midrange (2.5 V to 6 V); 0 1 Low range (1.25 V to 3 V); 1 0 Ultralow range (0.573 V to 1.375 V); 1 1 Ultralow range (0.573 V to 1.375 V)
VP3	0x18	PS3OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VP3.
	0x19	PS3OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS3OVTH when OV is true.
	0x1A	PS3UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VP3.
	0x1B	PS3UVHYST	7:5			Cannot be used.
			4:0			5-bit hysteresis to be added from PS3UVTH when UV is true.
	0x1C	SFDV3CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)**: 0 0 0 0; 0 0 1 5; 0 1 0 10; 0 1 1 20; 1 0 0 30; 1 0 1 50; 1 1 0 75; 1 1 1 100
			1:0	FLT1 to FLT0	R/W	**FLT1** / **FLT0** / **Fault Type Select**: 0 0 OV; 0 1 UV or OV; 1 0 UV; 1 1 Off
	0x1D	SFDV3SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Range Select**: 0 0 Midrange (2.5 V to 6 V); 0 1 Low range (1.25 V to 3V); 1 0 Ultralow range (0.573 V to 1.375 V); 1 1 Ultralow range (0.573 V to 1.375 V)
VH	0x20	PSVHOVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VH.
	0x21	PSVHOVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PSVHOVTH when OV is true.
	0x22	PSVHUVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VH.
	0x23	PSVHUVHYST	7:5			Cannot be used.
			4:0			5-bit hysteresis to be added from PSVHUVTH when UV is true.
	0x24	SFDVHCFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)**: 0 0 0 0; 0 0 1 5; 0 1 0 10; 0 1 1 20; 1 0 0 30; 1 0 1 50; 1 1 0 75; 1 1 1 100

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			1:0	FLT1 to FLT0	R/W	**FLT1** / **FLT0** / **Fault Type Select**: 0 0 OV; 0 1 UV or OV; 1 0 UV; 1 1 Off
	0x25	SFDVHSEL	7:1			Cannot be used.
			0	SEL0	R/W	**SEL0** / **Range Select**: 0 High range (6.0 V to 14.4 V); 1 Medium range (2.5 V to 6.0 V)
VX1	0x30	X1OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VX1.
	0x31	X1OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X1OVTH when OV is true.
	0x32	X1UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VX1.
	0x33	X1UVHYST	7:5			Cannot be used.
			4:0			5-bit hysteresis to be added from X1UVTH when UV is true.
	0x34	SFDX1CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)**: 0 0 0 0; 0 0 1 5; 0 1 0 10; 0 1 1 20; 1 0 0 30; 1 0 1 50; 1 1 0 75; 1 1 1 100
			1:0	FLT1 to FLT0	R/W	**FLT1** / **FLT0** / **Fault Type Select**: 0 0 OV; 0 1 UV or OV; 1 0 UV; 1 1 Off
	0x35	SFDX1SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Select**: 0 0 SFD (fault) only; 0 1 GPI (fault) only; 1 0 GPI (fault) + Second VP1 SFD (warning); 1 1 No function (input can still be used as ADC input)
	0x36	XGPI1CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin. **INTYP** / **Level/Edge**: 0 Detect level; 1 Detect edge
			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge is detected on input. **PULS1** / **PULS0** / **Pulse Length (µs)**: 0 0 10; 0 1 100; 1 0 1000; 1 1 10,000

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			2:0	GF2 to GF0	R/W	Glitch filter—length of time for which a pulse is ignored.

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
VX2	0x38	X2OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VX2.
	0x39	X2OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X2OVTH when OV is true.
	0x3A	X2UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VX2.
	0x3B	X2UVHYST	7:5			Cannot be used.
			4:0			5-bit hysteresis to be added from X2UVTH when UV is true.
	0x3C	SFDX2CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

			1:0	FLT1 to FLT0	R/W	

FLT1	FLT0	Fault Type Select
0	0	OV
0	1	UV or OV
1	0	UV
1	1	Off

	0x3D	SFDX2SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	

SEL1	SEL0	Function Select
0	0	SFD (fault) only
0	1	GPI (fault) only
1	0	GPI (fault) + second VP2 SFD (warning)
1	1	No function (input can still be used as ADC input)

	0x3E	XGPI2CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.

INTYP	Level/Edge
0	Detect level
1	Detect edge

			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge is detected on input.

PULS1	PULS0	Pulse Length (µs)
0	0	10
0	1	100
1	0	1000
1	1	10,000

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			2:0	GF2 to GF0	R/W	Glitch filter—length of time for which a pulse is ignored.

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
VX3	0x40	X3OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VX3.
	0x41	X3OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X3OVTH when OV is true.
	0x42	X3UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VX3.
	0x43	X3UVHYST	7:5			Cannot be used.
			4:0			5-bit hysteresis to be added from X3UVTH when UV is true.
	0x44	SFDX3CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			1:0	FLT1 to FLT0	R/W	

FLT1	FLT0	Fault Type Select
0	0	OV
0	1	UV or OV
1	0	UV
1	1	Off

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
	0x45	SFDX3SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	

SEL1	SEL0	Function Select
0	0	SFD (fault) only
0	1	GPI (fault) only
1	0	GPI (fault) + Second VP3 SFD (warning)
1	1	No function (input can still be used as ADC input)

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
	0x46	XGPI3CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.

INTYP	Level/Edge
0	Detect level
1	Detect edge

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge is detected on input.

PULS1	PULS0	Pulse Length (µs)
0	0	10
0	1	100
1	0	1000
1	1	10,000

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			2:0	GF2 to GF0	R/W	Glitch filter—length of time for which a pulse is ignored.

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
VX4	0x48	X4OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for OV threshold on VX4
	0x49	X4OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X4OVTH when OV is true.
	0x4A	X4UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for UV threshold on VX4.
	0x4B	X4UVHYST	7:5			Cannot be used.
			4:0			5-bit hysteresis to be added from X4UVTH when UV is true.
	0x4C	SFDX4CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

			1:0	FLT1 to FLT0	R/W	

FLT1	FLT0	Fault Type Select
0	0	OV
0	1	UV or OV
1	0	UV
1	1	Off

	0x4D	SFDX4SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	

SEL1	SEL0	Function Select
0	0	SFD (fault) only
0	1	GPI (fault) only
1	0	GPI (fault) + Second VH SFD (warning)
1	1	No function (input can still be used as ADC input)

	0x4E	XGPI4CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.

INTYP	Level/Edge
0	Detect level
1	Detect edge

			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge is detected on input.

PULS1	PULS0	Pulse Length (µs)
0	0	10
0	1	100
1	0	1000
1	1	10,000

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			2:0	GF2 to GF0	R/W	Glitch filter—length of time for which a pulse is ignored.

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

Input	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
VX1 to VX4, A0, A1	0x91	PDEN1	7			Cannot be used.
			6	A1PDOWN	R/W	1 = enable 20 µA pull-down on A1.
			5	A0PDOWN	R/W	1 = enable 20 µA pull-down on A0.
			4	VX4PDOWN	R/W	1 = enable 20 µA pull-down on VX4.
			3	VX3PDOWN	R/W	1 = enable 20 µA pull-down on VX3.
			2	VX2PDOWN	R/W	1 = enable 20 µA pull-down on VX2.
			1	VX1PDOWN	R/W	1 = enable 20 µA pull-down on VX1.
			0			Cannot be used.

OUTPUTS

The ADM1068/ADM1069/ADM1168/ADM1169 devices have eight programmable driver outputs (PDOs). Supply sequencing is achieved with the devices by using the PDOs as control signals for supplies. The output drivers can be used either as logic enables or as FET drivers.

The PDOs can be used for a number of functions; the primary function is to provide enable signals for LDOs or dc-to-dc converters, which generate supplies locally on a board. The PDOs can also be used to provide a POWER_GOOD signal when the inputs are in tolerance or to provide a reset output if one of the inputs goes out of spec (this can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOs can be programmed to pull up to a number of different options. The outputs can be programmed as

- Open drain (allowing the user to connect an external pull-up resistor)
- Weak pull-up to V_{DDCAP}
- Strong pull-up to V_{DDCAP}
- Weak pull-up to VPx
- Strong pull-up to VPx
- Strong pull-down to GND
- Internally charge-pumped high drive (12 V, PDO1 to PDO6)

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external N-FET, which is used to isolate, for example, a card-side voltage from a backplane supply (a PDO sustains greater than 10.5 V into a 1 μA load). The pull-down switches can be used to drive status LEDs.

The data driving each of the PDOs can come from one of three sources. The source can be enabled in the PDOCFG configuration register. The data sources are

- An output from the sequence engine (SE). This is how the devices normally operate with the ADM1068/ADM1069/ADM1168/ADM1169 controlling the outputs.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This enables software control of the PDOs. Thus, a microcontroller can be used to initiate a software power-up/power-down sequence.
- An on-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOs. It can be used to clock an external device such as an LED, for example.

Table 3 details all of the registers used to configure the outputs to perform the functions described in this section.

Table 3. Registers Used to Configure Outputs

Output	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description				
PDO1	0x07	PDO1CFG	7			Cannot be used.				
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.				
						CFG6	**CFG5**	**CFG4**	**PDO Status**	
						0	0	0	Disabled with weak pull-down	
						0	0	1	Enabled, follows the logic driven by the SE	
						0	1	0	Enables SMBus data, drive low	
						0	1	1	Enables SMBus data, drive high	
						1	X	X	Enables 100 kHz clock out onto pin	
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.				
						CFG3	**CFG2**	**CFG1**	**CFG0**	**PDO Pull-Up**
						0	0	0	X	None
						0	0	1	X	Pull-up to 12 V charge pump voltage
						0	1	1	0	Weak pull-up to VP1
						0	1	1	1	Strong pull-up to VP1
						1	0	0	0	Weak pull-up to VP2
						1	0	0	1	Strong pull-up to VP2
						1	0	1	0	Weak pull-up to VP3
						1	0	1	1	Strong pull-up to VP3
						1	1	1	0	Weak pull-up to V_{DDCAP}
						1	1	1	1	Strong pull-up to V_{DDCAP}
PDO2	0x0F	PDO2CFG	7			Cannot be used.				
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.				
						CFG6	**CFG5**	**CFG4**	**PDO Status**	
						0	0	0	Disabled with weak pull-down	
						0	0	1	Enabled, follows the logic driven by the SE	
						0	1	0	Enables SMBus data, drive low	
						0	1	1	Enables SMBus data, drive high	
						1	X	X	Enables 100 kHz clock out onto pin	
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.				
						CFG3	**CFG2**	**CFG1**	**CFG0**	**PDO Pull-Up**
						0	0	0	X	None
						0	0	1	X	Pull-up to 12 V charge pump voltage
						0	1	1	0	Weak pull-up to VP1
						0	1	1	1	Strong pull-up to VP1
						1	0	0	0	Weak pull-up to VP2
						1	0	0	1	Strong pull-up to VP2
						1	0	1	0	Weak pull-up to VP3
						1	0	1	1	Strong pull-up to VP3
						1	1	1	0	Weak pull-up to V_{DDCAP}
						1	1	1	1	Strong pull-up to V_{DDCAP}

Output	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
PDO3	0x17	PDO3CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	300 kΩ pull-up to 12 V charge pump voltage
0	1	1	0	Weak pull-up to VP1
0	1	1	1	Strong pull-up to VP1
1	0	0	0	Weak pull-up to VP2
1	0	0	1	Strong pull-up to VP2
1	0	1	0	Weak pull-up to VP3
1	0	1	1	Strong pull-up to VP3
1	1	1	0	Weak pull-up to V_{DDCAP}
1	1	1	1	Strong pull-up to V_{DDCAP}

PDO4	0x1F	PDO4CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	none
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	1	0	Weak pull-up to VP1
0	1	1	1	Strong pull-up to VP1
1	0	0	0	Weak pull-up to VP2
1	0	0	1	Strong pull-up to VP2
1	0	1	0	Weak pull-up to VP3
1	0	1	1	Strong pull-up to VP3
1	1	1	0	Weak pull-up to V_{DDCAP}
1	1	1	1	Strong pull-up to V_{DDCAP}

PDO5	0x27	PDO5CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

Output	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	1	0	Weak pull-up to VP1
0	1	1	1	Strong pull-up to VP1
1	0	0	0	Weak pull-up to VP2
1	0	0	1	Strong pull-up to VP2
1	0	1	0	Weak pull-up to VP3
1	0	1	1	Strong pull-up to VP3
1	1	1	0	Weak pull-up to V_{DDCAP}
1	1	1	1	Strong pull-up to V_{DDCAP}

Output	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
PDO6	0x2F	PDO6CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	1	0	Weak pull-up to VP1
0	1	1	1	Strong pull-up to VP1
1	0	0	0	Weak pull-up to VP2
1	0	0	1	Strong pull-up to VP2
1	0	1	0	Weak pull-up to VP3
1	0	1	1	Strong pull-up to VP3
1	1	1	0	Weak pull-up to V_{DDCAP}
1	1	1	1	Strong pull-up to V_{DDCAP}

Output	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description
PDO7	0x37	PDO7CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Do not use
0	1	1	0	Weak pull-up to VP1
0	1	1	1	Strong pull-up to VP1
1	0	0	0	Weak pull-up to VP2
1	0	0	1	Strong pull-up to VP2
1	0	1	0	Weak pull-up to VP3
1	0	1	1	Strong pull-up to VP3

Output	Reg. No.	Reg. Name	Bits	Bit Name	R/W	Description				
						1	1	1	0	Weak pull-up to V_{DDCAP}
						1	1	1	1	Strong pull-up to V_{DDCAP}
PDO8	0x3F	PDO8CFG	7			Cannot be used.				
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.				
						CFG6	**CFG5**	**CFG4**	**PDO Status**	
						0	0	0	Disabled with weak pull-down	
						0	0	1	Enabled, follows the logic driven by the SE	
						0	1	0	Enables SMBus data, drive low	
						0	1	1	Enables SMBus data, drive high	
						1	X	X	Enables 100 kHz clock out onto pin	
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.				
						CFG3	**CFG2**	**CFG1**	**CFG0**	**PDO Pull-Up**
						0	0	0	X	None
						0	0	1	X	Do not use
						0	1	1	0	Weak pull-up to VP1
						0	1	1	1	Strong pull-up to VP1
						1	0	0	0	Weak pull-up to VP2
						1	0	0	1	Strong pull-up to VP2
						1	0	1	0	Weak pull-up to VP3
						1	0	1	1	Strong pull-up to VP3
						1	1	1	0	Weak pull-up to V_{DDCAP}
						1	1	1	1	Strong pull-up to V_{DDCAP}

SEQUENCING ENGINE

The ADM1068/ADM1069/ADM1168/ADM1169 incorporate a sequencing engine (SE) that provides the user with powerful and flexible control of sequencing. The SE implements state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards, such as power-up and power-down sequence control, fault event handling, and interrupt generation on warnings. A watchdog function to verify the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing.

Considering the function of the SE from an applications viewpoint, it is best to think of the SE as providing a state for a state machine. This state has the following attributes:

- It is used to monitor signals indicating the status of the eight input pins, VP1 to VP3, VH, and VX1 to VX4.
- It can be entered from any other state.
- There are three exit routes that move the state machine to the next state: end-of-step detection, monitoring fault, and timeout.
- Delay timers for the end-of-step and timeout blocks can be programmed independently and change with each state change. The range of timeouts is from 0 ms to 400 ms.
- The output condition of the eight PDO pins is defined and fixed within a state.
- The transition from one state to the next is made in less than 10 µs, the time taken to download a state definition from EEPROM to the SE.

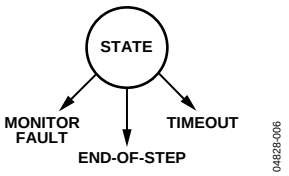

Figure 3. State Cell

The ADM1068/ADM1069/ADM1168/ADM1169 offer up to 63 such state definitions. Each state is defined by a 64-bit word.

Table 4 shows the details of the 64 bits that define a state. Table 8 details how to communicate with the SE. Table 9 provides details of additional sequence engine control registers present in the ADM1168/ADM1169 that allow the sequence engine to be restarted.

Table 4. Starting Address for Each State in SE

State	Start Address	State	Start Address
Reserved State	FA00	State 32	FB00
State 1	FA08	State 33	FB08
State 2	FA10	State 34	FB10
State 3	FA18	State 35	FB18
State 4	FA20	State 36	FB20
State 5	FA28	State 37	FB28
State 6	FA30	State 38	FB30
State 7	FA38	State 39	FB38
State 8	FA40	State 40	FB40
State 9	FA48	State 41	FB48
State 10	FA50	State 42	FB50
State 11	FA58	State 43	FB58
State 12	FA60	State 44	FB60
State 13	FA68	State 45	FB68
State 14	FA70	State 46	FB70
State 15	FA78	State 47	FB78
State 16	FA80	State 48	FB80
State 17	FA88	State 49	FB88
State 18	FA90	State 50	FB90
State 19	FA98	State 51	FB98
State 20	FAA0	State 52	FBA0
State 21	FAA8	State 53	FBA8
State 22	FAB0	State 54	FBB0
State 23	FAB8	State 55	FBB8
State 24	FAC0	State 56	FBC0
State 25	FAC8	State 57	FBC8
State 26	FAD0	State 58	FBD0
State 27	FAD8	State 59	FBD8
State 28	FAE0	State 60	FBE0
State 29	FAE8	State 61	FBE8
State 30	FAF0	State 62	FBF0
State 31	FAF8	State 63	FBF8

Table 5. Bitmap for Definition of Each State in SE

Reg. No.	Bit	SE Bit	If 0…	If 1…	Notes
0	0	0	Drive PDO1 low	Drive PDO1 high	
	1	1	Drive PDO2 low	Drive PDO2 high	
	2	2	Drive PDO3 low	Drive PDO3 high	
	3	3	Drive PDO4 low	Drive PDO4 high	
	4	4	Drive PDO5 low	Drive PDO5 high	
	5	5	Drive PDO6 low	Drive PDO6 high	
	6	6	Drive PDO7 low	Drive PDO7 high	
	7	7	Drive PDO8 low	Drive PDO8 high	
1	0	8			Reserved.
	1	9			Reserved.
	2	10			Reserved.
	3	11			Reserved.
	4	12	Exit state if VP1 = 0	Exit state if VP1 = 1	Monitor function: monitoring for faults on VP1 must be unmasked (next bit).
	5	13	Mask VP1 monitoring	Unmask VP1 monitoring	Bit 11 = 1; turns on the monitor function on VP1 channel.
	6	14	Exit state if VP2 = 0	Exit state if VP2 = 1	Monitor function: monitoring for faults on VP2 must be unmasked (next bit).
	7	15	Mask VP2 monitoring	Unmask VP2 monitoring	Bit 13 = 1; turns on the monitor function on VP2 channel.
2	0	16	Exit state if VP3 = 0	Exit state if VP3 = 1	Monitor function: monitoring for faults on VP3 must be unmasked (next bit).
	1	17	Mask VP3 monitoring	Unmask VP3 monitoring	Bit 15 = 1; turns on the monitor function on VP3 channel.
	2	18	Exit state if VH = 0	Exit S=state if VH = 1	Monitor function: monitoring for faults on VH must be unmasked (next bit).
	3	19	Mask VH monitoring	Unmask VH monitoring	Bit 19 = 1; turns on the monitor function on VH channel.
	4	20			Reserved.
	5	21			Reserved.
	6	22	Exit state if VX1 = 0	Exit state if VX1 = 1	Monitor function: monitoring for faults on VX1 must be unmasked (next bit).
	7	23	Mask VX1 monitoring	Unmask VX1 monitoring	Bit 23 = 1; turns on monitoring on VX1 channel.
3	0	24	Exit state if VX2 = 0	Exit state if VX2 = 1	Monitor function: monitoring for faults on VX2 must be unmasked (next bit).
	1	25	Mask VX2 monitoring	Unmask VX2 monitoring	Bit 25 = 1; turns on monitoring on VX2 channel.
	2	26	Exit state if VX3 = 0	Exit state if VX3 = 1	Monitor function: monitoring for faults on VX3 must be unmasked (next bit).
	3	27	Mask VX3 monitoring	Unmask VX3 monitoring	Bit 27 = 1; turns on monitoring on VX3 channel.
	4	28	Exit state if VX4 = 0	Exit state if VX4 = 1	Monitor function: monitoring for faults on VX4 must be unmasked (next bit).
	5	29	Mask VX4 monitoring	Unmask VX4 monitoring	Bit 29 = 1; turns on monitoring on VX4 channel.
	6	30	Mask WARNING monitoring	Unmask WARNING monitoring	Can only generate a monitor fault on WARNING = 1; therefore, no requirement for second bit to differentiate between WARNING = 0 and WARNING = 1.
	7	31	TIMEOUT<0>		Timeout length. See Table 6.
4	0	32	TIMEOUT<1>		
	1	33	TIMEOUT<2>		
	2	34	TIMEOUT<3>		
	3	35	SEQCOND<0>		Sequence condition. See Table 7.
	4	36	SEQCOND<1>		
	5	37	SEQCOND<2>		
	6	38	SEQCOND<3>		
	7	39	Sequence on selected input = high	Sequence on selected input = low	SEQSENSE

Reg. No.	Bit	SE Bit	If 0…	If 1…	Notes
5	0	40	SEQDELAY<0>		Sequence delay. See Table 6.
	1	41	SEQDELAY<1>		
	2	42	SEQDELAY<2>		
	3	43	SEQDELAY<3>		
	4	44	MONADDR<0>		MONADDR<5:0> is the state number (+1) to jump to if a monitor function fault occurs. For example, if MONADDR is set to 01000 (that is, 8), the SE jumps to State 8 (at Address FA40) if a monitor function fault occurs.
	5	45	MONADDR<1>		
	6	46	MONADDR<2>		
	7	47	MONADDR<3>		
6	0	48	MONADDR<4>		
	1	49	MONADDR<5>		
	2	50	TIMADDR<0>		TIMADDR<5:0> is the state number (+1) to jump to if a timeout fault occurs. For example, if TIMADDR is set to 01000 (that is, 8), the SE jumps to State 8 (at Address FA40) if a timeout function fault occurs.
	3	51	TIMADDR<1>		
	4	52	TIMADDR<2>		
	5	53	TIMADDR<3>		
	6	54	TIMADDR<4>		
	7	55	TIMADDR<5>		
7	0	56	SEQADDR<0>		SEQADDR<5:0> is the state number (+1) to jump to if a sequence state changes. For example, if SEQADDR is set to 01000 (that is, 8), the SE jumps to State 8 (at Address FA40) if a sequence state change occurs.
	1	57	SEQADDR<1>		
	2	58	SEQADDR<2>		
	3	59	SEQADDR<3>		
	4	60	SEQADDR<4>		
	5	61	SEQADDR<5>		
	6	62	Round-robin disable	Round-robin enable	This is OR'ed with RRCTRL.2.
	7	63	Fault latch closed	Fault latch open	

Table 6. Timeouts and Delays for Functions in the SE

TIMEOUT<3:0>, SEQDELAY<3:0>	Delay (ms)
0	Cannot be used
1	0.1
2	0.2
3	0.4
4	0.7
5	1
6	2
7	4
8	7
9	10
10	20
11	40
12	70
13	100
14	200
15	400

Table 7. SEQCOND and Sequence on Signal From in the SE[1]

SEQCOND<3:0>	Sequence On Signal From
0	Never sequence; set SEQSENSE = 0 always to ensure no sequence (Bit 39).
1	N/A.
2	VP1.
3	VP2.
4	VP3.
5	VH.
6	N/A.
7	VX1.
8	VX2.
9	VX3.
10	VX4.
11	WARNING.
12	SMBus jump. Wait for the SMBus command before jumping to the next state. Set SEQSENSE = 0 to ensure proper operation.

[1] N/A means not applicable.

Table 8. Communicating with the SE

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x93	SECTRL	7:3	N/A		Cannot be used.
		2	SMBus jump	W	Allows software control of SE state changes. Can force an unconditional jump to the next state. The bit can be set as the condition for an end-of-step change. This enables the user to clear external interrupts by moving forward a state change. The bit self-clears to 0 after the state change has occurred.
		1	SWSTEP	R/W	Step the SE forward to the next state. Use in conjunction with the halt bit to step through a sequence. Can be used as a tool for debugging sequences.
		0	Halt	R/W	Halt the SE. State changes do not happen. Must be set to allow read, erase, or write access to the SE EEPROM.
0xE9	SEADDR	7:6	N/A		Cannot be used.
		5:0	ADDR	R	SE current state used in conjunction with the halt bit (Address 0x93[0]).

Table 9. Additional ADM1168/ADM1169 Sequence Engine Control Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xDA	UNLOCKSE	7:0	Unlock Key	W	Writing 0x27 and then 0x10 to this register in consecutive writes unlocks the SEDOWNLD register so that it can be written to. To reset the lock, write 0x00 into the unlock key. Writing to SEDOWNLD does not reset the lock.
0xDB	SEDOWNLD	7:1	N/A		Cannot be used.
		0	Restart	W	1 causes the sequence engine to restart from the reserved state.

CONFIGURING SEQUENCE ENGINE STATES TO WRITE INTO THE BLACK BOX EEPROM ON THE ADM1168/ADM1169

The ADM1168/ADM1169 can use a section of EEPROM to store fault records when the sequence engine enters a user defined trigger state. These states are defined in EEPROM and downloaded to registers along with the other configuration data when the ADM1168/ADM1169 are being initialized. The register locations of the black box write triggers are shown in Table 10. These are loaded from the same locations in the 0xF8xx EEPROM block. The BBWRTRGx registers are read/write and, therefore, can be modified by software if required after the download.

When one or more of the bits in the BBWRTRx registers are set to 1, the black box is enabled, and fault records are written into EEPROM when the sequence engine enters a state that has its corresponding BBWRTRGx bit set to 1.

When the black box is enabled, all access to the configuration, user, and black box EEPROM sections is inhibited unless the BBCTRL.HALT bit is written to 1 to stop the black box.

When an ADM1168/ADM1169 powers up, the black box automatically searches the black box section of EEPROM to find the first unused location for the next fault record to be written. After this section of EEPROM is erased, the black box may be instructed to perform this search again so that it uses the correct location for the next fault record write. The BBSEARCH.RESET bit is used to initiate this action.

Table 10. ADM1168/ADM1169 Bitmap for Definition of Black Box Write Triggers for Each SE State[1]

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x94	BBWRTRG1	7	STATE7	R/W	State 7 write trigger.
		6	STATE6	R/W	State 6 write trigger.
		5	STATE5	R/W	State 5 write trigger.
		4	STATE4	R/W	State 4 write trigger.
		3	STATE3	R/W	State 3 write trigger.
		2	STATE2	R/W	State 2 write trigger.
		1	STATE1	R/W	State 1 write trigger.
		0	Reserved	R/W	Reserved state black box trigger; must always be set to 0.
0x95	BBWRTRG2	7	STATE15	R/W	State 15 write trigger.
		6	STATE14	R/W	State 14 write trigger.
		5	STATE13	R/W	State 13 write trigger.
		4	STATE12	R/W	State 12 write trigger.
		3	STATE11	R/W	State 11 write trigger.
		2	STATE10	R/W	State 10 write trigger.
		1	STATE9	R/W	State 9 write trigger.
		0	STATE8	R/W	State 8 write trigger.
0x96	BBWRTRG3	7	STATE23	R/W	State 23 write trigger.
		6	STATE22	R/W	State 22 write trigger.
		5	STATE21	R/W	State 21 write trigger.
		4	STATE20	R/W	State 20 write trigger.
		3	STATE19	R/W	State 19 write trigger.
		2	STATE18	R/W	State 18 write trigger.
		1	STATE17	R/W	State 17 write trigger.
		0	STATE16	R/W	State 16 write trigger.
0x97	BBWRTRG4	7	STATE31	R/W	State 31 write trigger.
		6	STATE30	R/W	State 30 write trigger.
		5	STATE29	R/W	State 29 write trigger.
		4	STATE28	R/W	State 28 write trigger.
		3	STATE27	R/W	State 27 write trigger.
		2	STATE26	R/W	State 26 write trigger.
		1	STATE25	R/W	State 25 write trigger.
		0	STATE24	R/W	State 24 write trigger.
0x98	BBWRTRG5	7	STATE39	R/W	State 39 write trigger.
		6	STATE38	R/W	State 38 write trigger.
		5	STATE37	R/W	State 37 write trigger.
		4	STATE36	R/W	State 36 write trigger.
		3	STATE35	R/W	State 35 write trigger.

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
		2	STATE34	R/W	State 34 write trigger.
		1	STATE33	R/W	State 33 write trigger.
		0	STATE32	R/W	State 32 write trigger.
0x99	BBWRTRG6	7	STATE47	R/W	State 47 write trigger.
		6	STATE46	R/W	State 46 write trigger.
		5	STATE45	R/W	State 45 write trigger.
		4	STATE44	R/W	State 44 write trigger.
		3	STATE43	R/W	State 43 write trigger.
		2	STATE42	R/W	State 42 write trigger.
		1	STATE41	R/W	State 41 write trigger.
		0	STATE40	R/W	State 40 write trigger.
0x9A	BBWRTRG7	7	STATE55	R/W	State 55 write trigger.
		6	STATE54	R/W	State 54 write trigger.
		5	STATE53	R/W	State 53 write trigger.
		4	STATE52	R/W	State 52 write trigger.
		3	STATE51	R/W	State 51 write trigger.
		2	STATE50	R/W	State 50 write trigger.
		1	STATE49	R/W	State 49 write trigger.
		0	STATE48	R/W	State 48 write trigger.
0x9B	BBWRTRG8	7	STATE63	R/W	State 63 write trigger.
		6	STATE62	R/W	State 62 write trigger.
		5	STATE61	R/W	State 61 write trigger.
		4	STATE60	R/W	State 60 write trigger.
		3	STATE59	R/W	State 59 write trigger.
		2	STATE58	R/W	State 58 write trigger.
		1	STATE57	R/W	State 57 write trigger.
		0	STATE56	R/W	State 56 write trigger.

[1] When the trigger bit for a given state is set to 1, a fault record is written into the next free location in the black box section of EEPROM when the sequence engine enters that state. When the trigger bit is set to 0, no fault record is written.

Table 11. ADM1168/ADM1169 Black Box Control Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x9C	BBCTRL	7:1	N/A		Cannot be used.
		0	Halt	R/W	The black box function is enabled when one or more of the BBWRTRGx register bits are set to 1. When the black box is enabled, it is no longer possible to read or write to the configuration, user, and black box sections of EEPROM. Writing this bit to 1 disables the black box and enables read and write access to the configuration, user, and black box sections of EEPROM. This bit cannot be set while a fault record is being written into the EEPROM; therefore, this bit should always be read after a write to ensure that the bit is set correctly.
0XD9	BBSEARCH	7:1	N/A		Cannot be used.
		0	Reset	R	When written to 1, the black box searches from Address 0xF980 to find the first unused fault record. After erasing the section of EEPROM holding the black box fault records, and for the black box to start writing records from the first location, this bit should be written to 1.

ADM1069/ADM1169 ADC

The ADM1069/ADM1169 feature an on-chip 12-bit ADC. The ADC has a 8-channel analog mux on the front end. Any or all inputs can be selected to be read by the ADC. The ADC can then be set up to continuously read the selected channels. The circuit controlling this operation is called the round robin (RR). The user selects the channels to operate on, and the ADC performs a conversion on each in turn. Averaging can be turned on, setting the round robin to take 16 conversions on each channel; otherwise, a single conversion is made on each channel. At the end of this cycle, the results are written to the output registers. The ADM1069/ADM1169 also feature limit registers, one per ADC channel. These registers can be programmed to a threshold against which the ADC readings are compared. Because only one register is provided for each input channel, a UV or OV threshold, but not both, can be set for a given channel.

Exceeding the threshold generates a warning that can be fed as an input to the SE. Therefore, an out-of-range ADC reading can be used to generate an interrupt on one of the PDOs. This is described in more detail in the Warnings section.

The round robin can be enabled via an SMBus write, or it can be programmed to turn on at a particular state in the SE program by enabling the RR bit. For example, it can be set to start after a power-up sequence is complete and all supplies are known to be within expected fault limits.

Table 12 through Table 16 show the details of the registers required to set up the ADC and its inputs.

ADC Readback Configuration Registers

Table 12. Limit Registers—An ADC Reading Above or Below This Limit Generates a Warning

Reg. No.	Input	Reg. Name	Bits	Bit Name	R/W	Description
0x71	VP1	ADCVP1LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP1 input.
0x72	VP2	ADCVP2LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP2 input.
0x73	VP3	ADCVP3LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP3 input.
0x74	VH	ADCVHLIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VH input.
0x76	VX1	ADCVX1LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX1 input.
0x77	VX2	ADCVX2LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX2 input.
0x78	VX3	ADCVX3LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX3 input.
0x79	VX4	ADCVX4LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX4 input.

Table 13. Sense Registers—Determine When a Warning Is Generated

Reg. No.	Input	Reg. Name	Bits	Bit Name	R/W	Description
0x7D	VX2	LSENSE1	7	SENS7	R/W	Limit sense for VX2 (0 = ADC > ADCVX2LIM gives warning, that is, overvoltage, 1 = ADC < ADCVX2LIM gives a warning, that is, undervoltage).
	VX1		6	SENS6	R/W	Limit sense for VX1 (0 = ADC > ADCVX1LIM gives warning, that is, overvoltage, 1 = ADC < ADCVX1LIM gives a warning, that is, undervoltage).
			5			Cannot be used.
	VH		4	SENS4	R/W	Limit sense for VH (0 = ADC > ADCVHLIM gives warning, that is, overvoltage, 1 = ADC < ADCVHLIM gives a warning, that is, undervoltage).
	VP3		3	SENS2	R/W	Limit sense for VP3 (0 = ADC > ADCVP3LIM gives warning, that is, overvoltage, 1 = ADC < ADCVP3LIM gives a warning, that is, undervoltage).
	VP2		2	SENS1	R/W	Limit sense for VP2 (0 = ADC > ADCVP2LIM gives warning, that is, overvoltage, 1 = ADC < ADCVP2LIM gives a warning, that is, undervoltage).
	VP1		1	SENS0	R/W	Limit sense for VP1 (0 = ADC > ADCVP1LIM gives warning, that is, overvoltage, 1 = ADC < ADCVP1LIM gives a warning, that is, undervoltage).
			0			Cannot be used.
0x7E		LSENSE2	7:2			Cannot be used.
	VX4		1	SENS0	R/W	Limit sense for VX4 (0 = ADC > ADCVX4LIM gives warning, that is, overvoltage, 1 = ADC < ADCVX4LIM gives a warning, that is, undervoltage).
	VX3		0	SENS0	R/W	Limit sense for VX3 (0 = ADC > ADCVX3LIM gives warning, that is, overvoltage, 1 = ADC < ADCVX3LIM gives a warning, that is, undervoltage).

Table 14. Round-Robin Select Registers—Determine Which Inputs Are Actually Read by the ADC as It Cycles

Reg. No.	Input	Reg. Name	Bits	Bit Name	R/W	Description
0x80	VX2	RRSEL1	7	VX2CHAN	R/W	0 => VX2 is included in RR. 1 => VX2 is excluded from RR.
	VX1		6	VX1CHAN	R/W	0 => VX1 is included in RR. 1 => VX1 is excluded from RR.
			5			Cannot be used.
	VH		4	VHCHAN	R/W	0 => VH is included in RR. 1 => VH is excluded from RR.
	VP3		3	VP3CHAN	R/W	0 => VP3 is included in RR. 1 => VP3 is excluded from RR.
	VP2		2	VP2CHAN	R/W	0 => VP2 is included in RR. 1 => VP2 is excluded from RR.
	VP1		1	VP1CHAN	R/W	0 => VP1 is included in RR. 1 => VP1 is excluded from RR.
			0			Cannot be used.
0x81		RRSEL2	7:2			Cannot be used.
	VX4		1	VX4CHAN	R/W	0 => VX4 is included in RR. 1 => VX4 is excluded from RR.
	VX3		0	VX3CHAN	R/W	0 => VX3 is included in RR. 1 => VX3 is excluded from RR.

Table 15. Round-Robin Control Register—Activates ADC Read; Determines Whether Averaging Is Used and Whether There Is a Continuous Read

Reg. No.	Input	Reg. Name	Bits	Bit Name	R/W	Description
0x82		RRCTRL	7:5			Cannot be used.
			4	CLEARLIM	R/W	Write this bit high to clear limit warnings. This bit then self-clears.
			3	STOPWRITE	R/W	This bit inhibits the RR from writing the results to the output registers. This must be set if the user is going to read back the two output registers for any channel using two byte reads. If the user does it using a block read, then it does not need to be set because the RR is inhibited from writing to the output registers when the SMBus interface is busy.
			2	AVERAGE	R/W	Turn on 16 times averaging.
			1	ENABLE	R/W	Turn on the RR for continuous operation.
			0	GO	R/W	Start the RR.

Table 16. ADC Value Registers

Reg. No.	Input	Reg. Name	Bits	Bit Name	R/W	Description
0xA2	VP1	ADCHVP1	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP1 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP1 when 0x82:2 (average) = 1.
0xA3		ADCLVP1	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP1 input.
0xA4	VP2	ADCHVP2	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP2 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP2 when 0x82:2 (average) = 1.
0xA5		ADCLVP2	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP2 input.
0xA6	VP3	ADCHVP3	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP3 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP3 when 0x82:2 (average) = 1.
0xA7		ADCLVP3	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP3 input.
0xA8	VH	ADCHVH	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VH when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VH when 0x82:2 (average) = 1.
0xA9		ADCLVH	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VH input.
0xAC	VX1	ADCHVX1	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX1 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX1 when 0x82:2 (average) = 1.
0xAD		ADCLVX1	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX1 input.
0xAE	VX2	ADCHVX2	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX2 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX2 when 0x82:2 (average) = 1.
0xAF		ADCLVX2	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX2 input.

Reg. No.	Input	Reg. Name	Bits	Bit Name	R/W	Description
0xB0	VX3	ADCHVX3	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX3 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX3 when 0x82:2 (average) = 1.
0xB1		ADCLVX3	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX3 input.
0xB2	VX4	ADCHVX4	7:4			Not used if 0x82:2 (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX4 when 0x82:2 (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX4 when 0x82:2 (average) = 1.
0xB3		ADCLVX4	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX4 input.

ADM1069/ADM1169 DACS

The ADM1069/ADM1169 feature four voltage output DACs. These DACs are primarily used to adjust the output voltage of a dc-to-dc converter by altering the current at its feedback node. With the on-board ADC, these DACs provide the tools for a closed-loop margining system. For more information on margining, see the relevant device data sheet.

Four DAC ranges are offered, and these are placed with midcode (Code 0x7F) at 0.6 V, 0.8 V, 1.0 V, and 1.25 V with an output swing of ±300 mV about these midcode voltages. These voltages are set to correspond to the most common LDO/dc-to-dc converter feedback voltages. The DACs have 8-bit resolution, but with the confined output range of 600 mV, this results ina voltage resolution of 600 mv/256 = 2.34 mV. Centering the DAC outputs on the four midcodes then provides the best use of the DAC resolution.

For most supplies, it is possible to select the DAC midcode voltage such that it is the same as the trim/feedback voltage of a converter so that dc-to-dc output is not modified. This allows the top half of the DAC range (300 mV) to margin up and the bottom half of the DAC range to margin down. The DAC output voltage is set by the code written to the DACx register. The voltage is linear with the unsigned binary number in this register.Code 0x7F is placed at the midcode voltage.The output voltage is given by

$$DACoutput = (DACx - 0x7F)/255 \times 0.6015 + V_{OFF}$$

where V_{OFF} is one of the four offset voltages.

Limit registers (called DPLIMx and DNLIMx) on the device offer the user some protection from firmware bugs that can cause catastrophic board problems by forcing supplies beyond their allowable output ranges. Essentially, the DAC code written into the DACx register is clipped so that the code used to set the DAC voltage is actually given by

DACCode
= DACx, DNLIMx ≤ DACx ≤ DPLIMx
= DNLIMx, DACx < DPLIMx
= DPLIMx, DACx > DPLIMx

The DAC output buffer is three-stated if DNLIMx > DPLIMx. The user can make it very difficult for the DAC output buffers to be turned on in normal system operation by programming the limit registers in this way (these are among the registers downloaded from EEPROM at startup).

Table 17 shows the detail of the registers required to set up the DACs.

Table 17. DAC Configuration Registers

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
DAC1	0x52	DACCTRL1	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC1.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC1.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5A	DAC1	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x62	DPLIM1	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC1 is set to a higher code, the DAC output limits to the contents of this register.
	0x6A	DNLIM1	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC1 is set to a lower code, the DAC output limits to the contents of this register. Note that, if DNLIM1 is set to be greater than DPLIM1, the DAC output is always disabled (this is a safety feature).
DAC2	0x53	DACCTRL2	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC2.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC2.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5B	DAC2	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x63	DPLIM2	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC2 is set to a higher code, the DAC output limits to the contents of this register.
	0x6B	DNLIM2	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC2 is set to a lower code, the DAC output limits to the contents of this register. Note that, if DNLIM2 is set to be greater than DPLIM2, the DAC output is always disabled (this is a safety feature).
DAC3	0x54	DACCTRL3	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC3.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC3.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5C	DAC3	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x64	DPLIM3	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC3 is set to a code higher than this, the DAC output limits to the contents of this register.
	0x6C	DNLIM3	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC3 is set to a code lower than this, the DAC output limits to the contents of this register. Note that, if DNLIM3 is set to be greater than DPLIM3, the DAC output is always disabled (this is a safety feature).

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
DAC4	0x55	DACCTRL4	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC4.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC4.
	0x5D	DAC4	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x65	DPLIM4	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC4 is set to a higher code, the DAC output limits to the contents of this register.
	0x6D	DNLIM4	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC4 is set to a lower code, the DAC output limits to the contents of this register. Note that, if DNLIM4 is set to be greater than DPLIM4, the DAC output is always disabled (this is a safety feature).

OFFSEL1	OFFSEL0	(Midcode) Output Voltage
0	0	1.25 V
0	1	1.0 V
1	0	0.8 V
1	1	0.6 V

WARNINGS, FAULTS, AND STATUS

WARNINGS

The ADM1068/ADM1069/ADM1168/ADM1169 feature a lower level of fault detection that can be used in conjunction with the fault detection provided on the inputs. These lower level fault reports are provided by the ADC limit registers and by the secondary SFDs on the VP1 to VP3 and VH inputs. (The secondary SFDs are available on these pins when VX1 to VX4 are used as digital inputs; see the Inputs section.)

WARNING is provided as a single input to the SE. It consists of a wide OR of the ADC limit registers and the secondary SFD outputs. Selecting WARNING as an input to the SE is shown in the Sequencing Engine section.

FAULT/STATUS REPORTING

If a fault occurs on one of the inputs being monitored by the ADM1068/ADM1069/ADM1168/ADM1169 (that is, a supply on one of the VXx/VPx/VH pins moves outside its threshold window or a logic level is deasserted, it is possible to identify on which input the fault occurred. This is done by reading back the fault plane over the SMBus.

The fault plane is simply two registers, FSTAT1 and FSTAT2, where each bit represents a function, for example, a VPx pin or VXx pin. By reading the contents of these registers and determining which bits are set to 1, the user can identify the inputs on which faults have occurred. A 1 is defined as a fault. The exception to this is when a VXx pin is used as a digital input. In this case, 1 is the true logic value of the input on the pin.

The fault data is reported to the fault plane only if explicitly enabled. This is done by setting the enable fault register write bit high in each individual state. To do this, set Bit 63 in the relevant state configuration to 1. If this bit is not set, a fault that occurs in this state does not appear in the fault plane.

To latch the data in the fault plane, the enable fault register write bit must be set to 0 in the next state that is entered. Only by setting this bit to 0 can the data be locked in the register. If a fault occurs on an input channel and then recovers while the enable fault register write bit is set to 1, the relevant bit in the fault register toggles from 0 to 1 and back to 0.

The ADM1068/ADM1169 also feature a number of status registers that can be read at any time to determine the status of the inputs. The contents of these registers can change at any time; that is, the data is not latched in these registers as is the case with FSTAT1 and FSTAT2. Table 18 shows the details of the fault and status registers.

Table 18. Fault and Status Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xE0	FSTAT1	7	FLT_VX2	R	Fault output from SFD on the VX2 pin if selected as an analog input or logic asserted on VX21 pin if selected as a digital input.
		6	FLT_VX1	R	Fault output from SFD on the VX1 pin if selected as an analog input or logic asserted on VX1 pin if selected as a digital input.
		5			Cannot be used.
		4	FLT_VH	R	Fault output from the VH SFD.
		3	FLT_VP3		Fault output from the VP3 SFD.
		2	FLT_VP2		Fault output from the VP2 SFD.
		1	FLT_VP1		Fault output from the VP1 SFD.
		0	N/A		Cannot be used.
0xE1	FSTAT2	7:2	N/A		Cannot be used.
		1	FLT_VX4	R	Fault output from SFD on the VX4 pin if selected as an analog input or logic asserted on VX4 pin if selected as a digital input.
		0	FLT_VX3	R	Fault output from SFD on the VX3 pin if selected as an analog input or logic asserted on VX3 pin if selected as a digital input.
0xE2	OVSTAT1	7	OV_VX2	R	OV threshold exceeded on VX2 (SFD) or VP2 (warning).
		6	OV_VX1	R	OV threshold exceeded on VX1 (SFD) or VP1 (warning).
		5	N/A		Cannot be used.
		4	OV_VH	R	OV threshold exceeded on the VH SFD.
		2	OV_VP3	R	OV threshold exceeded on the VP3 SFD.
		2	OV_VP2	R	OV threshold exceeded on the VP2 SFD.
		1	OV_VP1	R	OV threshold exceeded on the VP1 SFD.
		0	N/A		Cannot be used.
0xE3	OVSTAT2	7:2	N/A		Cannot be used.
		1	OV_VX4	R	OV threshold exceeded on VX4 (SFD) or VP4 (warning).
		0	OV_VX3	R	OV threshold exceeded on VX3 (SFD) or VP3 (warning).
0xE4	UVSTAT1	7	UV_VX2	R	UV threshold exceeded on VX2 (SFD) or VP2 (warning).
		6	UV_VX1	R	UV threshold exceeded on VX1 (SFD) or VP1 (warning).

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
		5			Cannot be used.
		4	UV_VH	R	UV threshold exceeded on the VH SFD.
		3	UV_VP3	R	UV threshold exceeded on the VP3 SFD.
		2	UV_VP2	R	UV threshold exceeded on the VP2 SFD.
		1	UV_VP1	R	UV threshold exceeded on the VP1 SFD.
		0	N/A		Cannot be used.
0xE5	UVSTAT2	7:2	N/A		Cannot be used.
		1	UV_VX4	R	UV threshold exceeded on VX4 (SFD) or VP4 (warning).
		0	UV_VX3	R	UV threshold exceeded on VX3 (SFD) or VP3 (warning).
0xE6	LIMSTAT1	7	LIM_VX2	R	1 = ADC limit set in ADCVX2LIM exceeded on VX2.
		6	LIM_VX1	R	1 = ADC limit set in ADCVX2LIM exceeded on VX2.
		5	N/A		Cannot be used.
		4	LIM_VH	R	1 = ADC limit set in ADCVX2LIM exceeded on VH.
		3	LIM_VP3	R	1 = ADC limit set in ADCVX2LIM exceeded on VP3.
		2	LIM_VP2	R	1 = ADC limit set in ADCVX2LIM exceeded on VP2.
		1	LIM_VP1	R	1 = ADC limit set in ADCVX2LIM exceeded on VP1
		0	N/A		Cannot be used.
0xE7	LIMSTAT2	7:2	N/A		Cannot be used.
		1	LIM_VX4	R	1 = ADC limit set in ADCVX2LIM exceeded on VX4.
		0	LIM_VX3	R	1 = ADC limit set in ADCVX2LIM exceeded on VX3.
0xE8	GPISTAT	7:5			Cannot be used.
		4	VX4_STAT	R	VX4 GPI input status (after signal conditioning).
		3	VX3_STAT	R	VX3 GPI input status (after signal conditioning).
		2	VX2_STAT	R	VX2 GPI input status (after signal conditioning).
		1	VX1_STAT	R	VX1 GPI input status (after signal conditioning).
		0	N/A		Cannot be used.

BLACK BOX STATUS REGISTERS AND FAULT RECORDS ON THE ADM1168/ADM1169

Each time the ADM1168/ADM1169 sequence engine changes state, the contents of UVSTATx, OVSTATx, LIMSTATx, and GPISTATx, along with some other pieces of information relating to the sequence engine state and the cause of the last state transition, are latched into seven black box status registers.

These registers provide a snapshot of the state of the inputs being monitored by the ADM1168/ADM1169, what the last state was, and what caused the last state change.

After the sequence engine changes state, if the new state it enters has its corresponding BBWRTRGx.STATEy bit set, the seven black box status registers are written sequentially into the next available location in the black box EEPROM section.

After the seven bytes are written, an eighth checksum byte is written to provide a method to check data integrity. This can be important if only a partial record is written because all the supplies powering the part have failed.

The order of the bytes in a fault record stored in EEPROM is as follows:

- PREVSTEXT
- PREVSEQST
- BBSTAT1
- BBSTAT2
- BBSTAT3
- BBSTAT4
- BBSTAT5
- CHECKSUM

The bytes are stored from lowest EEPROM address to highest; therefor, for the first fault record location in the black box EEPROM, PREVSTEXT would be stored at 0xF980 and CHECKSUM at 0xF987.

USE OF THE REVID REGISTER

The ADM1068 and ADM1168 and also the ADM1069 and ADM1169 each have the same I^2C addresses range. They all return the value of 0x41 when the MANID register is read. REVID is a read-only register that can be used to determine whether a device at a given address is an ADM1068/ADM1168 or an ADM1069/ADM1169. This is detailed in Table 20.

Table 19. ADM1168/ADM1169 Black Box Fault and Status Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xEA	PREVSTEXT	7	BBUSED		Always reads as 0. When this bit is written to the first byte of a fault record in EEPROM, it marks all eight bytes in use. When the black box is searching for the next free location to use, this bit is examined. If this bit is 0, then even if the previous fault record was only partially written to EEPROM, the eight bytes of the fault record are ignored.
		6	Reserved		Always reads as 0.
		5	SMBJUMP	R	Indicates that the previous state transition was due to an SMBJump being received.
		4	LIMWARN	R	Indicates that the previous state transition was due to one or more ADC warning limits being exceeded.
		3	SFDCMP	R	Indicates that the previous state transition was due to one or more supply fault detector limits being exceeded.
		2	Timeout	R	Indicates that the previous state transition was due to the timeout condition becoming true.
		1	Monitor	R	Indicates that the previous state transition was due to the monitor condition becoming true.
		0	Sequence	R	Indicates that the previous state transition was due to the sequence condition becoming true.
0xEB	PREVSEQST	7:6			Cannot be used.
		5:0	PREVADDR	R	State number of the state that was active immediately prior to the current state.
0xEC	BBSTAT1	7	UV_VX2	R	UV threshold exceeded on VX2 (SFD) or VP2 (warning).
		6	UV_VX1	R	UV threshold exceeded on VX1 (SFD) or VP1 (warning).
		5	N/A		Cannot be used.
		4	UV_VH	R	UV threshold exceeded on the VH SFD.
		3	UV_VP3	R	UV threshold exceeded on the VP3 SFD.
		2	UV_VP2	R	UV threshold exceeded on the VP2 SFD.
		1	UV_VP1	R	UV threshold exceeded on the VP1 SFD.
		0	N/A		Cannot be used.
0xED	BBSTAT2	7	N/A		Cannot be used.
		6	OV_VH	R	OV threshold exceeded on the VH SFD.
		5	OV_VP3	R	OV threshold exceeded on the VP3 SFD.
		4	OV_VP2	R	OV threshold exceeded on the VP2 SFD.
		3	OV_VP1	R	OV threshold exceeded on the VP1 SFD.
		2	N/A		Cannot be used.
		1	UV_VX4	R	UV threshold exceeded on VX4 (SFD) or VP4 (warning).
		0	UV_VX3	R	UV threshold exceeded on VX3 (SFD) or VP3 (warning).
0xEE	BBSTAT3	7	VX3_STAT	R	VX3 GPI input status (after signal conditioning).
		6	VX2_STAT	R	VX2 GPI input status (after signal conditioning).
		5	VX1_STAT	R	VX1 GPI input status (after signal conditioning).
		4	N/A		Cannot be used.
		3	OV_VX4	R	OV threshold exceeded on VX4 (SFD) or VP4 (warning).
		2	OV_VX3	R	OV threshold exceeded on VX34 (SFD) or VP3 (warning).
		1	OV_VX2	R	OV threshold exceeded on VX2 (SFD) or VP2 (warning).
		0	OV_VX1	R	OV threshold exceeded on VX1 (SFD) or VP1 (warning).
0xEF	BBSTAT4	7	VX1 CH	R	VX1 limit status – used with LSENSE1.
		6	N/A		Cannot be used.
		5	VH CH	R	VH limit status – used with LSENSE1.
		4	VP3 CH	R	VP34 limit status – used with LSENSE1.
		3	VP2 CH	R	VP2 limit status – used with LSENSE1.
		2	VP1 CH	R	VP1 limit status – used with LSENSE1.
		1	N/A		Cannot be used.
		0	VX4_STAT	R	VX4 GPI input status (after signal conditioning).

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x F0	BBSTAT5	7:3	N/A		Cannot be used.
		2	VX4 CH	R	VX4 limit status – used with LSENSE2.
		1	VX3 CH	R	VX3 limit status – used with LSENSE1.
		0	VX2 CH	R	VX2 limit status – used with LSENSE1.
0x F1	BBADDR	7:0	ADDR	R	Low byte of the address location in the 0xF980 to 0xF9FF range that the next fault record is written to. When no fault records have been written, the value is 0x80, and increments by 8 each time a fault record is written. The value is 0x F8 when there is only one fault record not written. When all locations have been written to, and the black box EEPROM is full, the value is 0x00.

Table 20. Decoding the REVID Register.

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xF5	REVID	7:4	Family	R	When the value 0x0 is read, the device is an ADM1068/ADM1069. When the value 0x1 is read, the device is an ADM1168/ADM1169.
		3:0	HWVER	R	This value is the hardware revision number.

Table 21. Register Map Quick Reference[1]

Base (Hex)	Function	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	Output
00	x	x	x	x	x	x	x	x	PDO1CFG	PDO1
08	VP1	PS1OVTH	PS1OVHYST	PS1UVTH	PS1UVHYST	SFDV1CFG	SFDV1SEL	x	PDO2CFG	PDO2
10	VP2	PS2OVTH	PS2OVHYST	PS2UVTH	PS2UVHYST	SFDV2CFG	SFDV2SEL	x	PDO3CFG	PDO3
18	VP3	PS3OVTH	PS3OVHYST	PS3UVTH	PS3UVHYST	SFDV3CFG	SFDV3SEL	x	PDO4CFG	PDO4
20	VH	PSVHOVTH	PSVHOVHYST	PSVHUVTH	PSVHUVHYST	SFDVHCFG	SFDVHSEL	x	PDO5CFG	PDO5
28	x	x	x	x	x	x	x	x	PDO6CFG	PDO6
30	VX1	X1OVTH	X1OVHYST	X1UVTH	X1UVHYST	SFDX1CFG	SFDX1SEL	XGPI1CFG	PDO7CFG	PDO7
38	VX2	X2OVTH	X2OVHYST	X2UVTH	X2UVHYST	SFDX2CFG	SFDX2SEL	XGPI2CFG	PDO8CFG	PDO8
40	VX3	X3OVTH	X3OVHYST	X3UVTH	X3UVHYST	SFDX3CFG	SFDX3SEL	XGPI3CFG	x	
48	VX4	X4OVTH	X4OVHYST	X4UVTH	X4UVHYST	SFDX4CFG	SFDX4SEL	XGPI4CFG	x	
50	DAC Control	x	x	DACCTRL1	DACCTRL2	DACCTRL3	DACCTRL4	x	x	
58	DAC Code	x	x	DAC1	DAC2	DAC3	DAC4	x	x	
60	DAC upper limit	x	x	DPLIM1	DPLIM2	DPLIM3	DPLIM4	x	x	
68	DAC lower limit	x	x	DNLIM1	DNLIM2	DNLIM3	DNLIM4	x	x	
70	ADCLIM		ADCVP1LIM	ADCVP2LIM	ADCVP3LIM	ADCVHLIM	x	ADCVX1LIM	ADCVX2LIM	
78	ADCLIM	ADCVX3LIM	ADCVX4LIM	x	x	x	LSENSE1	LSENSE2	x	
80	ADC setup	RRSEL1	RRSEL2	RRCTRL	x	x	x	x	x	
88	x	x	x	x	x	x	x	x	x	
90	Miscellaneous	UPDCFG	PDEN1	PDEN2	SECTRL	BBWRTRG1[2]	BBWRTRG2[2]	BBWRTRG3[2]	BBWRTRG4[2]	
98	Miscellaneous	BBWRTRG5[2]	BBWRTRG6[2]	BBWRTRG7[2]	BBWRTRG8[2]	BBCTRL[2]	x	x	x	
A0	ADC readback	x	x	ADCHVP1	ADCLVP1	ADCHVP2	ADCLVP2	ADCHVP3	ADCLVP3	
A8	ADC readback	ADCHVH	ADCLVH	x	x	ADCHVX1	ADCLVX1	ADCHVX2	ADCLVX2	
B0	ADC readback	ADCHVX3	ADCLVX3	ADCHVX4	ADCLVX4	x	x	x	x	
B8		x	x	x	x	x	x	x	x	
C0		x	x	x	x	x	x	x	x	
C8		x	x	x	x	x	x	x	x	
D0		x	x	x	x	x	x	x	x	
D8	Miscellaneous	UDOWNLD	BBSEARCH[2]	UNLOCKSE[2]	SEDOWNLD[2]	x	x	x	x	
E0	Fault (read-only)	FSTAT1	FSTAT2	OVSTAT1	OVSTAT2	UVSTAT1	UVSTAT2	LIMSTAT1	LIMSTAT2	
E8	Fault (read-only)	GPISTAT	SEADDR	PREVSTEXT[2]	PREVSEQST[2]	BBSTAT1[2]	BBSTAT2[2]	BBSTAT3[2]	BBSTAT4[2]	
F0	Miscellaneous	BBSTAT5[2]	BBADDR[2]	x	x	MANID	REVID1	MARK1	MARK2	
F8	Commands	EEALOW	EEAHIGH	EEBLOW	EEBHIGH	BLKWR	BLKRD	BLKER	x	

[1] x indicates that register locations do not exist.
[2] Available only on the ADM1168 and ADM1169.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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