ANALOG DEVICES

Hardware User Guide
UG-400

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

*ez*LINX *i*Coupler Isolated Interface Development Environment

FEATURES

Plug and play system evaluation
Easy evaluation of 8 isolated physical layer communication standards
Open source hardware
Open source software
***i*Coupler and *iso*Power technology**
ADSP-BF548 Blackfin processor running uClinux
Sample PC application
Sample embedded uClinux application
64 MB RAM
32 MB flash
Extender connector for additional functionality

APPLICATIONS

Isolated interfaces

EVALUATION KIT CONTENTS

EZLINX-IIIDE-EBZ
Power supply
***ez*LINX software DVD**
USB A to mini USB B cable

EZLINX-IIIDE-EBZ

10649-001

Figure 1.

GENERAL DESCRIPTION

The *ez*LINX™ *i*Coupler® isolated interface development environment provides developers with a cost-effective, plug and play method for evaluating eight digitally isolated physical layer communication standards (USB, RS-422, RS-485, RS-232, CAN, SPI, I^{2}C, and LVDS). The Blackfin® ADSP-BF548 processor runs the uClinux® operating system and allows for easy customization through the open source hardware and software platform. Development time is significantly reduced for embedded designers and system architects who are designing and evaluating isolated communication standards. The interfaces on *ez*LINX use Analog Devices, Inc., isolated transceivers with integrated *i*Coupler and *iso*Power® digital isolator technology.

The hardware of the ezLINX *i*Coupler isolated interface development environment contains the ADSP-BF548 Blackfin processor with 64 MB of RAM and 32 MB of flash memory. The isolated physical layer communication standards are implemented using Analog Devices isolated transceivers with integrated *i*Coupler and *iso*Power technology. Devices used to implement these isolated physical layer communication standards include the following:

- Isolated USB using the ADuM3160
- Isolated CAN using the ADM3053 signal and power isolated CAN transceiver
- Isolated RS-485 and RS-422 using the ADM2587E signal and power isolated RS-485/RS-422 transceiver
- Isolated RS-232 using the ADM3252E signal and power isolated RS-232 transceiver
- Isolated I^{2}C using the ADuM1250 and ADuM5000
- Isolated SPI using the ADuM3401, ADuM3402, and ADuM5000
- Isolated LVDS using the ADuM3442, ADuM5000, ADN4663, and ADN4664

This evaluation board contains multiple parts with *iso*Power technology, which uses high frequency switching elements to transfer power through the transformer. Special care must be taken during PCB layout to meet emissions standards. See the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for board layout recommendations. The ezLINX PCB layout has not been verified to pass radiated emissions specifications.

TABLE OF CONTENTS

REVISION HISTORY

8/12—Revision 0: Initial Version

SYSTEM ARCHITECTURE

The system architecture block diagram of the *ez*LINX hardware is shown in Figure 2. An extender connector, Hirose FX8-120P-SV(91), is added for additional functionality. The Ethernet option is not fitted on the standard *ez*LINX hardware.

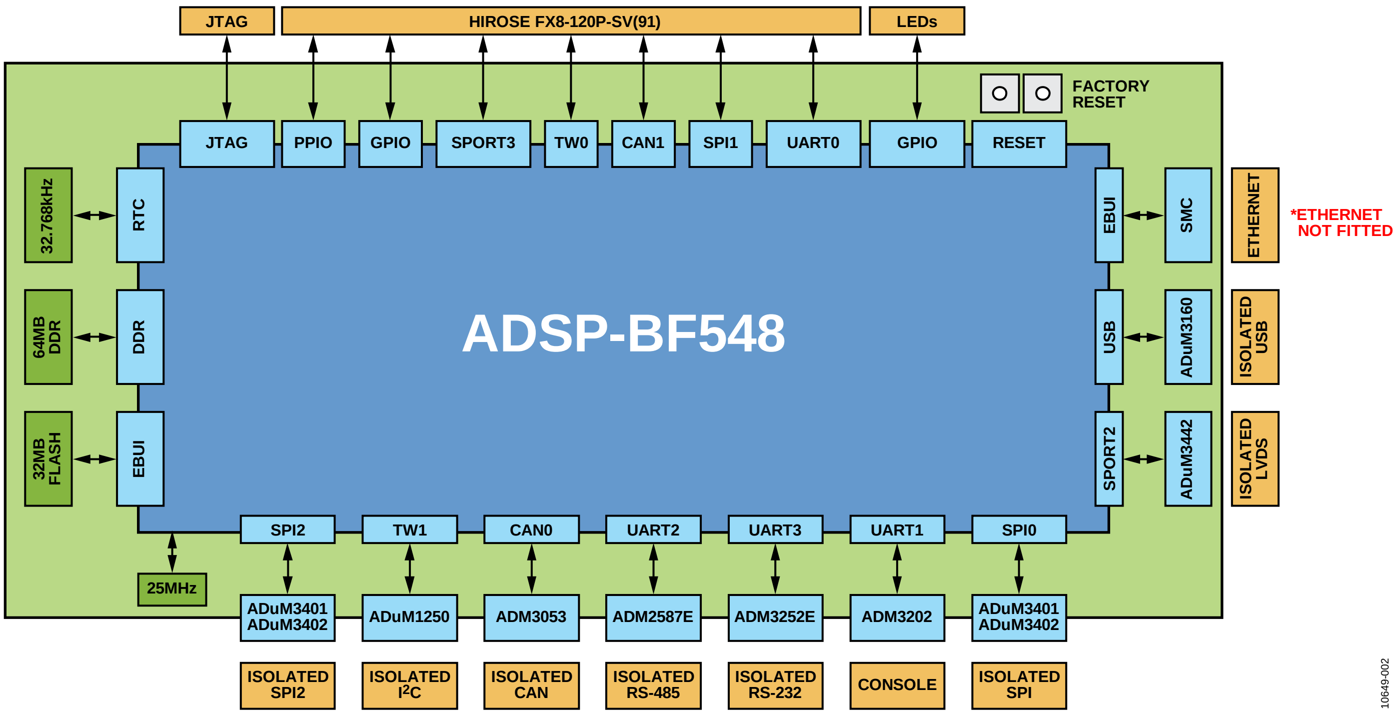

Figure 2. ezLINX Hardware Block Diagram

ISOLATED CAN

The isolated CAN port is implemented using the ADM3053 signal and power isolated CAN transceiver. The ADM3053 connects to CAN0 of the ADSP-BF548 and is capable of functioning at data rates of up to 1 Mbit/sec. Figure 3 shows a circuit diagram of the implementation of the ADM3053 on the *ez*LINX hardware.

The CAN node can be configured using Jumpers JP17 and JP18. When both Jumpers JP17 and JP18 are fitted, the CAN node is split terminated with 120 Ω and a common-mode capacitor of 47 nF. If termination is not required, remove JP17 and JP18. Table 4 shows the jumper configurations for all the interfaces on *ez*LINX.

The 5 V supply is connected to the V_{CC} pin (Pin 8) to power the *iso*Power isolated power supply of the ADM3053. This generates an isolated 5 V on the V_{ISOOUT} pin (Pin 12) of the ADM3053 and must be connected to the V_{ISOIN} pin (Pin 19). The 3.3 V supply is connected to the V_{IO} pin (Pin 6) to power the *i*Coupler signal isolation of the ADM3053. This is to ensure compatibility with the 3.3 V logic of the Blackfin ADSP-BF548. The R_S pin (Pin 18) is connected through a 0 Ω resistor to CAN_ISO_GND to deactivate slew rate limiting.

A 4-pin screw terminal connector, J8, is used for easy access to the CANH (Pin 1 of J8), CANL (Pin 3 of J8), and CAN_ISO_GND (Pin 2 and Pin 4 of J8) signals.

The AN-1123 Application Note, *Controller Area Network (CAN) Implementation Guide*, provides more information about implementing CAN nodes.

The ADM3053 contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for details on board layout considerations.

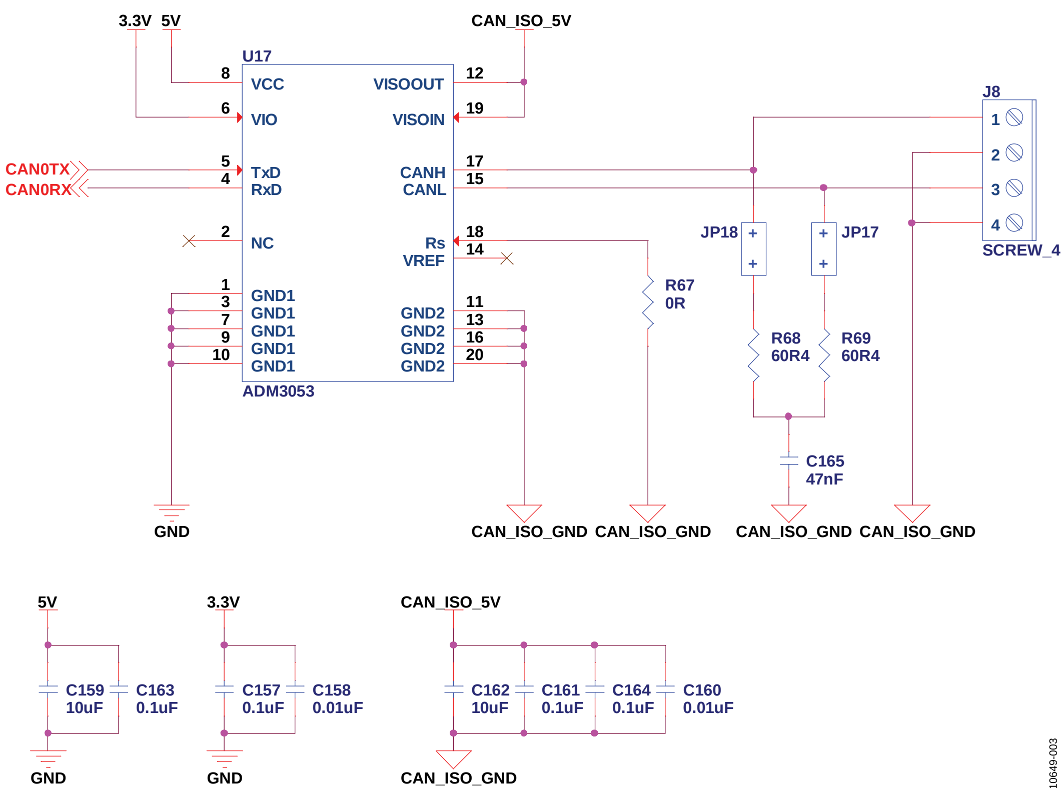

Figure 3. ADM3053 Isolated CAN Implementation

ISOLATED RS-485 AND RS-422

The isolated RS-485 and RS-422 port is implemented using the ADM2587E signal and power isolated CAN transceiver. The ADM2587E connects to UART2 of the ADSP-BF548 and is capable of functioning at data rates of up to 500 kbit/sec. Figure 4 shows a circuit diagram of the implementation of the ADM2587E on the *ez*LINX hardware.

The RS-485/RS-422 node can be configured using Jumpers JP3, JP4, JP19, and JP40. To configure the node as a half-duplex RS-485 node, connect JP3, JP4, and JP40. When JP3 and JP4 are fitted, A to Y are connected and B to Z are connected. When JP3 and JP4 are removed, the node is configured as a full-duplex RS-422 node. When JP19 is fitted, the A and B pins are terminated with 120 Ω. If termination is not required, remove JP19. When JP40 is connected, a pull-up resistor of 10 kΩ is connected to the RxD pin (Pin 4) of the ADM2587E. Table 4 shows jumper configurations for all the interfaces on *ez*LINX.

The 3.3 V supply is connected to the V_{CC} pins (Pin 2 and Pin 8) to power the *iso*Power isolated power supply and the *i*Coupler signal isolation of the ADM2587E. This generates an isolated 3.3 V on the V_{ISOOUT} pin (Pin 12) of the ADM2587E, which is connected to the V_{ISOIN} pin (Pin 19).

A 6-pin screw terminal connector, J7, is used for easy access to the A (Pin 2 of J7), B (Pin 3 of J7), Z (Pin 4 of J7), Y (Pin 5 of J7), and RS-485_ISO_GND (Pin 1 and Pin 6 of J7) signals.

The AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*, provides more information about implementing RS-485 and RS-422 circuits.

The ADM2587E contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during PCB layout to meet emissions standards. Refer to the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for details on board layout considerations.

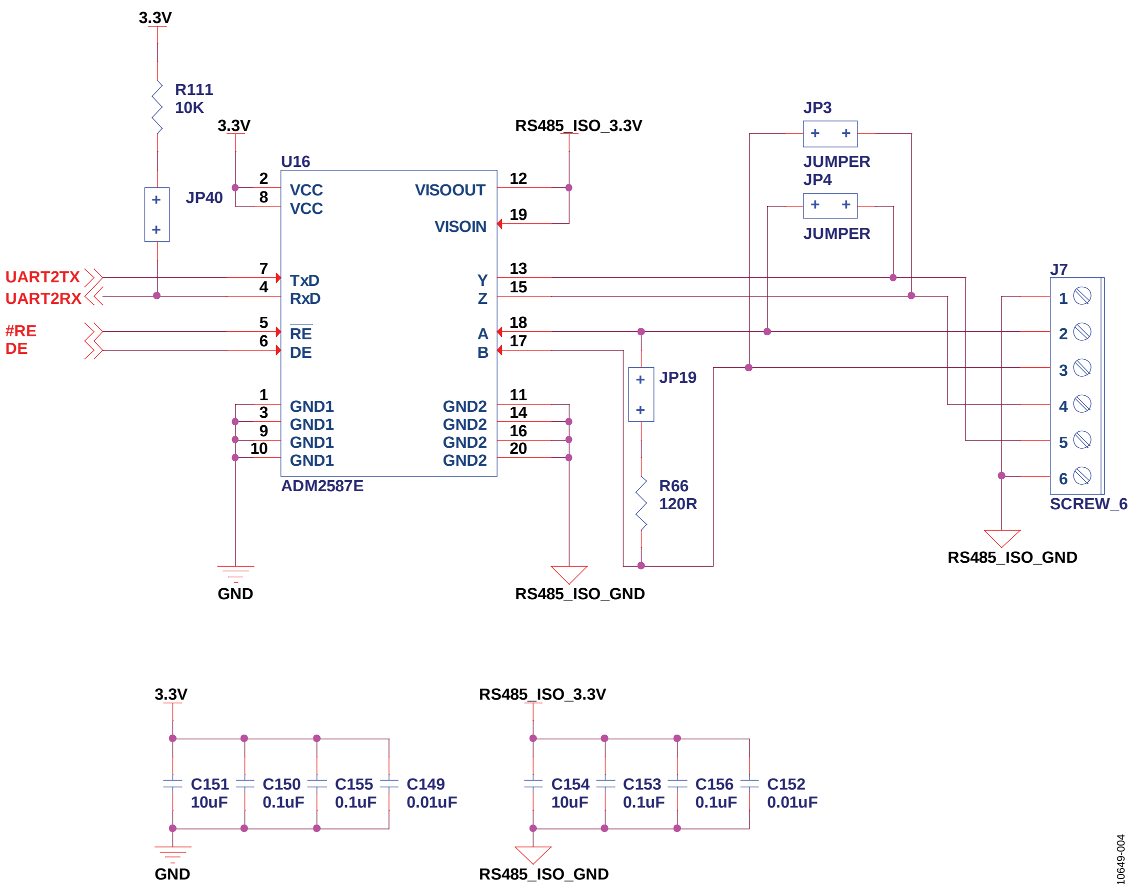

Figure 4. ADM2587E Isolated RS-485 and RS-422 Implementation

ISOLATED USB

The isolated USB port is implemented using the ADuM3160 full speed USB isolator. The ADuM3160 connects to the integrated PHY of the ADSP-BF548's USB controller and is capable of functioning at data rates of up to12 Mbit/sec. Figure 5 shows a circuit diagram of the implementation of the ADuM3160 on the *ez*LINX hardware.

The V_{BUS1} pin (Pin 1) and V_{DD1} pin (Pin 3) of the ADuM3160 are powered from the 5 V VBUS line of the USB mini connector and can only be connected to a USB master. The V_{BUS2} pin (Pin 16) and V_{DD2} pin (Pin 14) are powered from the 3.3 V generated by the *ez*LINX power supply.

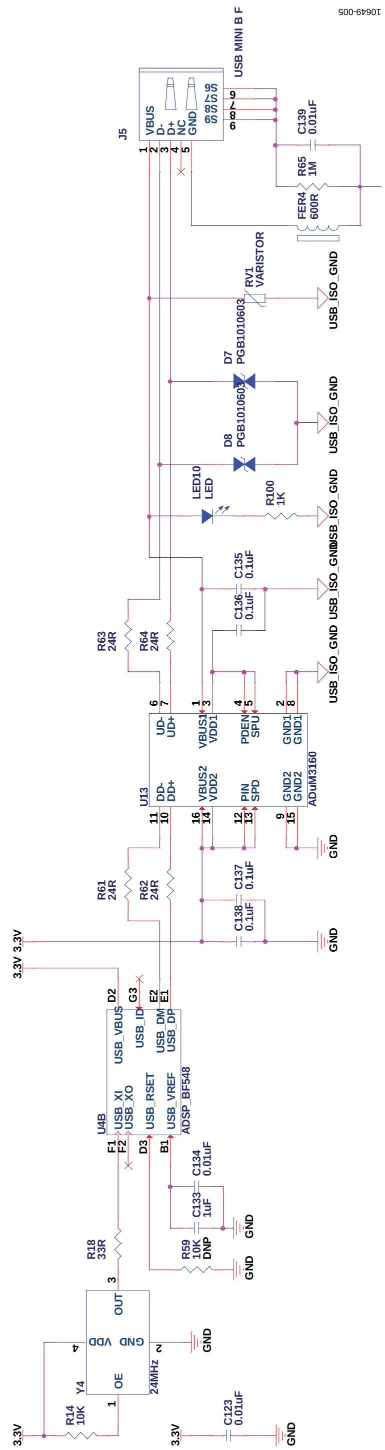

Figure 5. ADuM3160 Isolated USB Implementation

ISOLATED RS-232

The isolated RS-232 port is implemented using the ADM3252E signal and power isolated RS-232 transceiver. The ADM3252E connects to UART3 of the ADSP-BF548 and is capable of functioning at data rates of up to 460 kbit/sec. Figure 6 shows a circuit diagram of the implementation of the ADM3252E on the *ez*LINX hardware.

When the JP2 jumper is fitted, it implements a loopback of the isolated RS-232 transmitter output (Pin T_{OUT1}) to the receiver input (Pin R_{IN1}).

The V_{CC} pins (Pin A2, Pin B1, and Pin B2) of the ADM3252E are powered with 3.3 V and generate an isolated 3.3 V on the V_{ISO} pins (Pin A10, Pin B10, and Pin C10) using Analog Devices *iso*Power technology.

A 3-pin screw terminal connector, J6, is used for easy access to the T_{OUT1} (Pin 2 of J6), R_{IN1} (Pin 3 of J6), and RS232_ISO_GND (Pin 1 of J6) signals.

The ADM3252E contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during PCB layout to meet emissions standards. Refer to the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for details on board layout considerations.

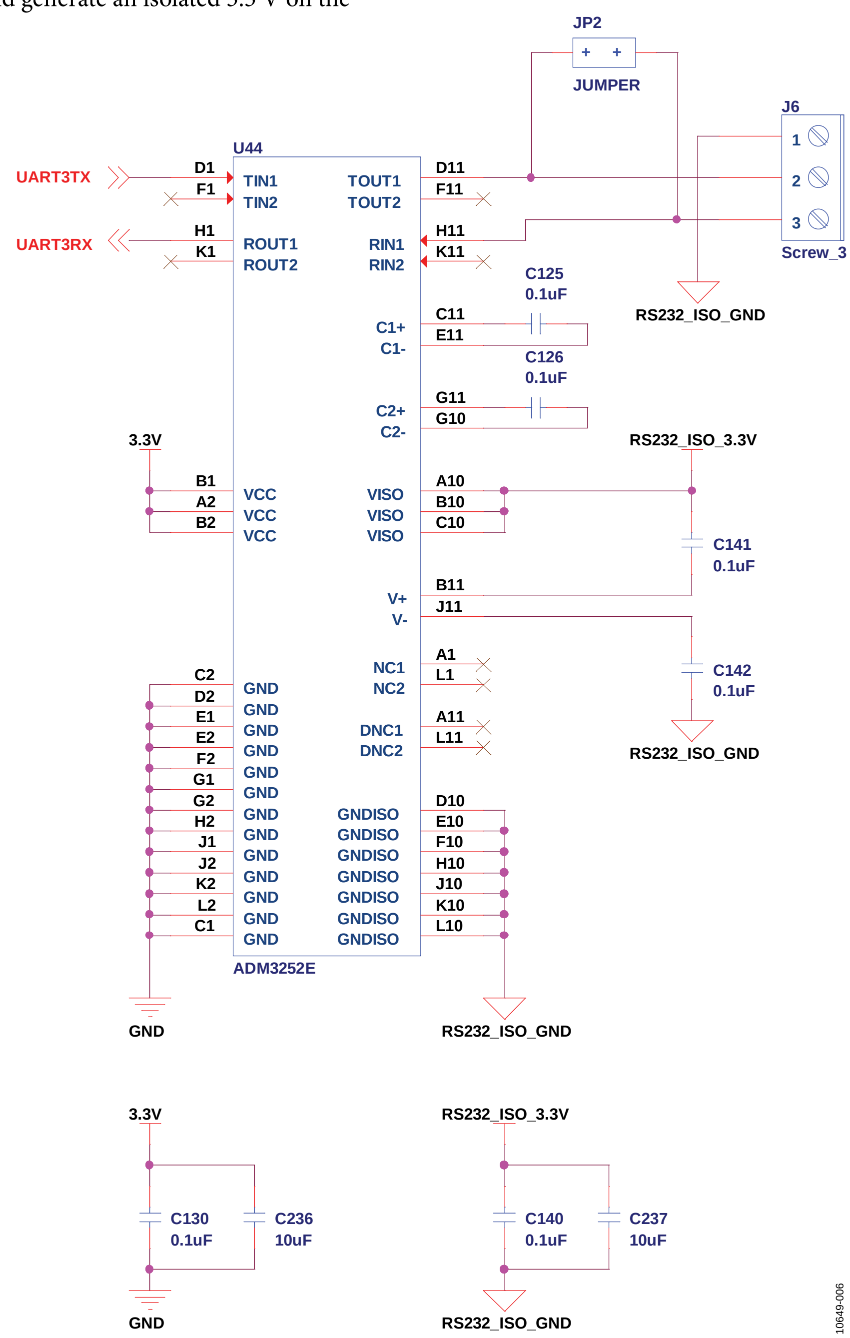

Figure 6. ADM3252E Isolated RS-232 Implementation

ISOLATED I^{2}C

The isolated I^{2}C port is implemented using the ADuM1250 I^{2}C isolator and the ADuM5000 *iso*Power isolated dc-to-dc converter. The ADuM1250 connects to TWI1 of the ADSP-BF548 and is capable of functioning at a maximum frequency of 1 MHz. Figure 7 shows a circuit diagram of the implementation of the ADuM1250 and ADuM5000 on the *ez*LINX hardware.

The V_{DD1} pin (Pin 1)) of the ADuM1250 and the V_{DD1} pins (Pin 1 and Pin 7) of the ADuM5000 are powered by 3.3 V. The ADuM5000 generates an isolated 3.3 V, which is used to supply power to the V_{DD2} pin (Pin 8) of the ADuM1250.

A 3-pin screw terminal connector, J22, is used for easy access to the SDA (Pin 1 of J22), SCL (Pin 2 of J22), and I2C_ISO_GND (Pin 3 of J22) signals.

The ADuM5000 contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during PCB layout to meet emissions standards. See the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for board layout recommendations.

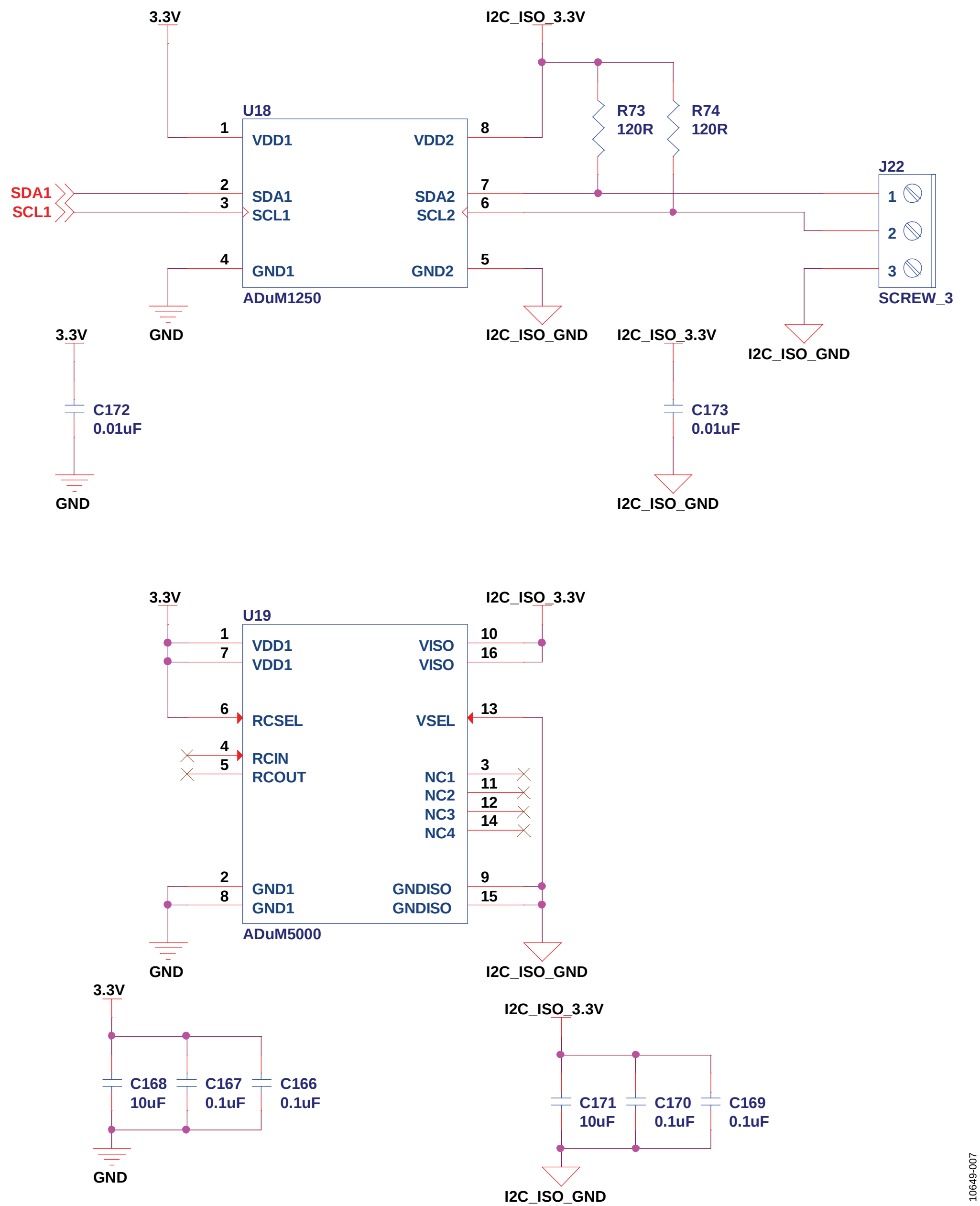

Figure 7. ADuM1250 and ADuM5000 Isolated I^{2}C Implementation

ISOLATED SPI

Two isolated SPI ports are implemented using the ADuM3401, the ADuM3402 *i*Coupler signal isolators, and the ADuM5000 *iso*Power isolated dc-to-dc converter. The isolated SPI0 implementation on the *ez*LINX hardware uses the ADuM3401. The ADuM3401 connects to SPI0 of the Blackfin ADSP-BF548 and is used to isolate the SCLK, MISO, SSEL1, and MOSI lines. The ADuM3402 is used for isolating the SPI slave select lines. Figure 8 shows a circuit diagram of the implementation of isolated SPI1 using the ADuM3401, ADuM3402, and ADuM5000 on the *ez*LINX hardware.

The isolated SPI2 implementation on the *ez*LINX hardware uses the ADuM3401. The ADuM3401 connects to SPI2 of the ADSP-BF548 and is used to isolate the SCLK, MISO, SSEL1, and MOSI lines. The ADuM3402 is used for isolating the SPI slave select lines. Figure 9 shows a circuit diagram of the implementation of the isolated SPI2 using the ADuM3401, ADuM3402, and ADuM5000 on the *ez*LINX hardware.

The V_{DD1} pin (Pin 1) of the ADuM3401 and ADuM3402 and the V_{DD1} pins (Pin 1 and Pin 7) of the ADuM5000 are powered by 3.3 V. The ADuM5000 generates an isolated 3.3 V, which is used to supply power to the V_{DD2} pin (Pin 16) of the ADuM3401 and ADuM3402.

Two 7-pin screw terminal connectors, J10 and J25, are used for easy access to the SPISCK (Pin 1 of J10 and J25), SPIMOSI (Pin 2 of J10 and J25), SPISEL1/SPISS (Pin 3 of J10 and J25), SPIMISO (Pin 4 of J10 and J25), SPISEL2 (Pin 5 of J10 and J25), SPISEL3 (Pin 6 of J10 and J25), and SPI_ISO_GND (Pin 7 of J10 and J25) signals.

To connect the isolated SPI0 as a master, connect Jumpers JP5, JP7, JP9, JP11, JP13, JP15, JP21, and JP36 while leaving Jumpers JP6, JP8, JP10, JP12, JP14, JP16, JP20, and JP37 open (see the Warnings section). To connect the isolated SPI0 as a slave, connect Jumpers JP6, JP8, JP10, JP12, JP14, JP16, JP20, and JP37 while leaving Jumpers JP5, JP11, JP13, JP15, JP21, and JP36 (see the Warnings section).

Table 1. Isolated SPI0 Connections

Jumper	SPI0 Master	SPI0 Slave
JP5	Connect	Open
JP6	Open	Connect
JP7	Connect	Open
JP8	Open	Connect
JP9	Connect	Open
JP10	Open	Connect
JP11	Connect	Open
JP12	Open	Connect
JP13	Connect	Open
JP14	Open	Connect
JP15	Connect	Open
JP16	Open	Connect
JP20	Open	Connect
JP21	Connect	Open
JP36	Connect	Open
JP37	Open	Connect

To connect the isolated SPI2 as a master, connect Jumpers JP22, JP24, JP26, JP28, JP30, JP32, JP35, and JP38 while leaving Jumpers JP23, JP25, JP27, JP29, JP31, JP33, JP34, and JP39 open (see the Warnings section). To connect the isolated SPI2 as a slave, connect Jumpers JP23, JP25, JP27, JP29, JP31, JP33, JP34, and JP39 while leaving Jumpers JP22, JP24, JP26, JP28, JP30, JP32, JP35, and JP38 open (see the Warnings section).

Table 2. Isolated SPI2 Connections

Jumper	SPI2 Master	SPI2 Slave
JP22	Connect	Open
JP23	Open	Connect
JP24	Connect	Open
JP25	Open	Connect
JP26	Connect	Open
JP27	Open	Connect
JP28	Connect	Open
JP29	Open	Connect
JP30	Connect	Open
JP31	Open	Connect
JP32	Connect	Open
JP33	Open	Connect
JP34	Open	Connect
JP35	Connect	Open
JP38	Connect	Open
JP39	Open	Connect

The ADuM5000 contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during PCB layout to meet emissions standards. See the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for board layout recommendations.

Warnings

JP20 and JP21

JP20 and JP21 should never both be connected because doing so will create a short circuit between 3.3 V and GND.

JP34 and JP35

JP34 and JP35 should never both be connected because doing so will create a short circuit between 3.3 V and GND.

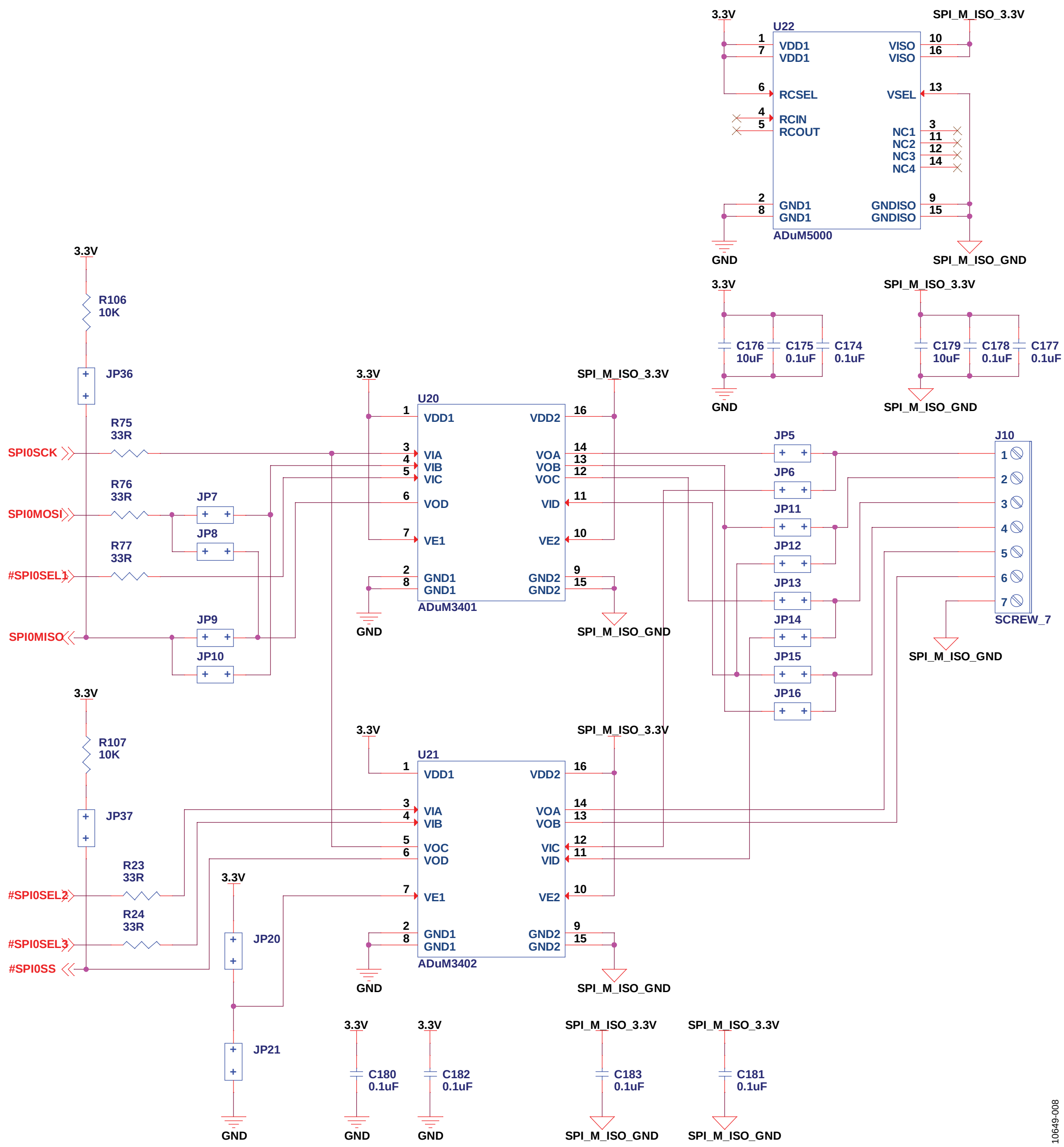

Figure 8. ADuM3401, ADuM3402, ADuM5000 Isolated SPI1 Implementation

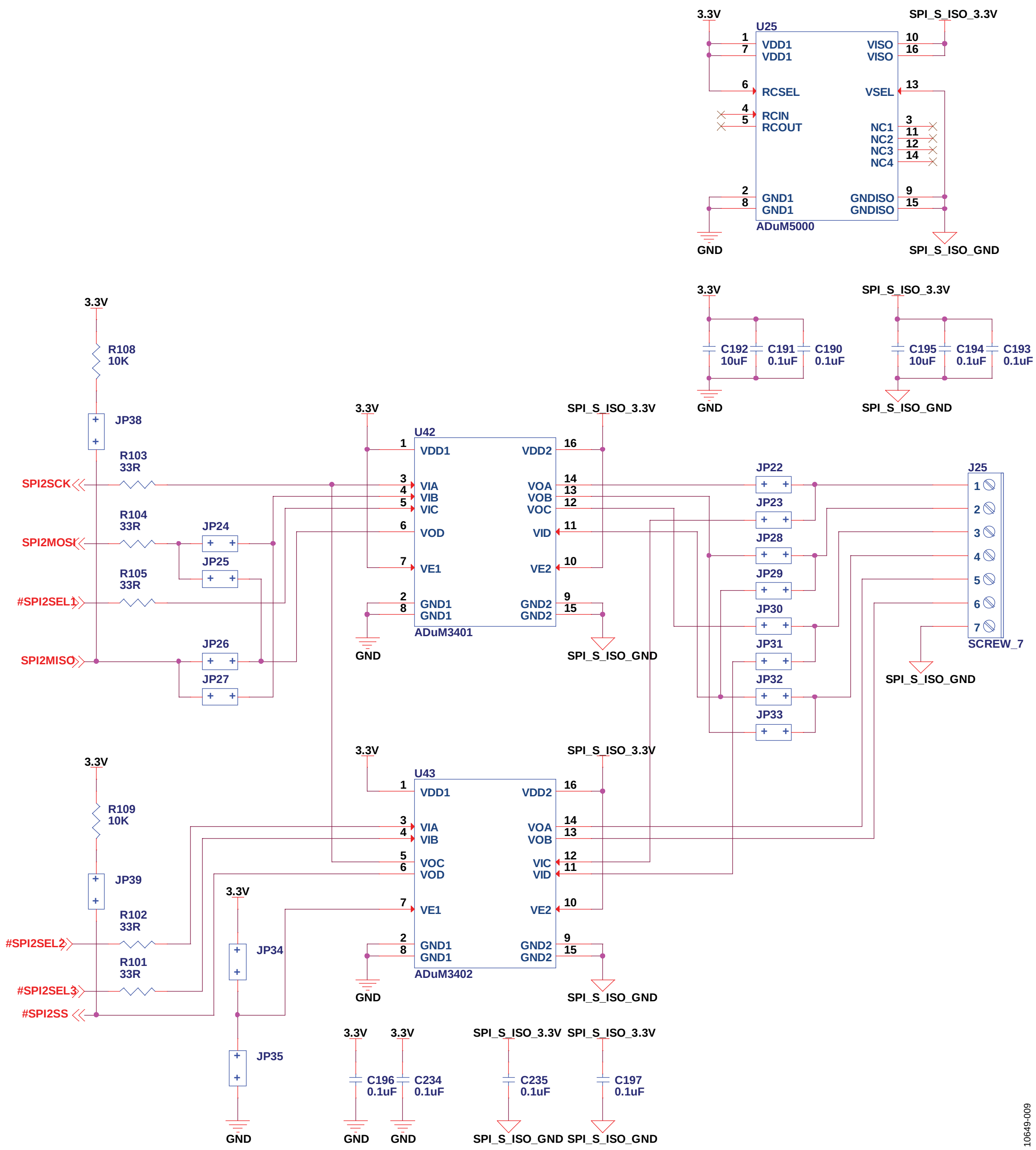

Figure 9. ADuM3401, ADuM3402, ADuM5000 Isolated SPI2 Implementation

ISOLATED LVDS

The isolated LVDS port is implemented using the ADuM3442 *i*Coupler signal isolator, the ADN4664 dual LVDS receiver, the ADN4663 dual LVDS transmitter, and the ADuM5000 *iso*Power isolated dc-to-dc converter. The ADuM3442 is connected to SPORT2 of the ADSP-BF548. Figure 10 shows a circuit diagram of the implementation of the isolated LVDS using the ADuM3442, ADN4663, ADN4664, and ADuM5000 on the *ez*LINX hardware.

The V_{DD1} pin (Pin 1) of the ADuM3442 and the V_{DD1} pin (Pin 1 and Pin 7) of the ADuM5000 are powered by 3.3 V. The ADuM5000 generates an isolated 3.3 V, which is used to supply power to the V_{DD2} pin (Pin 16) of the ADuM3442, the V_{CC} pin (Pin 1) of the ADN4663, and the V_{CC} pin (Pin 8) of the ADN4664.

A 32-pin header connector is used for easy access to the isolated LVDS signals.

The ADuM5000 contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during PCB layout to meet emissions standards. See the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with* iso*Power Devices*, for board layout recommendations.

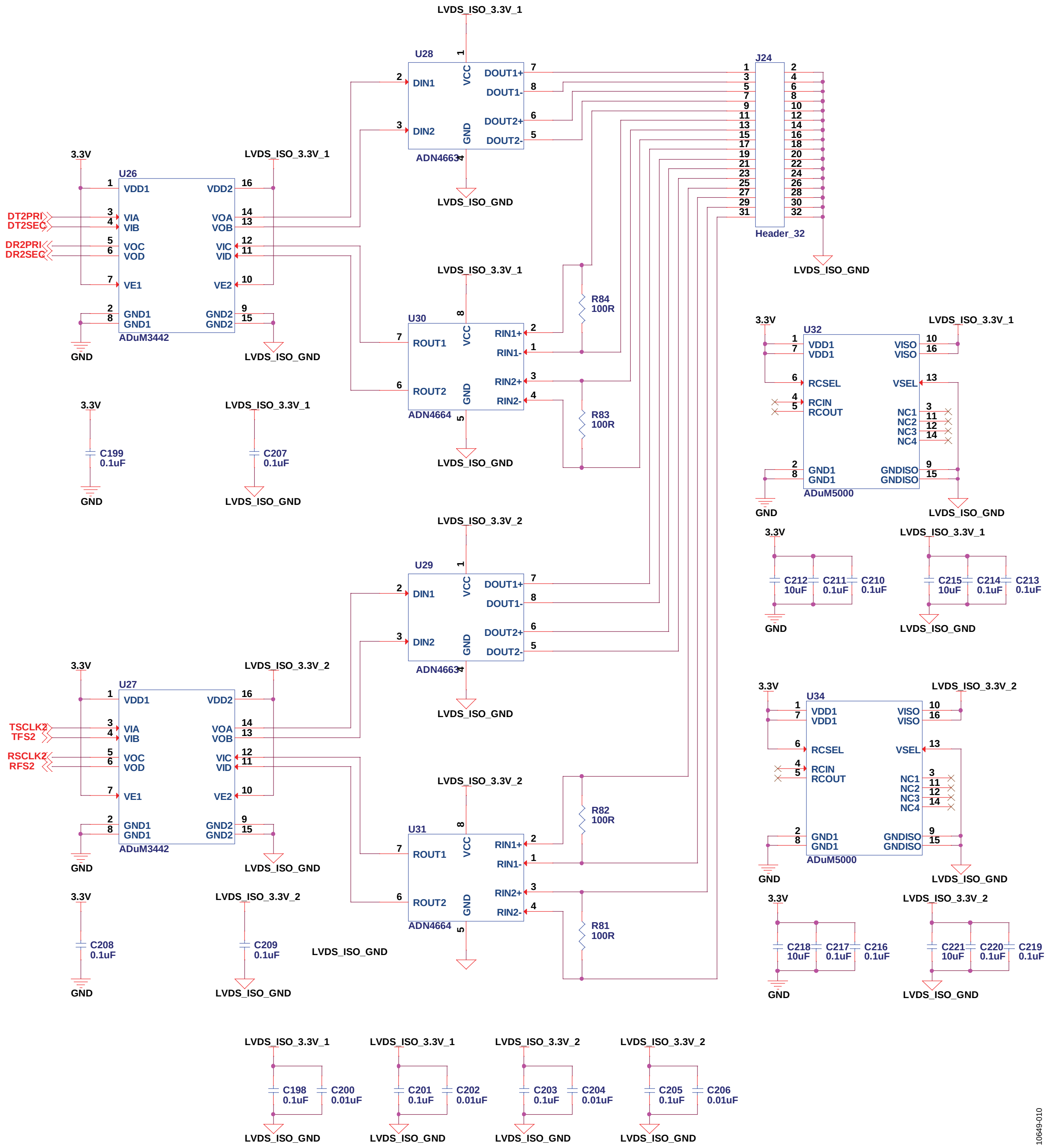

Figure 10. ADuM3442, ADN4663, ADN4664, and ADuM5000 Isolated LVDS Implementation

POWER INPUT

An ac-to-dc desktop power supply is used to supply 7.5 V input to the J1 barrel connector on the *ez*LINX hardware. This supply connects to the UNREG_IN node of the circuit through a protection circuit as shown in Figure 11.

3.3 V POWER SUPPLY

The ADP1864 constant frequency, current-mode, step-down dc-to-dc controller is used with an external P-channel MOSFET to generate the regulated 3.3 V power supply for the *ez*LINX hardware. The circuit implementation of the 3.3 V power supply is shown in Figure 12.

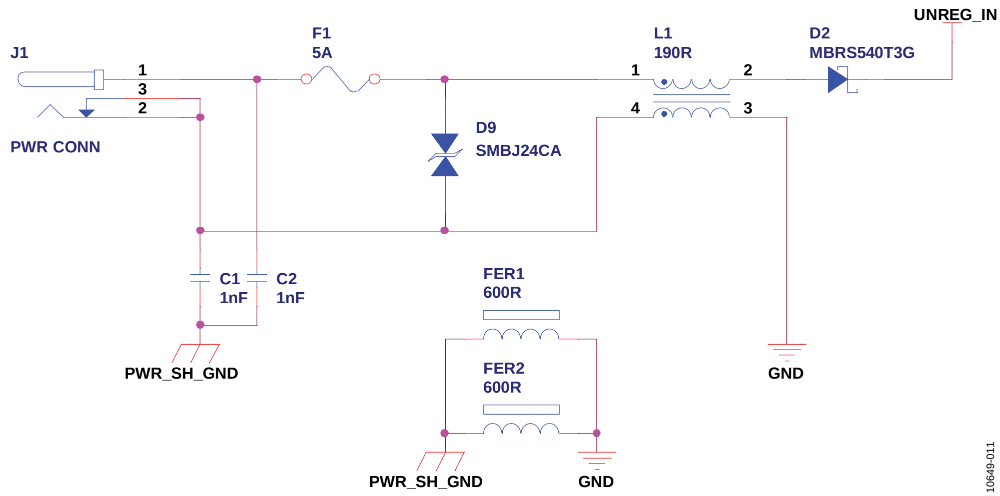

Figure 11. Power Input

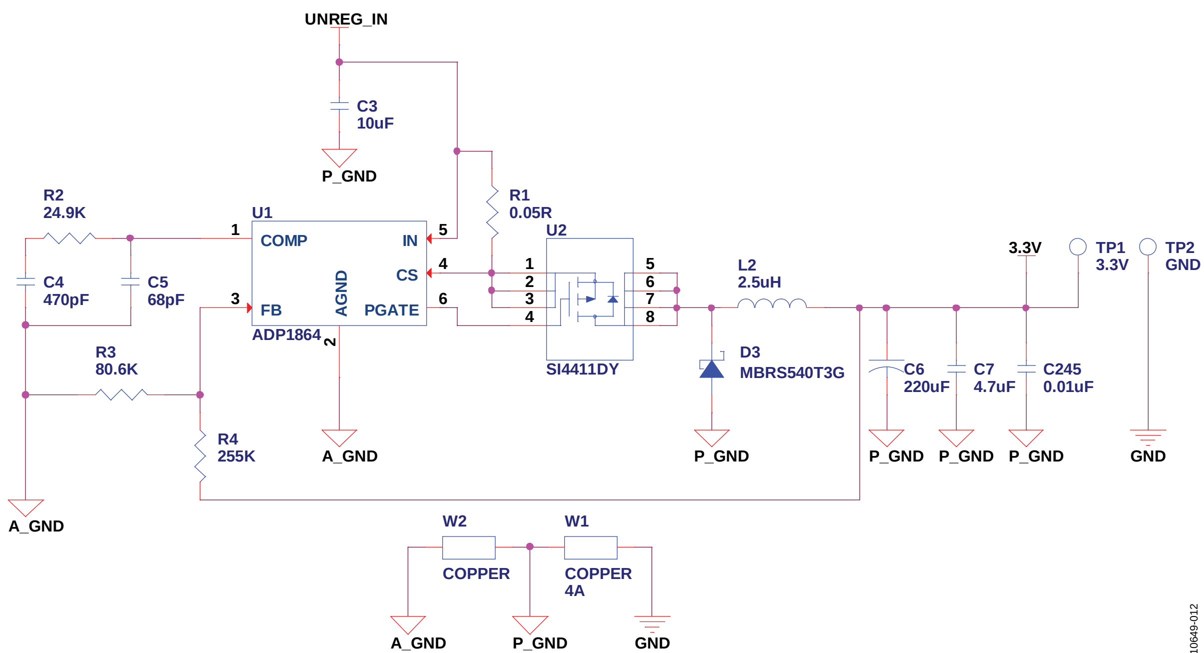

Figure 12. 3.3 V Power Supply

1.2 V, 2.5 V, AND 5 V POWER SUPPLIES

A P-channel MOSFET is used to regulate the 3.3 V input to 1.2 V (see Figure 13). The ADP1706 linear regulator is used to regulate the 3.3 V input to 2.5 V (see Figure 14). The ADP3335 low dropout regulator is used to regulate the UNREG_IN input to 5 V (see Figure 15).

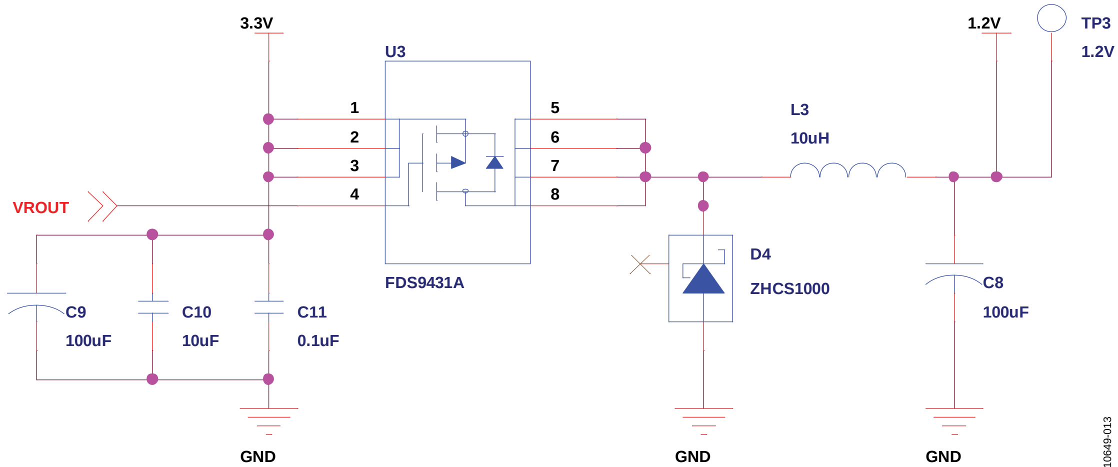

Figure 13. 1.2 V Power Supply

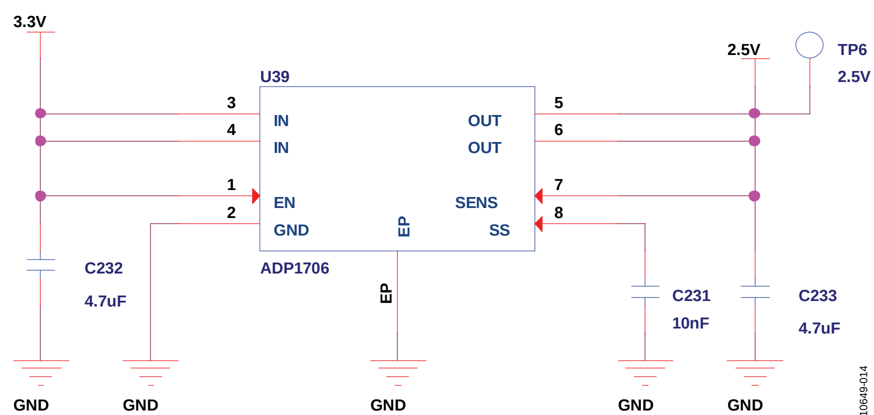

Figure 14. 2.5 V Power Supply

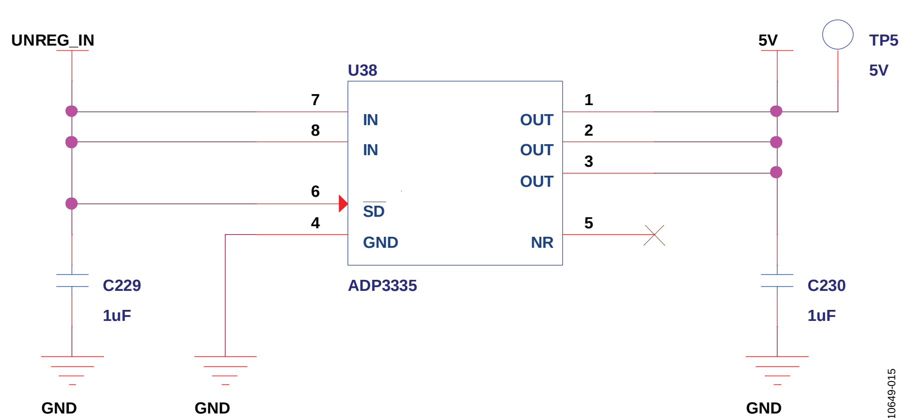

Figure 15. 5 V Power Supply

EXTENDER CONNECTOR

The Hirose FX8-120P-SV(91) extender connector is used for daughter board connections. This allows additional functionality to be added to the ezLINX hardware. Figure 16 shows the circuit implementation of the J23 and J26 extender connectors. Connector J26 is a 3-pin header connector that allows the CAN1 signals of the ADSP-BF548 to be routed to an external daughter board.

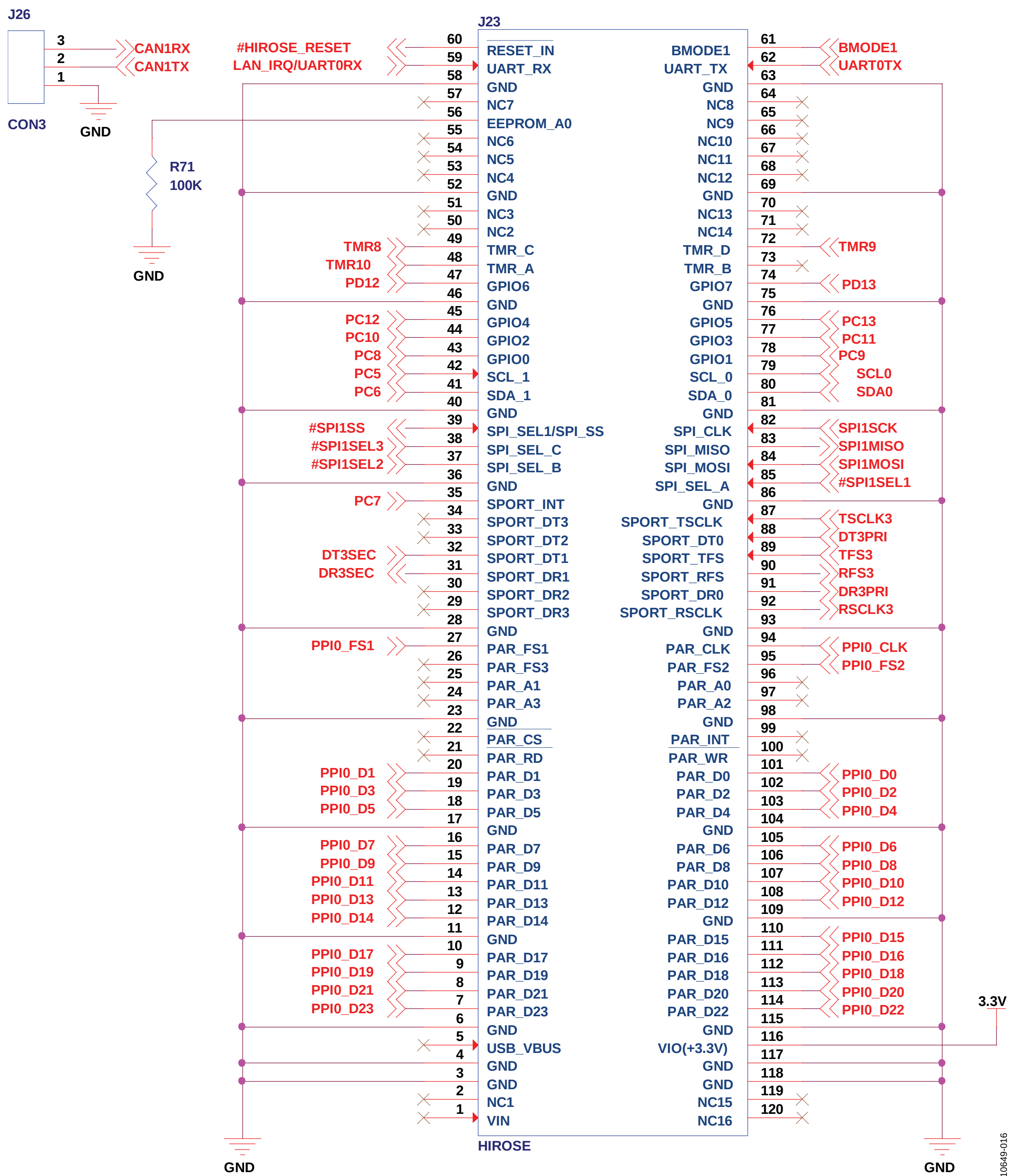

Figure 16. Extender Connector Using Hirose FX8-120P-SV(91)

RS-232 CONSOLE

The RS-232 console connector is used for accessing the console of the uClinux kernel running on the ADSP-BF548 processor. It uses the ADM3202 RS-232 line driver and receiver to connect to UART1 of the ADSP-BF548. The RS-232 signals connect to a DB-9 connector, J4. A circuit implementation of the RS-232 console is shown in Figure 17.

The RS-232 console is used to directly access the uClinux kernel running on the ADSP-BF548. When the console is connected to a RS-232 port on the PC, the kernel can be accessed through a terminal program.

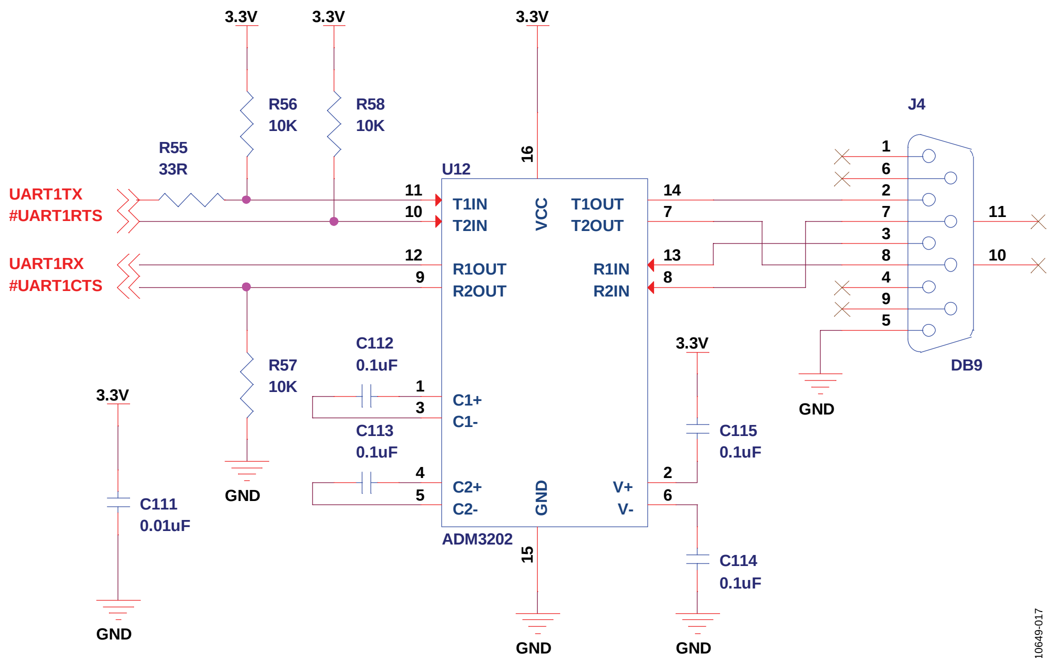

Figure 17. RS-232 Console Implementation

LEDs

There are 10 LEDs on the *ez*LINX evaluation board. The red LED6 illuminates to indicate when the reset button is being pressed. The orange LED10 illuminates to indicate when the isolated USB port is connected to a USB port on the PC. The green LED7 illuminates to indicate when the board is powered.

The orange LED1 illuminates to indicate when the uClinux kernel and application finishes booting up.

Table 4 describes the functionality and connections of the LEDs for the ADSP-BF548 and other circuitry.

Table 3.

LED	ADSP-BF548 Port	Function
LED1	PD6	Illuminates when the uClinux kernel and application finishes booting up. This LED can also be used as a general-purpose indicator that can be turned on and off through software.
LED2	PD7	General-purpose indicator that can be turned on and off through software.
LED3	PD8	General-purpose indicator that can be turned on and off through software.
LED4	PD9	General-purpose indicator that can be turned on and off through software.
LED5	PD10	General-purpose indicator that can be turned on and off through software.
LED6	PD11	General-purpose indicator that can be turned on and off through software.
LED7	Not Applicable	Illuminates when the 3.3 V power supply is available.
LED8	Not Applicable	Illuminates when the reset button is pressed.
LED10	Not Applicable	Illuminates when the VBUS voltage from the USB host is connected.

JUMPER CONFIGURATIONS

Table 4.

Interface	Configuration	Jumpers Fitted	Jumpers Open
RS-485/RS-422	Half-duplex configuration	JP3, JP4, JP40	Not applicable
	Full-duplex configuration	Not applicable	JP3, JP4, JP40
	120 Ω termination	JP19	Not applicable
RS-232	Loopback T_{OUT1} to R_{IN1}	JP2	Not applicable
CAN	Split terminate the bus with 120 Ω and a common-mode 47 nF capacitor	JP17, JP18	Not applicable
	No termination	Not applicable	JP17, JP18
SPI0	Master mode	JP5, JP7, JP9, JP11, JP13, JP15, JP20,[1] JP36	JP6, JP8, JP10, JP12, JP14, JP16, JP21,[1] JP37
	Slave mode	JP6, JP8, JP10, JP12, JP14, JP16, JP21, JP37	JP5, JP7, JP9, JP11, JP13, JP15, JP20, JP36
SPI2	Master mode	JP22, JP24, JP26, JP28, JP30, JP32, JP35,[2] JP38	JP23, JP25, JP27, JP29, JP31, JP33, JP34,[2] JP39
	Slave mode	JP23, JP25, JP27, JP29, JP31, JP33, JP34, JP39	JP22, JP24, JP26, JP28, JP30, JP32, JP35, JP38

[1] Warning: JP20 and JP21 should never both be connected because doing so will create a short circuit between 3.3 V and GND.
[2] Warning: JP34 and JP35 should never both be connected because doing so will create a short circuit between 3.3 V and GND.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

UG10649-0-8/12(0)

ANALOG DEVICES

www.analog.com