ANALOG DEVICES

AN-629
APPLICATION NOTE

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ADN2841 Evaluation Kit

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INTRODUCTION

This application note describes the ADN2841 laser diode driver evaluation kit. The evaluation kit is a demonstration board that provides electrical evaluation of the ADN2841. This document describes how to configure the board in order to operate the part electrically. The document contains the following information:

- Board description
- Quick start for electrical operation
- Description of board settings
- Component list
- Schematic of board
- Silkscreen image of board

BOARD DESCRIPTION

The ADN2841 is a dual-loop 50 Mbps to 2.7 Gbps laser diode driver. To use the board in an electrical configuration, a current mirror circuit is employed to close the average power and extinction ratio control loops and thus takes the place of the laser and monitor diodes. Mirror gain is related to laser slope efficiency and MPD current. Resistors R2 through R4 allow the user to modify the gain of the current mirror such that the LDD can be used over the full slope efficiency and modulation current range. The board is initially set up to divide the sum of the bias current and the average modulation current by 50, thus producing the simulated monitor photodiode current. Note that the circuitry provided for the current mirror does not simulate the laser diode threshold current. Power, DEGRADE, and FAIL LEDs are made available for monitoring purposes. **Power to the board is –5 V only.**

QUICK START FOR ELECTRICAL OPERATION

To ensure proper operation in the electrical configuration, verify the following:

1. Jumper K1 is connected (shorted circuit).
2. Jumpers K3 and K4 are connected to A; Jumpers K2 and K5 are connected to B.
3. If the input data is clocked, it is necessary to enable the clock select pin (CLKSEL). CLKSEL is enabled by connecting K4 to B. If the clock inputs are not used, or the input data is not latched, connect K4 to A.
4. Adjust R21, the bias potentiometer, until the combined series resistance of R21 and R33 is roughly 1.2 kΩ.
5. Adjust R20, the modulation potentiometer, until the combined series resistance of R20 and R32 is 3 kΩ.
6. Set R19, the alarm set potentiometer, until the combined series resistance of R19 and R31 is 1 kΩ.
7. Power up the board by applying –5 V to the power input SMA.
8. Apply a differential signal, typically 500 mV, to J6 and J7 (DATAN and DATAP).
9. If the clock select pin is enabled by K4, apply a differential clock signal, typically 500 mV, to J4 and J5 (CLKN and CLKP).
10. The electrical eye and switching characteristics of the ADN2841 may be observed using a digital communications analyzer or high speed oscilloscope through the SMA Connector J2, the IMODP output.
11. The bias and modulation currents can also be monitored by observing IBMON and IMMON, respectively. IBMON and IMMON are both a 1:100 ratio of I_{BIAS} and IMOD. Both are terminated with resistors and can be viewed at Test Points T3 and T4 using a voltmeter or oscilloscope.
12. I_{BIAS} and IMOD will be set to approximately 20 mA and 40 mA, respectively, using the resistance values given above for R20 combined with R32 and R21 combined with R33. To change the average power or extinction ratio, use the following procedure. Adjust R21 to get the desired I_{BIAS}. Note that when increasing I_{BIAS} and IMOD, users need to first adjust R21 such that the current increases to the new I_{BIAS} plus half the increase intended for IMOD. Then adjust R20 to get the desired IMOD. This will also have the effect of returning I_{BIAS} to its intended value. It may take a couple of iterations to adjust the settings correctly. This is due to the dual-control loop effect. It is important to note that there is no threshold current adjustment on this evaluation board and, therefore, continually increasing the modulation current, IMODN, may result in the bias current, I_{BIAS}, falling to zero. I_{BIAS} cannot go negative. The allowable resistance range at the Power Set Input (PSET), the Extinction Ratio Set Input (ERSET), and the Alarm Set (ASET) is between 1 kΩ and 25 kΩ. Resistors R31 through R33 ensure that the resistance at these nodes never falls below the minimum allowable value. If the node resistances increase above 25 kΩ, the ADN2841 will not operate within its specifications.

Table I. Description of Board Settings

Component	Name	Function
J3	POWER	–5 V Power Input to Board.
J2	IMODP	IMODP Output. Connect to oscilloscope with 50 Ω input impedance.
J1	IDTONE	IDTONE Input.
J4	CLKN	CLKN Input.
J5	CLKP	CLKP Input.
J6	DATAP	DATAP Input.
J7	DATAN	DATAN Input.
T1	IMPDMON	IMPD Current Mirror Output.
T2	IMPDMON2	MPD2 Current Mirror Output.
T3	IBMON	Bias Current Mirror Output.
T4	IMMON	Modulation Current Mirror Output.
R19	ASET Potentiometer	Adjusts Bias Threshold Current for DEGRADE and FAIL Alarms.
R20	ERSET Potentiometer	Adjusts the Extinction Ratio.
R21	PSET Potentiometer	Adjusts the MPD current and thus the average power.
K1	K1	Jumper to Bypass Supply Protection Diode.
K2	K2	Jumper for LBWSET.
K3	K3	Jumper to Exercise ALS.
K4	K4	Jumper for CLKSEL.
K5	K5	Jumper for IDTONE.

NOTES
1. The bandwidth of the control loops will vary when the PSET resistor or current mirror gain is varied. Users' evaluation of the ADN2841 should cover a range of settings of the PSET resistor and current mirror gain. This range should be equivalent to users' expected range of laser specifications and power and extinction ratio settings.
2. It is important to note that the resistor values for R2 through R4 on this evaluation board will not support the full slope efficiency range of the various lasers on the market. These resistor values may need to be changed to ensure the PNP current mirror has adequate headroom for operation at maximum and minimum I_{BIAS} and IMOD.

Table II. Component List

Component	Quantity	Description
R19, R20, R21	3	50 kΩ Trim Potentiometers
D1	1	Supply Protection Diode (1N4001)
D2, D3, D4	3	SMD LEDs
C4–C12	9	10 nF Capacitors
C2	1	220 μF Capacitor
C13, C14	2	1 μF Capacitors (Loop Bandwidth Setting)
Q3, Q4	2	Transistors (SOT-23)
C1	1	22 μF Capacitor
C3	1	1 nF Capacitor
R15, R18	2	10 kΩ Resistors
R3, R4	2	20 Ω Resistors
R7	1	51 Ω Resistor
R2	1	510 Ω Resistor
R1, R16, R17,	3	330 Ω Resistors
R6, R31–R33	4	1 kΩ Resistors
R11, R12, R13, R14	4	1.5 kΩ Resistors
R10, R25, R26*, R27*, R28, R29	6	0 Ω Resistors
K1–K5	5	Pin Header Jumper Sockets
J1–J8*	8	SMA Connectors
U1	1	ADN2841
L1	1	10 μH Inductor

*Components that are not populated.

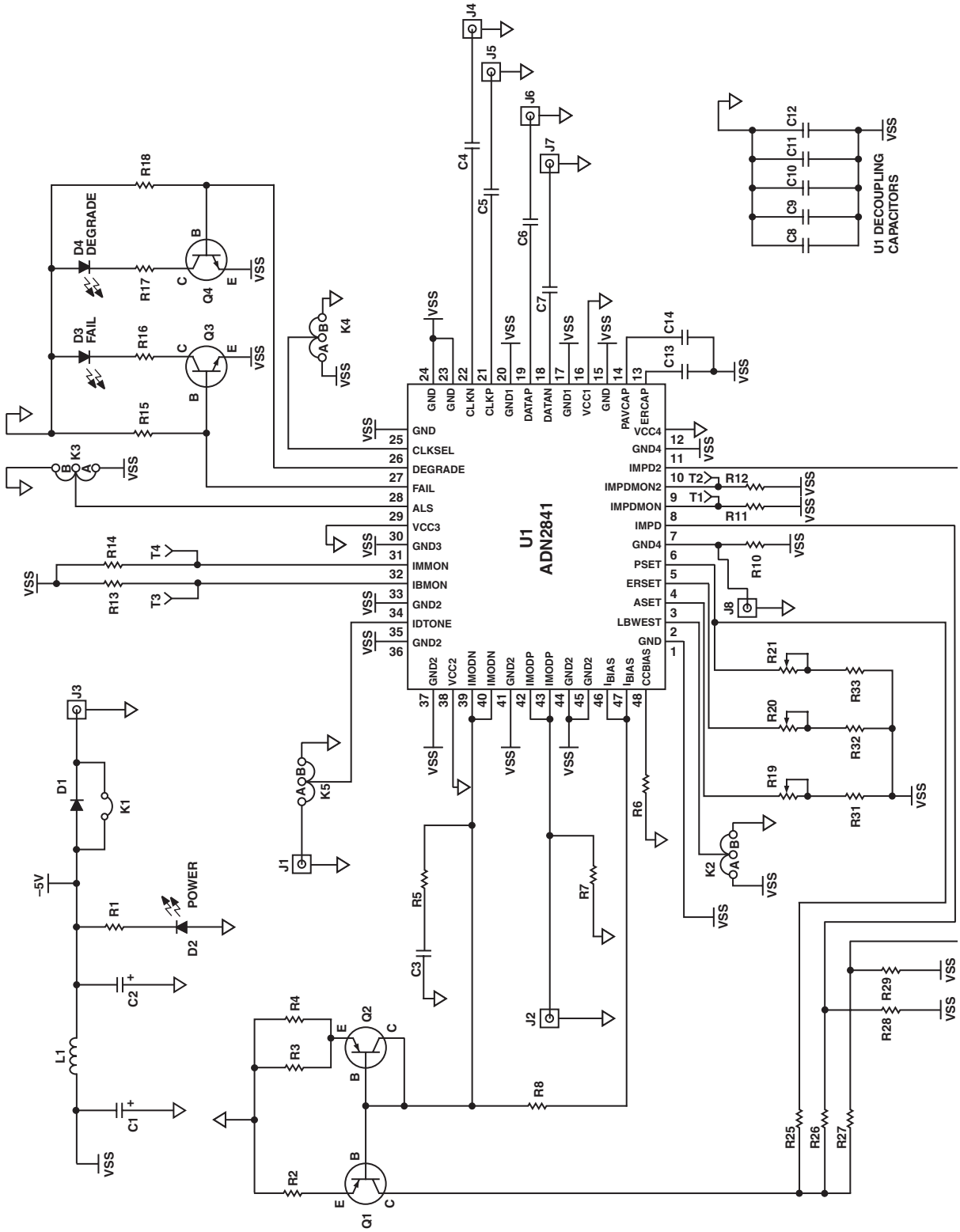

Figure 1. Schematic of Board

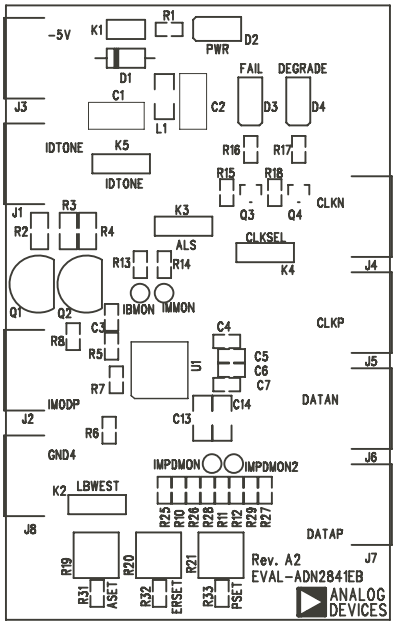

Figure 2. Silkscreen Image of Board

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