

Preliminary Technical Data

FEATURES

Small Form-factor Pluggable (SFP) MSA compliant SFF-8472 Digital Diagnostic Monitoring Multi-Rate from 155Mbps to 4.25Gbps Internal Calibration Closed-Loop control of extinction ratio(ADN2870) Build-in LOS/RSSI detectors (ADN2891/2) Embedded MCU, MicroConverter®(ADuC7020):

- 16/32-bit RISC ARM7TDMI core, 45MIPS peak
- 5 channels 12-bit ADC
- 4 x 12-bit DACs
- On-chip Power Supply Monitor
- On-chip Temperature Monitor
- Programmable Logic Array
- 62K Bytes EEPROM, 8K Bytes SRAM
- Four I²C Device Addressing

APPLICATONS

Multi-rate OC-3 to OC-48FEC SFP/SFF Modules 1x/2x/4x Fibre Channel Modules Gigabit Ethernet Modules

DESCRIPTION

The SFP Reference Design Kit(SFP-RDK) provides a complete optical transceiver chipset and system-level solution for designers. The SFP-RDK includes:

- SFP Transceiver Module Board
- SFP Host Board
- JTAG Adapter board
- PCB Schematics
- PCB Layout, Gerber Files, CAD Files
- Bill of Materials
- SFP Firmware Source Code in ANSI C
- Evaluation GUI software
- Applications Note(AN-706), User Manuals

The SFP-RDK consists of Analog Devices' optical transceiver chip set: the ADN2870 dual loop laser driver, the ADN2880/2 Transimpedance amplifier, the ADN2891/2 Limiting amplifier and the ADuC7020 MicroConverter*. Use of the micro-controller allows flexible module designs support user definable functions.



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11/03/2004

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ELECTRICAL CHARACTERISTICS

(T_A= T_{MAX} to T_{MIN}, V_{CC}= 3.1V to 3.5V, unless otherwise noted, refer to individual datasheets)

PARAMETER	MIN	ТҮР	MAX	UNITS	CONDITIONS
POWER SUPPLY					
Supply Voltage	3.10		3.50	V	
Power Dissipation					2.488Gbps, PRBS2^23-1
MicroConverter (ADuC7020)		3		mA	Normal Mode, 1MHz Clock
		TBD		mA	Average power
Laser Driver (ADN2870)		30		mA	TX_Disable asserted
Limiting Amplifier (ADN2871)		TBD		mA	TX_Disable asserted
Limiting Amplifier (ADN2891)		44	60	mA	
Limiting Amplifier (ADN2892)		50		mA	
Fransimpedance Amplifier (ADN2880)	50	75	120	mA	$I_{INAVE} = 0 \text{ mA}$
Fransimpedance Amplifier (ADN2882)		TBD		mA	$I_{INAVE} = 0 \text{ mA}$
TRANSMITTER					
Laser Bias Current	2		100	mA	
Laser Modulation Current	5		90	mA	
Differential Input Data Voltage	0.4		2.4	Vp-р	
TX Fault Output Low Voltage			0.8	V	
TX Fault Output High Voltage	2.4			V	
TX Disable Input Low Voltage			0.8	V	
TX Disable Input High Voltage	2.4			V	
RECEIVER					
Differential Output Data Voltage	650	700	800	mVp-p	
LOS Output Low Voltage			0.8	V	
LOS Output High Voltage	2.4			V	
Random Jitter		2	5	ps RMS	Input>10mVp-p, OC-48, PRBS2 ²³ -
Deterministic Jitter		13.7	19	ps p-p	Input>10mVp-p, OC-48, PRBS2 ²³ -

TIMING CHARACTERISTICS

PARAMETER	MIN	ΤΥΡ	MAX	UNITS	CONDITIONS
Serial ID Clock Range			100	KHz	
Tx Disable Assert Time			10	μs	
Tx Disable Negate Time			1	ms	
Time to Initialize, including					
Reset of TX_FAULT			300	ms	
Tx Fault Assert Time			100	μs	
TX Disale to Reset	10				
LOS Assert Time		600		μs	
LOS Deassert Time		100		μs	
RX Data Output Rise Time		65		ps	20%-80%
RX Data Output Fall Time		65		ps	20%-80%

Ordering Guide

Model	Description	Supported Data Rates	Supported Lasers	PC Board	IC's
EVAL-ADNSFP-SE	Single-ended	OC-3 to OC-48FEC	FP/DFB/VCSEL	V1.3	ADN2891
	laser drive	100/1000 Ethernet			ADN2880
					ADN2870
					ADuC7020
EVAL-ADNSFP-Diff	Differential laser	OC-3 to OC-48FEC	FP/DFB/VCSEL	V1.4	ADN2891
	drive	Rate to 3.3Gbps			ADN2880
					ADN2870
					ADuC7020
EVAL-ADNSFP-FC	Differential laser	100/1000 Ethernet	FP/DFB/VCSEL	V1.4	ADN2892
	driver	1x/2x/4x Fiber Channel			ADN2882
					ADN2870
					ADuC7020

Note: The EVAL-ADNSFP-FC will support the ADN2891 Limiting Amp pinout and functionality allowing this board to handle SONET data.

Selection Guide

Model	EVAL-ADNSFP-SE	EVAL-ADNSFP-Diff	EVAL-ADNSFP-FC
Receive Section Max Data Rate ROSA TIA Limiting Amp LOS Range Protocols Supported	3.3G ADN2880ACPZ ADN2891ACPZ 3mV to 50mV SONET, 8B/10B	3.3G ADN2880ACPZ ADN2891ACPZ 3mV to 50mV SONET, 8B/10B	4.25G ADN2882ACPZ ADN2892ACPZ 3mV to 50mV 8B/10B
Transmit Section Max Data Rate Laser Control Laser Drive Circuit LDD Supported Lasers Protocols Supported Laser	4.25G Dual Loop Single Ended ADN2870ACPZ FP/DFB/VCSEL SONET, 8B/10B TBD	4.25G Dual Loop Single Ended ADN2870ACPZ FP/DFB/VCSEL SONET, 8B/10B TBD	4.25G Dual Loop Differential ADN2870ACPZ FP/DFB/VCSEL SONET, 8B/10B AOC 5962-581
Supervisor Supervisor	ADuC7020ACPZ	ADuC7020ACPZ	ADuC7020ACPZ
Recommended Usage			
OC-3 to OC-48 Single Rate Modules			
OC-3 to OC-48 Multi Rate Modules	\checkmark		
1GE Modules		\checkmark	
1X/2X/4X Fiber Channel Modules			
LX4 Modules	√*	<u>√*</u>	
DWDM SFP	$\sqrt{*}$	$\sqrt{*}$	

 $\sqrt{10^{+1}}$ The SFP Reference Design can provide a performance benchmark for these types of modules.

The Analog Devices SFP Reference Design is available in several configuration depending on the end application. The primary differences are related to the speed of the receive section, and the configuration of the laser driver interface circuit.

Receive Section:

-SE and -Diff versions are design to work with SONET data at rates less than 3.3G; they will also support 8B/10B encoded data. -FC version features a limiting amp and TIA that support rates up to 4.25G and 8B/10B encoded data. The limiting amplifier in the -FC version (ADN2892) has a BW select feature to improve sensitivity for 1X FC and 1GE data rates, and can filter relaxation oscillations from legacy CD lasers used in older fiber channel modules.

Transmit Section

The –SE version has a typical single ended drive circuit. The differential driver circuit in the –Diff and –FC versions can produce superior transmit eye quality by improving fall times to increase eye margin. This is particularly important when driving VCSELs that can have slow fall time performance. All three boards will support FP/DFP or VCSEL lasers.

Module Board Optical Edge Pad Dimensions and Placement

Viewed from ROSA/TOSA to board edge. All dimensions are in millimeters



Figure 2. Edge pin configuration PC Board V1.3 (EVAL-ADNSFP-SE)



Figure 3. Edge pin configuration PC Board V1.4 (EVAL-ADNSFP-Diff/-FC)

Board Outlines



Figure 4. SFP Host Board



Figure 5. SFP Module Board V1.3 (Top side)



Figure 6. SFP Module Board V1.3 (Bottom side)



Figure 7. SFP Module Board V1.4 (Top side)



Figure 8. SFP Module Board V1.4 (Bottom side)

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Contents of SFP Reference Design Kit Package

The SFP-RDK package contains the following items.

- SFP Module Board with TOSA and ROSA
- SFP Host Board
- GUI Adapter Board (RS232-to-I2C, ADuC7020-MiniEval)
- JTAG Adapter Board
- RS-232 Cable (MicroConverter Dongle Cable)
- Test Report
- CD containing:
 - Firmware source files
 - ➢ GUI software files
 - ➢ GUI driver files



SFP Reference Design Kit Package

SFP Reference Design Kit

GUI

al Port	DIAGNOSTIC MONITOR	ADuc?	020 Setup	ADN2870 Setup	temory A0 Memo	IN A2 EEPR	OM	
CLOSE	TEMPERATURE	-40	-20	0 20	40	60	80	+100
STOP	37.8 °C I⊽ Enable	Low Alam	0.25	Low Warning 10	High Warning 60	Hig	m 70	-
us/Control Bits	Vcc	0						6.5/
Disable V Tx Disable	3.27 V I⊽ Enable	Low Alam	3.1	Low Warning 3.2	High Warning 34	Hig Ala	h 36	
Rote Sel	TX LASER BIAS	0		2				131mA
Fault	IF Enable	Low Alam	20	Low 30 Warning	High Warning 50	Hig Ala	h 70	
to Ready	TX POWER	0						6.5nW
k status.	F Enable	Low Alam	0.1	Low Varning 0.2	High Warning 35	Hig Ala	h 4	-li
10) ok : real-time monitor 25] ok	RK POWER	0						6.5mW
C0] ok 7F] ok B0] ok 251 ok	Enable	Low Alam	0.01	Low Verning	High Warning 0.5	Hig Ala	h 1	i.
90 ok 14 ok 00 ok	AUK (TX LASER MO	OULATIC 0						131mA
00] ok 00] ok 68] ok	I Enable	Low Alam	-	Low Warning	High Warning	Hig Ala	h [

SFF-8472 Diagnostic Window

📽 Analog Devices - SFP Reference Designs Kit File Help Serial Port
OPEN
CLOSE DIAGNOSTIC MONITOR ADuC7020 Setup ADN2870 Setup Memory A0 Memory A2 EEPROM Average Power Calibra Monitor RUN STOP 606 DEC (0 - 4095) 369.7 mV Read Write Extinction Ratio Calibration Status/Control Bits Tx Disable S/W Tx Disable 739 DEC [0 · 4095] 450.8 mV Read Wile ER Compensation Setup Tx Fault Calibration (Loop must be disabled) Compensation Loop C Enable C Disable Read SETP 1 Store Imod/ERREF at Low Temp. ₩ Enable Parameters Slope 308- DEC -0.308 V/A loading slope read [01] ok read [34] ok read [03] ok read [38] ok offset data. SETP 2 Store Imod/ERREF at High Temp. Offset 827 DEC 504.5 mV Calculate Slope/Offset SETP 3 Read Tx Power Monitor Disable Enable ANALOG DEVICES

ADN2870 Setup Window

Serial Port	Dischartie Howiton: ADI/2009 Selan ADI/2009 Cate Harris 40 Harris 40 FC000H	
OPEN CLOSE	Elevent Time	
fonitor	D Read	
RUN STOP	A Hour Head	
Auto Bun	FLASH/EE Control	
itatus/Control Bits		
TxDisable	Execute Force Flash Update Execute Sutem Initialize	
S/W Tx Disable		
Rx Rate Sel		
S/W Rx Rate Sel	Temperature Sensor Calibration	
Tx Fault	Reference Temperature 25.00 T C* Read Write	
RxLOS		
Data Ready	ADC Code 1200 DEC (0 - 4095) Read Write	
I♥ Enable		
oading Temp ADC code		
rad [80] ok		
ANALOG		
DEVICES		

🗣 Analog Devices - SFP Reference Designe Kit File Help Serial Por DIAGNOSTIC MONITOR | ADuC7020 Setup | ADN2870 Setup | Memory A0 | Memory A2 | EEPROM | OPEN CLOSE Memory Contents at I2C Device Address A2 Monito
 D
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 E
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 1
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 RUN STOP Status/Control Bits Tx Disable SMT 8 0 **TxE** ABCDEF 🔽 Enable loading A2 data, read (45) ok, read (00) ok, read (FF) ok, read (FF) ok, read (00) ok, read (79) ok, Read 256-Byte read [18] ok read [84] ok ANALOG DEVICES

ADuC7020 Setup Window

A0h and A2h Memory Windows

Preliminary Technical Data



EEPROM Read and Write Window