ANALOG DEVICES

AN-1103
APPLICATION NOTE

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Layout Considerations for Digital Power Management (ADP1046)

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INTRODUCTION

The ADP1046 is a digital power controller. It is a secondary side controller featuring several analog-to-digital converters (ADCs) with different data conversion rates. It also has integrated I^2C communication, analog comparators, and digital compensation. For such complicated mixed signal devices where several input and output functions are present in a small 5 mm × 5 mm area, layout is crucial, and proper care must be taken to avoid layout hazards. It is better to address layout issues from the beginning to avoid complications and failures at a later stage in the design cycle or, much worse, in the field. This application note provides critical layout guidelines to avoid noise coupling as well as proper grounding techniques for the ADP1046.

MODES OF NOISE COUPLING AND HOW TO MINIMIZE THEM

Noise is predominantly a high frequency phenomenon. In the case of a switching power supply, high frequency denotes any frequency above 100 kHz where the higher order harmonics of significant amplitude can be as high as 1 MHz to 10 MHz. A low frequency noise is generally not considered detrimental to the proper functioning of the circuit and is characterized in the order of a few hertz (Hz), for example, the output ripple of the boost power factor correction stage. In an electromagnetic circuit, there are four main causes of noise injection: common impedance coupling, capacitive coupling, inductive coupling, and radiation.

Common Impedance Coupling

Noise from common impedance coupling is introduced when the return trace of one loop connects to the trace of another loop and a common path is shared for the signal. For example, if one loop contains a high frequency (HF) signal (a noisy switching waveform), the other is a low frequency signal (quiet VDD signal), and both loops share the same return, noise can very easily be injected into the low frequency (LF) path due to the sharing of the common return. The voltage drop caused by the HF signal on the shared impedance is also seen by the LF loop. A star connection is the safest way to avoid this type of noise.

Capacitive Coupling

Noise from capacitive coupling is introduced when the signal traces are routed close to each other. Whenever a trace is routed close to another with high frequency dv/dt changes, noise is capacitively coupled due to stray capacitances between the two traces. This type of noise is modeled as a current source with high input impedance and affects low impedance nodes. Rerouting the signal traces is the only option available to reduce noise without adding external filtering components.

Inductive Coupling

Inductive coupling can be considered the opposite of capacitive coupling. Mutual inductance is the coupling mechanism for this type of noise. Reducing the loop area of high di/dt traces is crucial to reduce noise pickup.

Radiation

Noise from radiation is at very high frequencies (above 30 MHz). The switching nodes of a power supply where high di/dt transitions occur act as antennas, radiating noise, and can affect far fields and remote parts of the circuit. Using a six-frame Faraday shield or reducing the antenna effect is the best option (reducing copper area at noisy nodes).

PLACEMENT OF THE ADP1046

The ADP1046 is a secondary side controller. It must be placed in a location that is close to the output because the majority of the ADCs for sensing output voltage and current, as well as the PWM outputs that control the synchronous rectifiers, are present at the secondary side. However, the IC also provides PWM pulses for driving power switches placed on the primary side of the power supply. It also monitors and provides protection for primary signals such as primary current. Therefore, it cannot be placed too far away from the MOSFET drivers and the primary current sense transformer.

In a power supply layout, the switching elements (for example, MOSFETs, IGBTs) and their respective gate drivers must be close together. Placement of the ADP1046 should be done in a manner that does not degrade the PWM outputs or the sensing/measuring of the current and output voltages.

For prototyping and bench testing, it is highly recommended that the user lay out the ADP1046 on a small daughter card and connect it to the power board using external connectors (see the PRD1274). This layout allows easy monitoring of signals because the pins of the ADP1046 are easily accessible on the daughter card.

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REVISION HISTORY

4/12—Revision 0: Initial Version

ADP1046 LAYOUT AND GROUNDING

In mixed signal systems, the first step is to separate the analog and digital signals to reduce interference. Noise in the digital side can couple with the analog circuitry and severely interfere with the signal integrity. Grounding is very important in mixed signal systems and can be the major source of radiated noise in systems where several multipoint grounds are present. In the case of a power supply using the ADP1046, the system has three grounds: the power ground (PGND), the analog ground (AGND), and the digital ground (DGND). The proper grounding technique for the ADP1046 is to place a ceramic capacitor (330 nF/X7R) from VCORE to DGND. DGND must be connected to AGND with a star connection. An AGND plane can be created on the second layer of the PCB to prevent noise caused by the high speed ADCs and other digital circuitry from appearing on the analog side. A ground plane acts as a Faraday shield and terminates the noise signal to ground.

Layout engineers who prefer to use separate DGND planes must ensure that the AGND and DGND planes do not overlap because the analog and digital noise can easily couple from one ground plane to another. Instead, the AGND and DGND planes should be connected at a single point, and the planes must be separated by at least 3 mm to 6 mm using a 0 Ω resistor. This layout eliminates any ground bouncing and provides the IC with a clean ground reference.

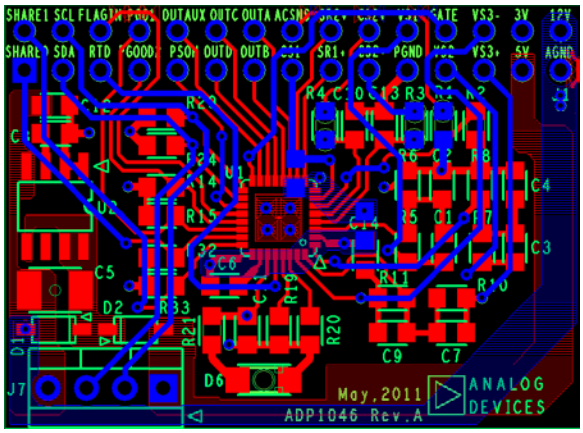

Figure 1. ADP1046 Daughter Card Layout

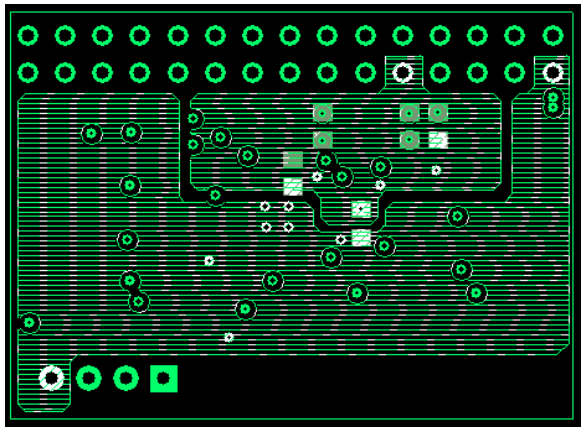

Figure 2. Single Point Connection Between PGND and AGND Using 0 Ω

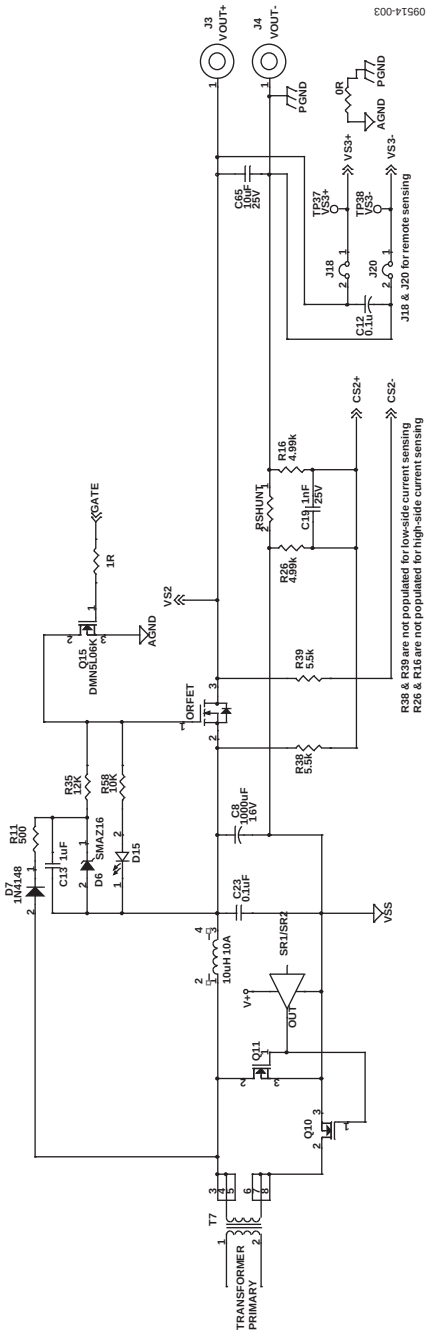

Figure 3. Typical PSU Secondary Side with Synchronous Rectifiers

The exposed pad of the IC must be connected to AGND. VCORE is referenced to DGND and VDD is referenced to AGND. All signals referenced to AGND and DGND must be connected to their respective grounds with vias to the second layer. Additionally, PGND and AGND must be tied together at a single point with a 0 Ω resistor (see Figure 2).

The return point of the synchronous rectifier drivers must be tied to VSS (see Figure 3) to minimize any inductance along its path.

Instead of following general guidelines, it is necessary to understand how a signal traces its path back to the source and then decide how to keep this loop area small.

LOCATION OF PGND

The location of PGND must be selected as the return point of the load (see Figure 3).

VS3 AND CS2 DIFFERENTIAL SENSING

VS3± and CS2± are the two differential inputs of the ADP1046. The recommended trace width is 15 mils to 20 mils.

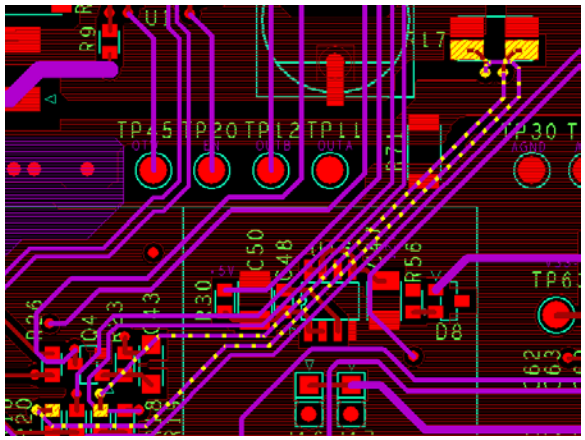

Figure 4. Parallel Traces of CS2+ and CS2− From Sense Resistor

The layout of these traces is not as critical as the layout of other signal traces because the same common-mode noise is seen across both the pins by virtue of differential sensing. VS3− is connected to PGND. The level shifting resistors for CS2 must be kept close to the IC (preferably on a daughter card if a daughter card is used). It is recommended that the traces for the differential VS3± inputs be run parallel to each other.

It is recommended that a 100 nF/X7R capacitor be placed between VS3− and AGND to reduce common-mode noise. The recommended location of this capacitor is on a daughter card close to the IC rather than on the PCB.

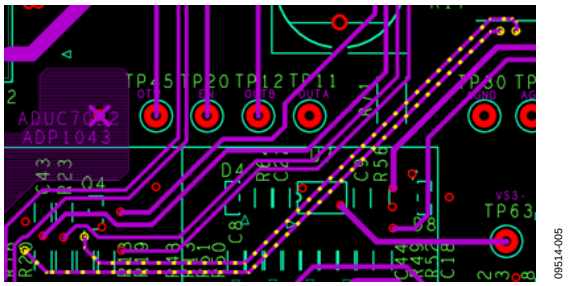

Figure 5. VS3+ and VS3− Traces

VS1, VS2, VS3− SENSING

VS1, VS2, and VS3− must be referenced to PGND.

The ADCs connected at the output of the PSU are generally far from the switching nodes of a power supply. The only way they are affected is due to the switching ripple. The ADP1046 uses sigma-delta (Σ-Δ) ADCs at 1.6 MHz and 25 MHz, which have superior noise cancellation at lower frequencies due to their internal oversampling architecture. However, the traces for VS1 and VS2 must still be routed as far as possible from any dv/dt or di/dt traces or nodes that have high transients present on them.

RES PIN

Connect a 10 kΩ/0.1% resistor from the RES pin to AGND with a via close to the IC. The tolerance of the internal clock frequency is directly proportional to the accuracy of the RES pin resistor and, therefore, a 0.1% resistor is recommended.

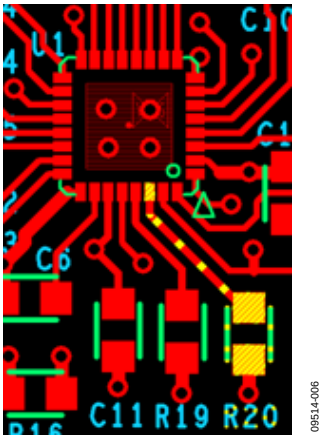

Figure 6. RES Pin, R20 = 10 kΩ

CS1 PIN

The CS1 pin (referenced to PGND), which monitors the primary current, has a fast and accurate form of protection. An internal comparator provides fast overcurrent protection (OCP), and this analog signal must be routed away from the MOSFET drivers or PWMs that have high frequency pulses. A 1 nF capacitor is recommended to be placed between the CS1 pin and PGND, as shown in Figure 8. The primary current is sensed by converting it into a voltage across a termination resistor on the secondary side of the current transformer (CT). The trace from the CT secondary to the CS1 pin is long due to the placement of the IC. Placing the termination resistor close to the CT automatically degrades the voltage across the trace (but the loop area is shorter and inductive noise is suppressed). A damping resistor of much higher value can be placed across the secondary side of the CT to shorten the loop, and the termination resistor can be placed as close to the CS1 pin as possible. There is no signal degradation due to the signal being a current signal.

Due to the distance from the primary to the CS1 pin, the recommended trace width is 30 mils. Because the absolute maximum rating of the CS1 pin is 3.3 V (cycle by cycle OCP limit at 1.2 V), it is recommended that a 2.5 V Zener diode be connected in parallel with the termination resistor. An additional diode with low forward voltage drop can also be placed in parallel to prevent the pin from being pulled to less than −0.3 V.

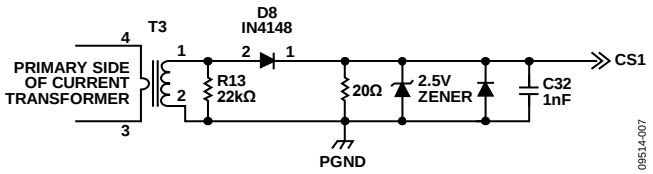

Figure 7. Typical Circuit for Primary Current Sensing with 1 nF Placed Close to the IC (Preferably on Daughter Card)

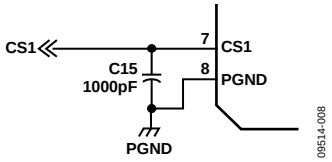

Figure 8. CS1 Filtering Capacitor Placed Close to the Pins of the IC

ACSNS PIN

The ACSNS pin is referenced to PGND. The pickup point for ACSNS is the switching node on the secondary side of the power transformer. This pin is used to detect the presence of switching (short D10 and R55, and open C25) or for line feedforward.

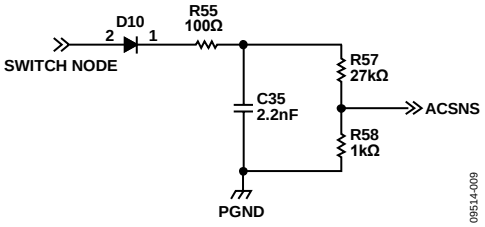

Figure 9. Typical Application Circuit for Line Feedforward

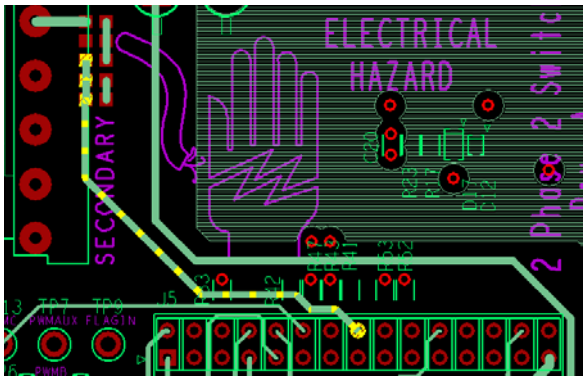

Figure 10. ACSNS Trace from Switch Node

PSON PIN

PSON is referenced to AGND. A 1 nF capacitor is recommended from PSON to AGND.

POWER TRACES (VDD AND VCORE PINS)

The VDD pin of the ADP1046 has a maximum input voltage of 3.6 V (typically 3.3 V), and the digital core 2.5 V is fed through an internal regulator. Although the IC consumes ~20 mA, the power traces to the VDD pin must be as short as possible. This is done to avoid any degradation due to the inductance of the trace that may cause noise on the rail. It is best wherever possible to shorten the length of the power traces rather than increasing their width to reduce the inductance. Preferably, the ground plane should be directly below the power traces so that the return path is shortened (loop is small).

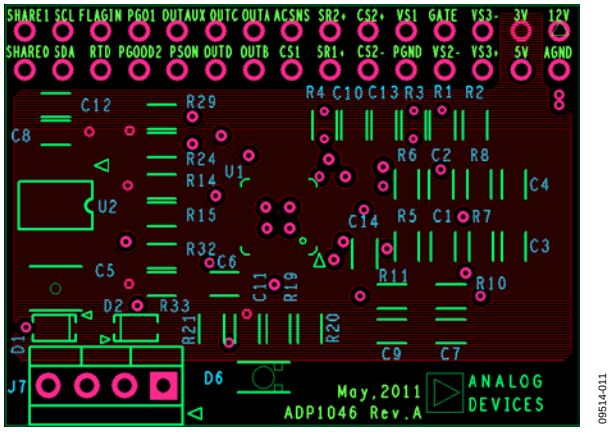

Figure 11. Power VDD Trace

DECOUPLING CAPACITORS

The use of bypass or decoupling capacitors is a common and proven technique for reducing noise on a pin. The supply pins, VDD and VCORE, are especially prone to noise because they are low impedance nodes. The recommended capacitor values for VDD and VCORE are 4.7 µF and 300 nF, respectively (X7R). Additionally, note that inductive noise can severely affect these pins, and the capacitor must be placed very close to the pin with minimal loop area.

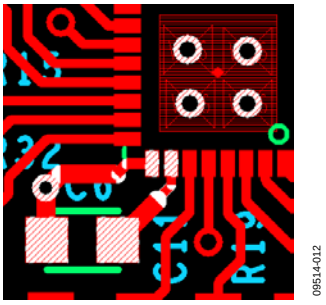

Figure 12. 330 nF Capacitor Connected Close to VCORE and DGND

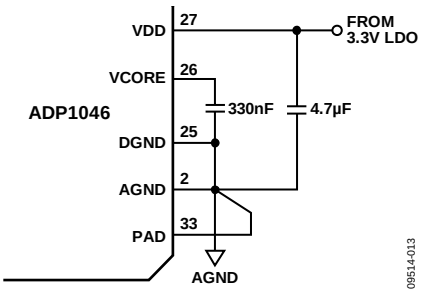

Figure 13. Small Loop Areas for Bypass Capacitors on VDD and VCORE

OUTA TO OUTD, SR1, AND SR2 PWM OUTPUTS

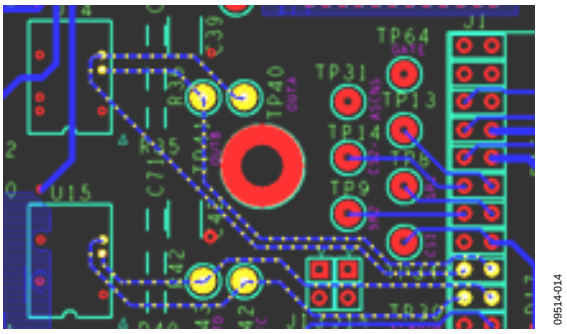

Figure 14. OUTA to OUTD Traces to MOSFET Drivers

All the PWM outputs (OUTA to OUTD, SR1, SR2, and OUTAUX) are referenced to AGND. Like the differential traces, the PWM and SR traces must also be run parallel to each other (recommended trace width of 15 mils), and the spacing must be kept uniform to ensure a constant differential impedance to avoid crosstalk (capacitive coupling) and signal integrity. The spacing between traces should be equal to or greater than the trace width.

The PWM traces are the controlling signals of a PSU, and because they contain high frequency information, it is best to keep the traces short to avoid degradation due to trace inductance and spikes. It is critical to choose the proper location of the ADP1046 initially to make sure that these critical signals are not compromised. Figure 15 shows a noise-affected PWM pulse due to improper layout that can be detrimental to the overall functionality of the system.

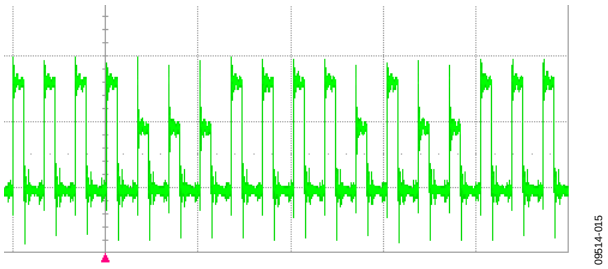

Figure 15. Noise-Affected PWM Pulse (2 V/DIV)

The SR driver must be referenced to the true floating output of the PSU, that is, the return of the transformer (VSS in Figure 3) and not to PGND. This is important because SR drivers are typically powered from the output rail (for 12 V applications or from an auxiliary power supply). This prevents the return path from including the current sense resistor. In addition, such placement of the driver IC ensures that the complete gate-source drive capability of the driver IC appears across the gate-source terminals of the FET with minimal loop area.

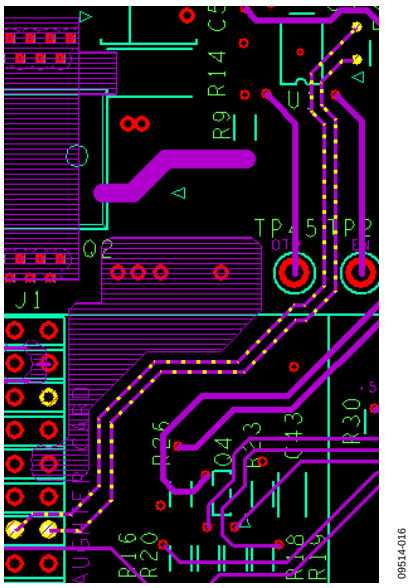

Figure 16. SR1 and SR2 Parallel Running Traces Separated by 15 mils to SR Driver

GATE PIN

The GATE pin (referenced to AGND) is a totem pole output (configurable polarity using the GUI) without any pull-up resistor. The GATE pin provides the signal for turning on/off the OrFET for reverse current protection. This trace must be kept as short as possible and routed away from the synchronous driver switch nodes.

RTD PIN

The RTD pin sources a constant current and is an analog signal. This signal is difficult to route because the power transistors are the parts under the greatest thermal stress. Do not terminate the thermistor with a via to the AGND plane; instead, use a dedicated trace back to the AGND pin. The recommended trace width is 30 mils. The 16.5 kΩ in parallel with the thermistor allows the ADP1046 to read the temperature in °C.

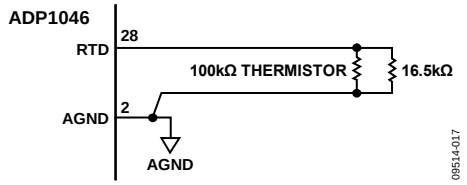

Figure 17. Correct: Dedicated Trace to AGND

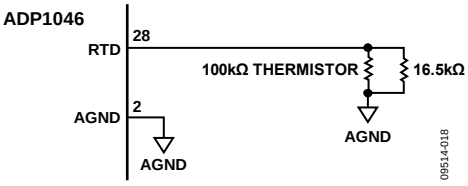

Figure 18. Incorrect: Thermistor Terminated to AGND Through AGND Plane

PGOOD1, PGOOD2, AND FLAGIN PINS

PGOOD1, PGOOD 2, and FLAGIN are all referenced to AGND. PGOOD1 and PGOOD2 are small signal traces for visual monitoring through LEDs. They should be routed after all the other important traces are finalized. FLAGIN can be routed along with the PGOOD signals.

SHAREo AND SHAREi PINS

The SHAREo and SHAREi pins are open drain. The pull-up resistors (2.2 kΩ) for analog and digital current sharing must be kept close to the IC.

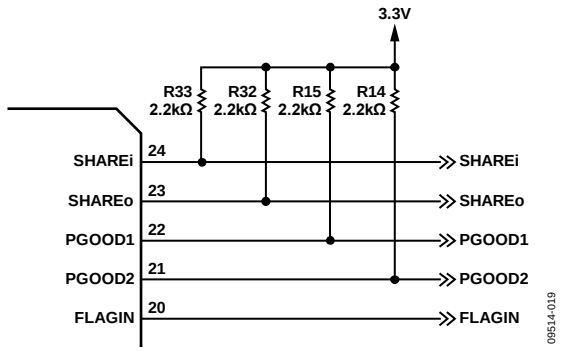

Figure 19. Pull-Up Resistors Close to IC

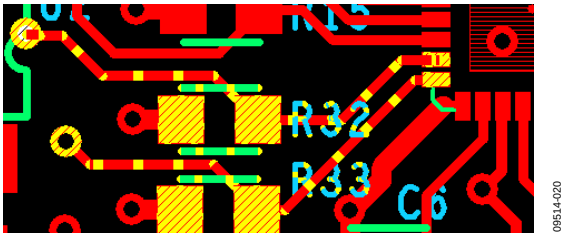

Figure 20. Pull-Up Resistors Close to IC

SDA AND SCL PINS (I²C CLOCK AND DATA)

The SDA and SCL pins are referenced to AGND. Because SDA and SCL are communication lines, extra effort must be taken to route them so that the shortest possible length is achieved to eliminate noise pickup from surrounding traces (long traces act as antennas). It is recommended that these traces be surrounded by the ground plane. In addition, a filtering circuit (see Figure 21) is used to prevent communication errors. A minimum trace width of 30 mils is good practice.

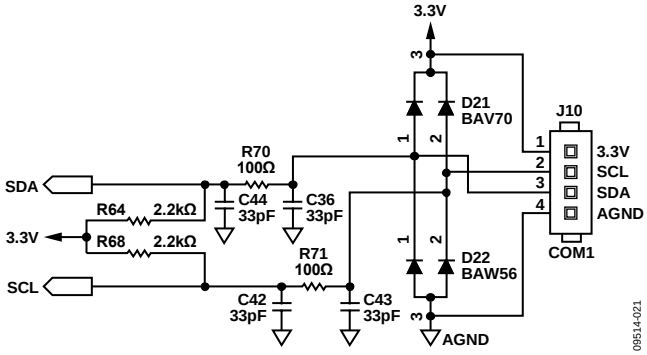

Figure 21. Filtering Circuit for I²C Communication

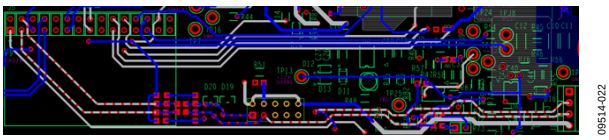

Figure 22. Example of I²C Communication Traces

CLEARANCE AND CREEPAGE REQUIREMENTS

The ADP1046 is located on the secondary (isolated) side of the power supply. The primary signals (OUTx and CS1) are fed either to an isolated driver or to a current transformer (CT). These components by themselves are designed to meet the required creepage and clearance isolation requirements. Additional safety requirements are not required while routing.

CONCLUSION

Using the autorouting feature may not produce the optimal layout, but other tools that layout programs provide, such as a transmission line calculator and router checks, can be useful as a final check.

Identify the sources of noise, type of noise, and effective coupling method, and separate analog and digital signals.

Proper routing can eliminate the need for external shielding. It is better to minimize the noise at the source than to use corrective measures to fix layout issues later.

Use small loop areas and avoid routing through high dv/dt lines. The recommended trace widths can be scaled for high power density power supplies in the case of modules (dc-to-dc bricks).

Use the recommended resistor values (RES pin) and capacitor values (VDD and VCORE pins).

Long traces can act as antennas; therefore, terminate to AGND plane wherever possible (except for RTD traces)

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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