

# AN-1383 **Application Note**

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### ADP1046A EEPROM Programming

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#### INTRODUCTION

The ADP1046A offers a register map and an EEPROM that are programmed with settings for a specific power topology and application based on the user system preferences. This application note focuses on the hardware considerations and software procedures to program the ADP1046A in a production line environment.

#### HARDWARE

Figure 1 shows the recommended pin settings for the ADP1046A in the EEPROM programming environment. Use surfacemount components for all components. In addition, ceramic capacitors are recommended.

#### **RECOMMENDED PIN SETTINGS**

Table 1 Common and Cotting

Table 1 lists the settings for the components shown in Figure 1.

Table 1. Component Settings				
Component Value Unit		Unit	Comments	
VDD Pin	3.3	V		
GND <sup>1, 2</sup>			Ground plane of the board	
NC			No connect pin; leave this pin floating	
C1	0.5	μF	Capacitor 1	
C2, C3	2.5	μF	Capacitor 2, Capacitor 3	
R1, R2	5	kΩ	Resistor 1, Resistor 2	
R3, R4	2.2	kΩ	Resistor 3, Resistor 4	
R5	10	kΩ	Resistor 5, 0.1% accurate	
R6, R7	10	Ω	Optional resistors	

<sup>1</sup> One continuous ground plane must be present across the entire area of the board.

<sup>2</sup> To avoid noise interference, the SDA, SCL, and GND lines from the programmer to the device must be as small as possible.



T vdd Х́мс 

Figure 1. Recommended Pin Settings

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### **REVISION HISTORY**

6/2016—Revision 0: Initial Version
Changes to Figure 5 and Board Settings Hexadecimal
File Section

2/2016—Revision 0: Initial Version

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### ADDITIONAL LAYOUT RECOMMENDATIONS

If the ADP1046A is soldered on the board, then the components listed in Table 1 must be close to the pins, as shown in Figure 4. If a socket is used, place the components on the bottom side of the board near the pins, as shown in Figure 2.



Figure 2. Board Layout



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Figure 3. Board Layout, Bottom View



Figure 4. Board Layout, IC on Board

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### SOFTWARE PROGRAMMING

There are two methods for programming register settings into the EEPROM of the device: standard or alternative.

### STANDARD EEPROM PROGRAMMING

To program the register settings into the EEPROM using the standard method, take the following steps:

- 1. Read the register settings from the ".46r" file that is generated using either the ADP1046A graphical user interface (GUI) or a hex file and write the following register values to the corresponding registers of the device via I<sup>2</sup>C:
  - a. Write to Register 0x08 to Register 0x0F
  - b. Write to Register 0x22
  - c. Write to Register 0x26 to Register 0x2A
  - d. Write to Register 0x2C to Register 0x37
  - e. Write to Register 0x3B
  - f. Write to Register 0x3F to Register 0x5D
  - g. Write to Register 0x5F to Register 0x7D
- 2. Read back the values written and compare them to the register settings in the .46r file to ensure the write operation was executed correctly.
- 3. To unlock the EEPROM, a repeated write is required to Register 0x88. First, write 0xFF to Register 0x88 and then immediately write 0xFF to Register 0x88 again.
- 4. To upload the contents in the registers to the EEPROM, execute a send command to Register 0x82.
- 5. Wait for 50 ms for the upload to complete.
- 6. To lock the EEPROM, write 0x01 to Register 0x88.

### ALTERNATIVE EEPROM PROGRAMMING

To program the board settings into the EEPROM using the alternative method, take the following steps and see Figure 5:

- 1. To unlock the EEPROM, a repeated write is required to Register 0x88. First, write 0xFF to Register 0x88 and then immediately write 0xFF to Register 0x88 again.
- 2. Erase EEPROM Page 2 by writing 0x02 to Register 0x87; wait 30 ms to for the erase to complete.
- 3. Set the address offset to zero by writing 0x0000 to Register 0x85.
- 4. Write to EEPROM Page 2 by performing a block write to Register 0x8D using the board data from the hexadecimal file.
- 5. Unlock the EEPROM by writing 0x01 to Register 0x88.

#### Example Using Hexadecimal File



Figure 5. EEPROM Alternative Programming Using Hexadecimal File

#### **Board Settings Hexadecimal File**

The hexadecimal file reads as follows:

Note the following information that is embedded in the file format:

- The first two digits after the colon, 7E, represent the byte count. In this case, it is 126 bytes.
- The next four digits, 008D, represent the address.
- The next two digits, 00, represent the record type.
- The remaining digits, beginning with 0102036 and ending with the final string of 36 zeros, represent the data.
- The final two digits, 7E, represent the checksum.

# FORMAT FOR STORING BOARD SETTINGS IN EEPROM

The data that is written to the EEPROM for board settings starts with 0x010203, it is used by the graphical user interface (GUI) to detect if valid board settings data is present in Page 2 of the EEPROM.

Each board setting is represented as three-byte data in the hexadecimal file. The first two bytes represent the mantissa and the third byte represents the exponent. For example, the first board setting, input voltage of 48 V, is represented as 0x6000F7. To understand the breakdown of the hexadecimal code, see Table 2.

#### Table 2. Hexadecimal Code Segments

Man		
High Bits	Low Bits	Exponent
0x60	0x00	0xF7

#### **Converting Hexadecimal Data to Board Settings**

- Mantissa = 0x6000
- Mantissa in decimal = 24,576
  - Exponent = 0xF7
- Exponent after twos complement = -9
- Input voltage =  $24,576 \times 2^{-9} = 48$  V

Figure 6 shows the ADP1046A GUI window with the board settings. These settings are further defined in Table 3 where the Item column represents the component locator numbers within Figure 6.



Figure 6. ADP1046A GUI Window with Board Settings

### Table 3. Component Values for Board Settings

		Mantissa		
ltem	Board Value	High Bits	Low Bits	Exponent
1	Input voltage = 48 V	0x60	0x00	0xF7
2	N1 = 6	0x60	0x00	0xF4
3	N2 = 3	0x60	0x00	0xF3
4	$R(CS2) = 11 m\Omega$	0xB0	0x00	0xF4
5	I (load) = 8 A	0x80	0x00	0xF4
6	$R1 = 11 k\Omega$	0xB0	0x00	0xF4
7	$R2 = 1 k\Omega$	0x80	0x00	0xF1
8	C3 = 1 µF	0x80	0x00	0xF1
9	C4 = 1 μF	0x80	0x00	0xF1
10	N1 (CS1) = 1	0x80	0x00	0xF1
11	N2 (CS1) = 100	0x64	0x00	0xF8
12	$R(CS1) = 10 \Omega$	0xA0	0x00	0xF4
13	$\text{ESR}(L1) = 6 \text{ m}\Omega$	0x60	0x00	0xF4
14	L1 = 6 μH	0x60	0x00	0xF4
15	C1 = 1500 μF	0x5D	0xC0	0xFC
16	$\text{ESR}(\text{C1}) = 50 \text{ m}\Omega$	0x64	0x00	0xF7
17	$\text{ESR}(\text{L2}) = 0 \text{ m}\Omega$	0x00	0x00	0x00
18	$L2 = 0 \mu H$	0x00	0x00	0x00
19	$C2 = 220 \mu\text{F}$	0x6E	0x00	0xF9
20	$\text{ESR}(\text{C2}) = 20 \text{ m}\Omega$	0xA0	0x00	0xF5
21	R (normal mode) = $1.5 \Omega$	0x60	0x00	0xF2
22	R (light load mode) = $12 \Omega$	0x60	0x00	0xF5
23	Capacitor across R1 and R2 = 0 $\mu$ F	0x00	0x00	0x00
24	Topology = 0	0x00	0x00	0x00
25	Switches/diodes = 0	0x00	0x00	0x00
26	High-side/low-side sense (CS2) = $0 \text{ m}\Omega$	0x00	0x00	0x00
27	Second LC stage = 1 (only when Item 17 to Item 20 are populated)	0x80	0x00	0xF1
28	CS1 input type = 0 (default value for internal use)	0x00	0x00	0x00
29	$R3 = 0 k\Omega$	0x00	0x00	0x00
30	$R4 = 0 k\Omega$	0x00	0x00	0x00
31	Pulse-width modulator (PWM) main = 0 (default value for internal use)	0x00	0x00	0x00
32	$C5 = 0 \mu F$	0x00	0x00	0x00
33	$C6 = 0 \mu F$	0x00	0x00	0x00
34	$R6 = 27 k\Omega$	0x6C	0x00	0xF6
35	R7 = 1 kΩ	0x80	0x00	0xF1

#### Resonant Mode Topology

For resonant mode topology (Figure 7), the additional components require different settings than the general board settings listed in Table 3. The resonant mode settings are listed in Table 4.

Table 4. Resonant Mode Components

ltem	Board Value
1	Input voltage = 385 V
2	N1 = 6
3	N2 = 3
4	$R(CS2) = 2.2 m\Omega$
5	l (load) = 12.5 A
6	$R1 = 46.4 \text{ k}\Omega$
7	$R2 = 1 k\Omega$
8	$C3 = 1 \mu F$
9	$C4 = 1 \mu F$
10	N1 (CS1) = 1
11	N2 (CS1) = 100
12	$R(CS1) = 20 \Omega$
13	ESR (L1) = 6 m $\Omega$
14	L1 = 6 µH
15	C1 = 680 µF
16	ESR (C1) = 50 m $\Omega$
17	$\text{ESR}(\text{L2}) = 0 \text{ m}\Omega$
18	$L2 = 0 \mu H$
19	C2 = 330 µF
20	ESR (C2) = 20 m $\Omega$
21	R (normal mode), load = 3.84 $\Omega$
22	R (light load mode), load = 24 $\Omega$
23	Capacitor across R1 and R2 = 0 (1 = yes, $0 = no$ )
24	Topology = 7 (0 = full bridge, 1 = half bridge, 2 = two switch forward, 3 = interleaved two switch forward, 4 = active clamp forward, 5 = resonant mode, $6 = custom$ )
25	Switches/diodes = 0 (0 = switches, 1 = diodes)
26	High-Side/Low-Side Sense (CS2) = 0 (1 = high-side sense, 0 = low-side sense)
27	Second LC stage = 1 (1 = yes, $0 = no$ )
28	CS1 input type = 0 (1 = ac, $0 = dc$ )
29	$R3 = 0 k\Omega$
30	$R4 = 0 k\Omega$
31	Pulse-width modulator main = 0 (0 = OUTA, 1 = OUTB, 2 = OUTC, 3 = OUTD, 4 = SR1, 5 = SR2, 6 = OUTAUX)
32	$C5 = 0 \ \mu F$
33	$C6 = 0 \ \mu F$
34	$R6 = 27 k\Omega$
35	$R7 = 1 k\Omega$
36	$C7 = 0.009 \mu\text{F}$
37	L3 = 70 μH
38	$Lm = 400 \ \mu H$
39	ResF = 108 kHz
40	$R8 = 145 \text{ m}\Omega$
41	$R9 = 10 \text{ m}\Omega$

# **Application Note**



Figure 7. ADP1046A GUI Window with Board Settings for Resonant Mode

#### Phase Shifted, Full Bridge Topology

For phase shifted, full bridge topology (Figure 8) the additional components require different settings than either the general board settings (Table 3) or the resonant mode settings (Table 4). The phase shifted, full bridge settings are listed in Table 5.

Table 5. Phase Shifted Full Bridge Components

ltem	Board Value
1	Input voltage = 385 V
2	N1 = 6
3	N2 = 3
4	$R(CS2) = 2.2 m\Omega$
5	l (load) = 12.5 A
6	$R1 = 46.4 \text{ k}\Omega$
7	$R2 = 1 k\Omega$
8	C3 = 1 µF
9	C4 = 1 µF
10	N1 (CS1) = 1
11	N2 (CS1) = 100
12	$R(CS1) = 20 \Omega$
13	$\text{ESR}(L1) = 6 \text{ m}\Omega$
14	L1 = 6 μH
15	C1 = 680 μF
16	$\text{ESR}(\text{C1}) = 50 \text{ m}\Omega$
17	$\text{ESR}(L2) = 0 \text{ m}\Omega$
18	$L2 = 0 \mu H$
19	C2 = 330 μF
20	$\text{ESR}(\text{C2}) = 20 \text{ m}\Omega$
21	R (normal mode), load = 3.84 $\Omega$
22	R (light load mode), load = 24 $\Omega$
23	Capacitor across R1 and R2 = 0 (1 = yes, $0 = n_0$ )
24	Topology = 1 (0 = full bridge, 1 = half bridge, 2 = two switch forward, 3 = interleaved two switch forward,
	4 = active clamp forward, $5 = $ resonant mode, $6 = $ custom)
25	Switches/diodes = 0 ( $0 = $ switches, $1 = $ diodes)
26	High-side/low side sense (CS2) = 0 (1 = high-side sense,
	0 = low-side sense)
27	Second LC stage = 1 (1 = yes, $0 = no$ )
28	CS1 input type = 0 (1 = ac, $0 = dc$ )
29	$R3 = 0 k\Omega$
30	$R4 = 0 k\Omega$
31	PWM main = 0 (0 = OUTA, 1 = OUTB, 2 = OUTC, 3 = OUTD, 4 = SR1, 5 = SR2, 6 = OUTAUX)
32	$C5 = 0 \mu F$
33	C6 = 0 µF
34	$R6 = 27 k\Omega$
35	$R7 = 1 k\Omega$
36	$C7 = 0.009 \mu\text{F}$
37	$L3 = 70 \ \mu H$
38	Lm = 400 μH
39	ResF = 108 kHz
40	$R8 = 145 \text{ m}\Omega$
40	$R9 = 10 m\Omega$

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Figure 8. ADP1046A GUI Window with Board Settings for Phase Shifted, Full Bridge Topology

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