Wide Input Range, Full Bridge Phase Shifted topology using ADP1046A

48V/600W

PRD1404

FEATURES

600W Phase Shifted Full Bridge Topology
Wide Input Range to minimize hold up capacitor
Wide ZVS range down to 10% rated load
Short circuit and Fast Over Voltage protection
Remote voltage sensing
Line voltage feedforward
I2C serial interface to PC
Software GUI
Programmable digital filters for DCM and CCM
7 PWM outputs including Auxiliary PWM
Digital Trimming
Current, voltage, and temperature sense through GUI
Calibration and trimming

CAUTION

This evaluation board uses high voltages and currents. Extreme caution must be taken especially on the primary side, to ensure safety for the user. It is strongly advised to power down the evaluation board when not in use. A current limited power supply is recommended as input as no fuse is present on the board.

ADP1046A EVALUATION BOARD OVERVIEW

This evaluation board features the ADP1046A in a switching power supply application. With the evaluation board and software, the ADP1046A can be interfaced to any PC running Windows 2000/XP/Vista/NT/7 via the computer's USB port. The software allows control and monitoring of the ADP1046A internal registers. The board is set up for the ADP1046A to act as an isolated switching power supply with a rated load of 48V/12.5A from an input voltage ranging from a 340VDC to 400VDC.

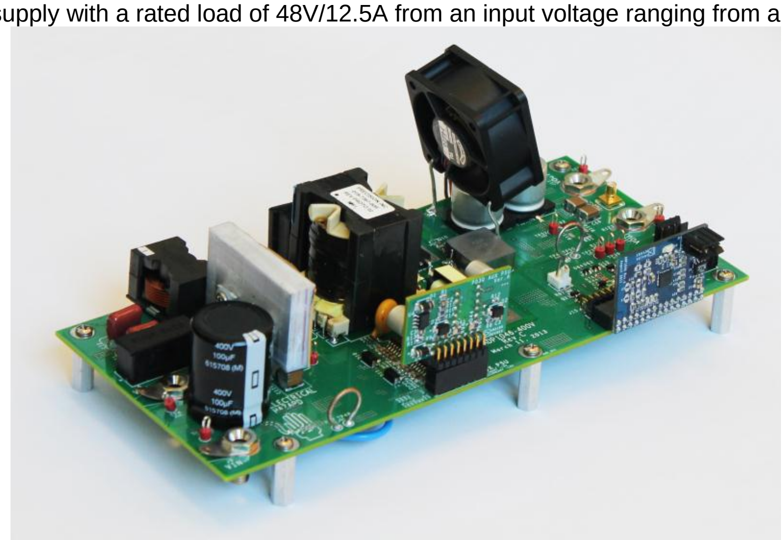

Figure 1 – Prototype

Rev. 1.0

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REVISION HISTORY

04/28/2013—Revision 1.0: SPM
05/02/2013—Revision 2.0: SPM

BOARD SPECIFICATIONS

Specification	*MIN*	*TYP*	*MAX*	*Units*	*Notes*
V_{IN}	340	385	400	V	
V_{OUT}		48		V	
I_{OUT}	0.0	12.5	15	A	With 400 LFM air flow.
Overload current (OCP limit)			15	A	OCP set to shutdown PSU after~10ms
Efficiency		96.35%		%	Typical reading at 385Vin, 12.5A load
Switching frequency		111.6		KHz	
Output Voltage Ripple		550		mV	At 12.5A load

Table 1 - Target Specifications

TOPOLOGY AND CIRCUIT DESCRIPTION

This application note consists of the ADP1046A in a typical isolated DC/DC switching power supply in a full bridge phase shifted topology with synchronous rectification. The circuit is designed to provide a rated output load of 48V/12.5A from a nominal input voltage of 385VDC operated in CCM at all times. The ADP1046A is can provide functions such as the output voltage regulation, output over voltage protection, input and output current protection, primary cycle by cycle protection, and over temperature protection. *Figure 70* provides a top level schematic that describes the power flow and auxiliary power supply that starts up at 50VDC and provides power to the ADP1046A through a 3.3V LDO, the iCoupler isolation plus gate drivers, the on board fan, and the synchronous rectifier drivers. The transformer is designed to provide a wide input voltage range (340-410VDC) and the circuit has wide ZVS (Zero Voltage Switching) range down to 10% of the rated load.

The auxiliary power supply using transformer (T3) and IC (U10) generates a 12V rail on the primary side and a 13V rail on the secondary side to power the iCoupler isolation devices (MOSFET drivers), synchronous rectifier driver and the ADP1046A using the 3.3V LDO. This auxiliary supply starts up at approximately 50VDC.

The primary side consists of the input terminals (JP8, JP9), switches (Q1-Q4), the current sense transformer (T5) and the main transformer (T1). There is also an resonant inductor that aids in zero voltage switching at lighter load conditions. The ADP1046A is situated on the secondary side and is powered via the auxiliary power supply or the USB connector via the LDO. The gate signal for the primary switches is generated by the ADP1046A through the iCouplers and fed into the MOSFET drivers (U17, U18). Bypass capacitors (C71, C72, C114-116) are placed closed to the primary switches. Diodes (D36-37) clamp the resonance between the resonant inductor and the output capacitance (COSS) of the output rectifiers.

The secondary (isolated) side of the transformer consists of a center tapped winding. The synchronous rectifier driver (U7) provides the drive signals for the switches (Q9, Q23). The output inductor (L8) and output capacitor (C11, C41) act as a low pass filter for the output voltage. The output voltage is fed back to the ADP1046A using a voltage divider and has a nominal voltage of 1V which is differentially sensed. Output current measured using a sense resistor (R2) which is also differentially sensed. To protect the synchronous rectifiers from exceeding the peak reverse voltage an RCD clamp is implemented (D58, D59, R112-115, C94)

The primary current is sensed through the CS1 pin with a small RC time constant (R44, C22) that act as a low pass filter to remove the high frequency noise on the signal. An additional RC can be placed, but the internal Σ-Δ ADC naturally averages the signal. The position of the current transformer is placed in series with the resonant inductor to avoid saturation.

Line voltage feedforward is implemented using an RCD circuit (D13, R59, R64, C38, C43) that detects the peak voltage at the synchronous FET. There are two time constants that can be implemented in series with each other. The time constants must be matched such that it retains the peak value during the switching frequency period but also is not too long in case there is a step down change in the input voltage. This peak voltage is further ratioed and fed in the ACSNS pin of the controller (ADP1046A). A thermistor (RT1) is placed on the secondary side close to synchronous FET and acts thermal protection for the power supply. A 16.5k resistor is placed in parallel with the thermistor that allows the software GUI to read the temperature directly in degrees Celsius.

Capacitor (C69) is a YCAP that reduces common mode noise from the transformer.

Also present on the secondary is a 4 pin connector for I2C communication. This allows the PC software to communicate with the IC through the USB port of the PC. The user can easily change register settings on the ADP1046A, and monitor the status registers. It is recommended that the USB dongle be connected directly to the PC, not via external hub.

Switch (SW2) acts as a hardware PS_OFF switch. The polarity is configured using the GUI to be active high.

CONNECTORS

The following table lists the connectors on the board:

Connector	Evaluation Board Function
J8	DC Input positive terminal
J9	DC Input negative terminal
J11	Output voltage positive terminal
J12	Output voltage negative terminal
J16	Socket for auxiliary power supply
J18	I2C connector

Table 2 - Board connectors

The pin outs of the USB dongle are given below:

Figure 2 – I2C connector (pin1 on left)

Pin (left to right)	Function
1	5V
2	SCL
3	SDA
4	Ground

Table 3 - I2C connector pin out descriptions

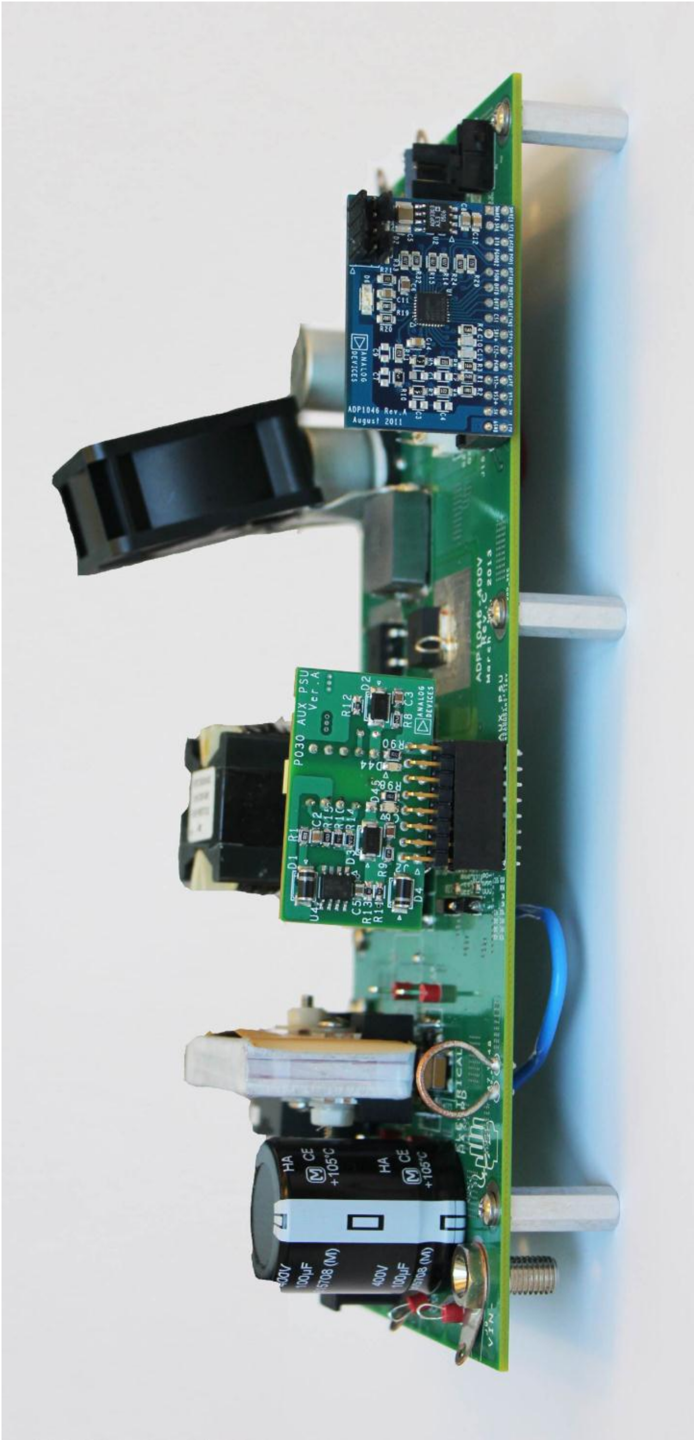

Figure 3 – PCB Side View

Figure 4 – PCB (top)

SETTING FILES AND EEPROM

The ADP1046A communicates with the GUI software using the I2C bus.

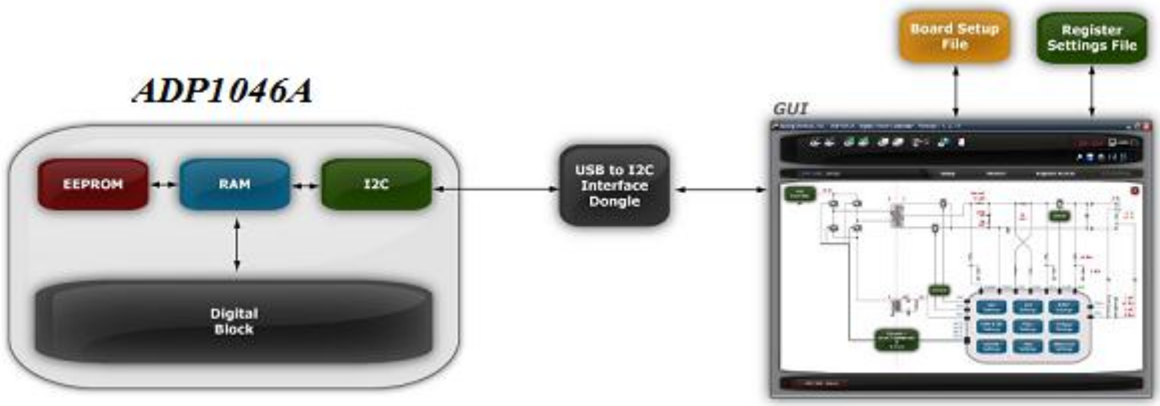

Figure 5 - ADP1046A and GUI interaction

The register settings (having extension .46r) and the board settings (having extension .46b) are two files that are associated with the ADP1046A software. The register settings file is contains information such as the over voltage and over current limits, softstart timing, PWM settings etc. that govern the functionality of the part. The ADP1046A stores all its settings in the EEPROM.

The EEPROM on the ADP1046A does not contain any information about the board, such as current sense resistor, output inductor and capacitor values. This information is stored in board setup file (extension .46b) and is necessary for the GUI to display the correct information in the ‘Monitor’ tab as well as ‘Filter Settings’ window. The entire status of the power supply such as the ORFET and synchronous rectifiers enable/disable, primary current, output voltage and current can be thus digitally monitored and controlled using software only. Always make sure that the correct board file has been loaded for the board currently in use.

Each ADP1046A chip has trim registers for the temperature, input current and the output voltage and current, and ACSNS. These can be configured during production and are not overwritten whenever a new register settings file is loaded. This is done in order to retain the trimming of all the ADCs for that corresponding environmental and circuit condition (component tolerances, thermal drift, etc.). A guided wizard called the ‘Auto Trim’ is started which trims the above mentioned quantities so that the measurement value matches the valued displayed in the GUI to allow ease of control through software.

BOARD EVALUATION

EQUIPMENT

• DC Power Supply (300-400V, 600W)

• Electronic Load (60V/600W)

• Oscilloscope with differential probes

• PC with ADP1046A GUI installed

• Precision Digital Voltmeters (HP34401or equivalent - 6 digits) for measuring DC current and voltage

SETUP

NOTE: DO NOT CONNECT THE USB CABLE TO THE EVALUATION BOARD UNTIL THE SOFTWARE HAS FINISHED INSTALLING

1) Install the ADP1046A software by inserting the installation CD. The software setup will start automatically and a guided process will install the software as well as the USB drivers for communication of the GUI with the IC using the USB dongle.
2) Insert the daughter card in connector J5 as shown in Figure 6
3) Ensure that the PS_ON switch (SW1 on schematic) is turned to the OFF position. It is located on the bottom left half of the board.
4) Connect one end of USB dongle to the board and the other end to the board to the USB port on the PC using the “USB to I2C interface” dongle.
5) The software should report that the ADP1046A has been located on the board. Click “Finish” to proceed to the Main Software Interface Window. The serial number reported on the side of the checkbox indicates the USB dongle serial number. The windows also displays the device I2C address.

Figure 6 - ADP1046A address of 50h in the GUI

5. If the software does not detect the part it enters into simulation mode. Ensure that the connecter is connected to the daughter card. Click on ‘Scan for ADP1046A now’ icon (magnifying glass) located on the top right hand corner of the screen.

Figure 7 - "Scan for ADP1046A Now' icon

5. Click on the "Load Board Settings" icon (fourth button from the left) and select the ADP1046A_FBPS_600W_xxxx**.46b** file. This file contains all the board information including values of shunt and voltage dividers. Note: All board setting files have an extension of .46b

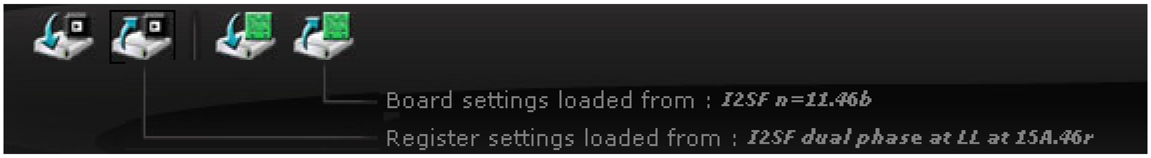

Figure 8 - Different icons on dashboard for loading and saving .46r and .46b files

6. The IC on the board comes preprogrammed and this step is optional. The original register configuration is stored in the ADP1046A_FBPS_600W_xxxx**.46r** register file (Note: All register files have an extension of .46r). The file can be loaded using the second icon from the left in Figure 8.

7. Connect a DC power source (385VDC nominal, current limit to ~2A) and an electronic load at the output set to 1 Ampere.

8. Connect a voltmeter on test points TP26(+) and TP46(-). Ensure that the differential probes are used and the ground of the probes are isolated if oscilloscope measurements are made on the primary side of the transformer.

9. Click on the Dashboard settings (3rd icon in Figure 7 and turn on the software PS_ON)

10. The board should now up and running, and ready for evaluation. The output should now read 12 VDC.

11. Click on the 'MONITOR' tab and then on the Flags and readings icon. This window provides a snapshot of the entire state of the PSU in a single user friendly window.

BOARD SETTINGS

The following screenshot displays the board settings.

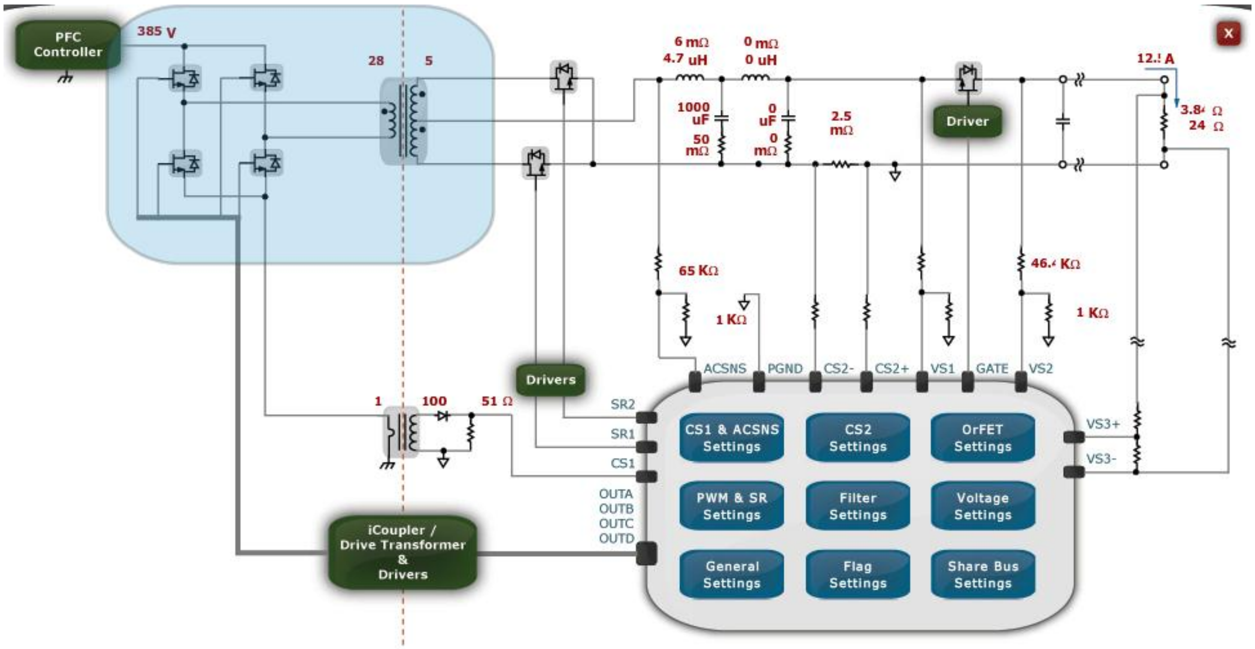

Figure 9 - Main Setup window of ADP1046A GUI

THEORY OF OPERATION DURING STARTUP

The following steps briefly describe the startup procedure of the ADP1046A and the power supply and the operation of the state machine for the preprogrammed set of registers that are included in the design kit.

1. The on board auxiliary power starts up at approximately 50VDC. This provides a drive voltage on the isolated side to an LDO (3.3V) that powers up the ADP1046A. After VDD (3.3V) is applied to the ADP1046A it takes approximately 20-50µs for VCORE to reach 2.5V. The digital core is now activated and the contents of the registers are downloaded in the EEPROM. The ADP1046A is now ready for operation.
2. PS_ON is applied. The power supply begins the programmed softstart ramp of 50ms (programmable).
3. Since the ‘softstart from pre-charge’ setting is active the output voltage is sensed before the softstart ramp begins. Depending upon the output voltage level of the effective softstart ramp is reduced by the proportional amount.
4. The PSU now is running in steady state. PGOOD1 turns on after the programmed debounce.
5. If a fault is activated during the softstart or steady state, the corresponding flag will be set and the programmed action will be taken such as disable PSU and re-enable after 1 sec or ‘Disable SR and OrFET, Disable OUTAUX’ etc.

FLAGS SETTINGS CONFIGURATIONS

Basically when a flag is triggered, the ADP1046A state machine waits for a programmable debounce time before taking any action. The response to each flag can be programmed individually. The flags can be programmed in a single window by selecting the FLAG SETTINGS icon in the MONITOR tab in the GUI. This monitor window shows all the fault flags (if any) and the readings in one page. The 'Get First Flag' button determines the first flag that was set in case of a fault event.

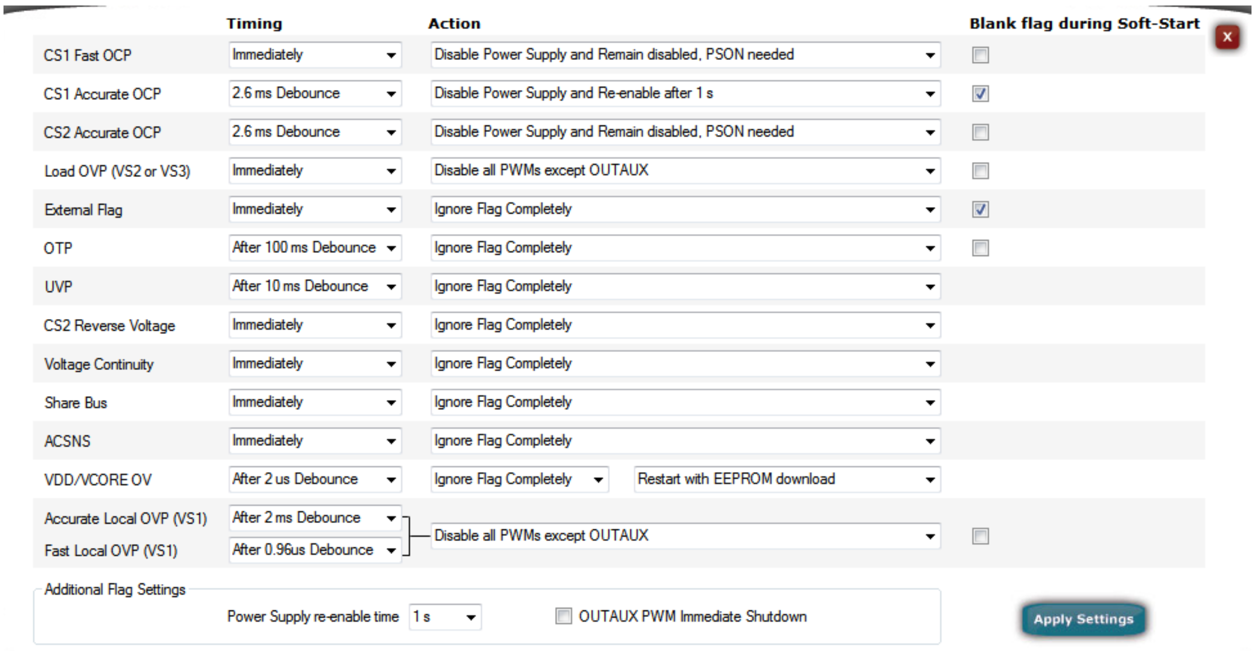

Figure 10 - Fault Configurations

PWM SETTINGS

The ADP1046A has a fully programmable PWM setup that controls 7 PWMs. Due to this flexibility the IC can function in several different topologies such as any isolated buck derived topology, push pull, flyback and also has the control law for resonant converters.

Each PWM edge can be moved in 5ns steps to achieve the appropriate deadtime needed and the maximum modulation limit sets the maximum duty cycle.

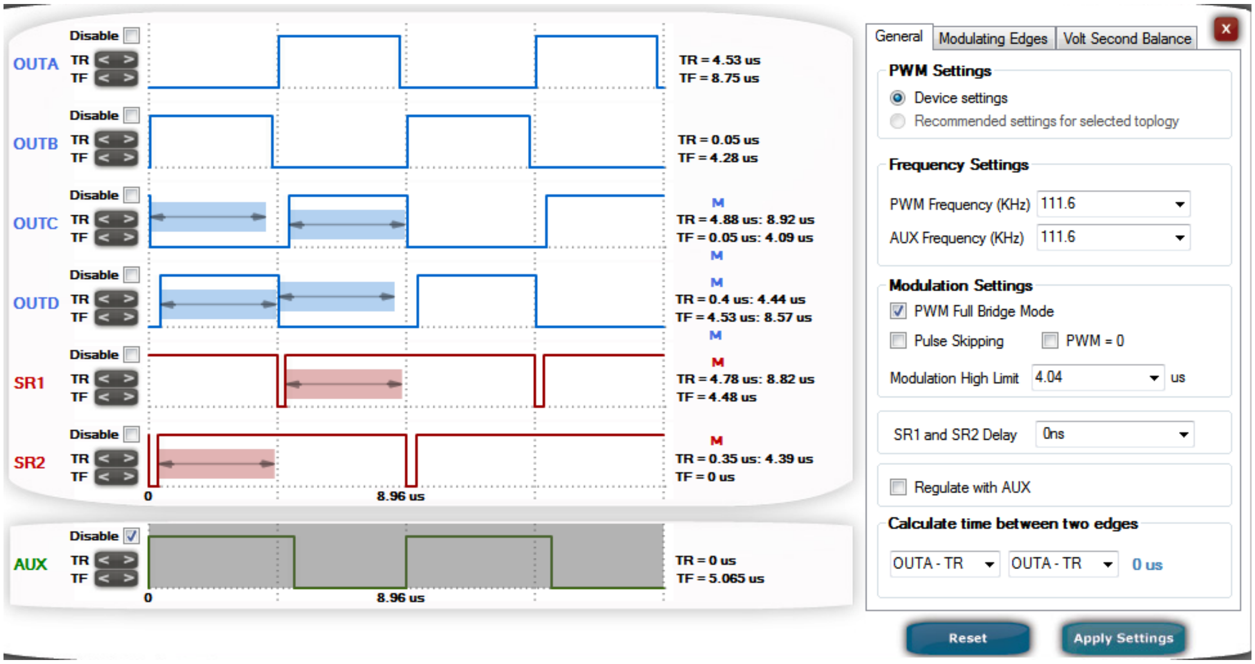

Figure 11 – PWM Settings window in the GUI

PWM	Switching element being controlled
OUTA-OUTD	Primary switch PWM configured for Phase shifted topology
SR1-SR2	Synchronous rectifier PWMs
OUTAUX	N/A

Table 4 –PWMs and their corresponding switching element

BOARD EVALUATION AND TEST DATA

STARTUP

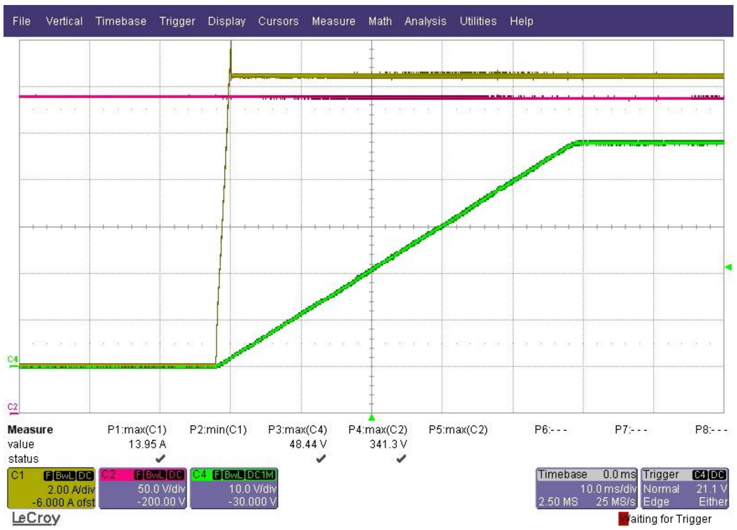

Figure 12 - Startup at 340VDC, 600W load(software PSON)
Green trace: Output voltage, 10V/div, 10ms/div
Yellow trace: Load current, 2A/div, 10ms/div
Red trace: Input voltage, 50V/div, 10ms/div

Figure 13 - Startup at 385VDC, 600W load (software PSON)
Green trace: Output voltage, 10V/div, 10ms/div
Yellow trace: Load current, 2A/div, 10ms/div
Red trace: Input voltage, 50V/div, 10ms/div

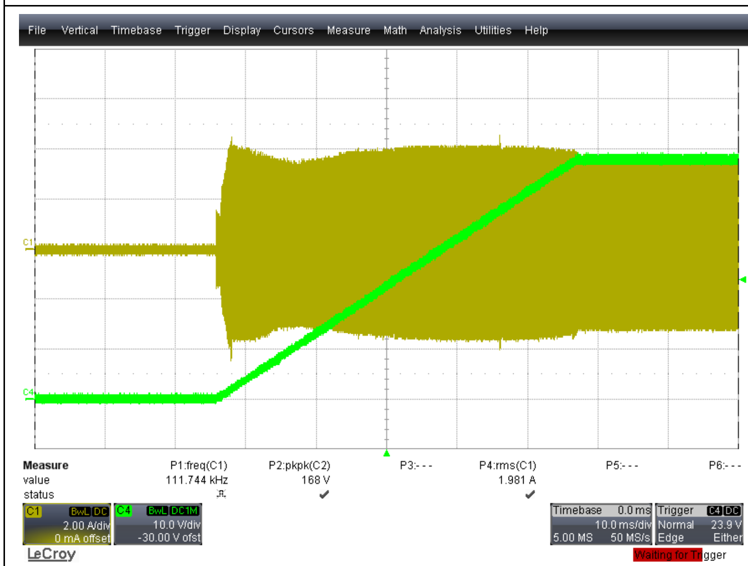

Figure 14 - Startup at 385VDC, full load
Green trace: Output voltage, 10V/div, 10ms/div
Yellow trace: Primary current, 2A/div, 10ms/div

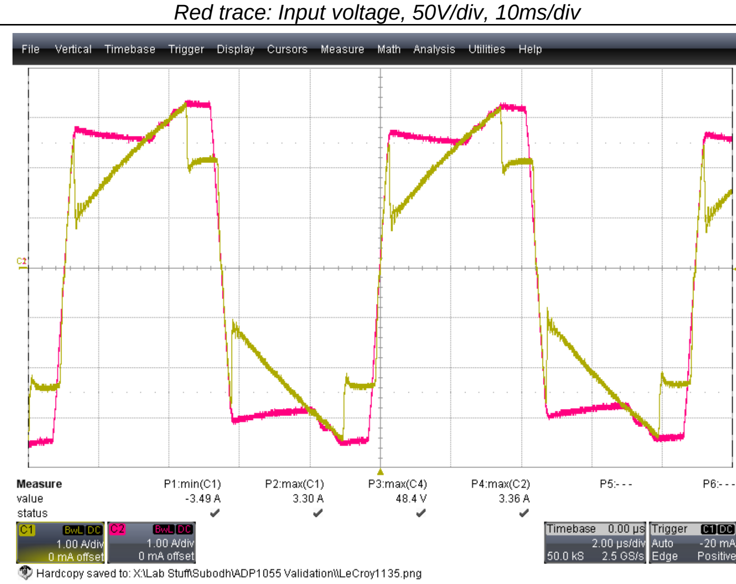

Figure 15 – Primary current at full load
Red trace: Resonant inductor current, 1A/div, 2us/div
Yellow trace: Primary current, 1A/div, 2us/div

OVERCURRENT AND SHORT CIRCUI PROTECTION

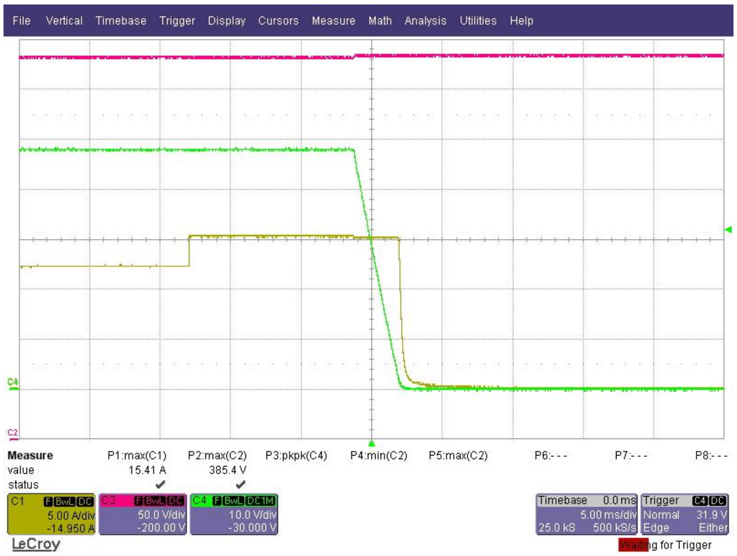

Figure 16 - OCP at 385VDC, 15A load(Action to shutdown after ~10ms)
Green trace: Output voltage, 10V/div, 5ms/div
Yellow trace: Load current, 5A/div, 5ms/div
Red trace: Input voltage, 50V/div, 5ms/div

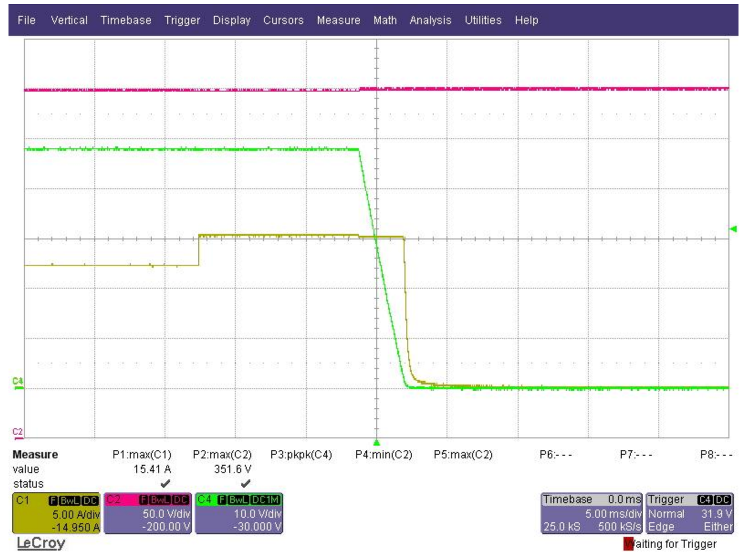

Figure 17 – OCP at 350VDC, 15A load(Action to shutdown after ~10ms)
Green trace: Output voltage, 10V/div, 5ms/div
Yellow trace: Load current, 5A/div, 5ms/div
Red trace: Input voltage, 50V/div, 5ms/div

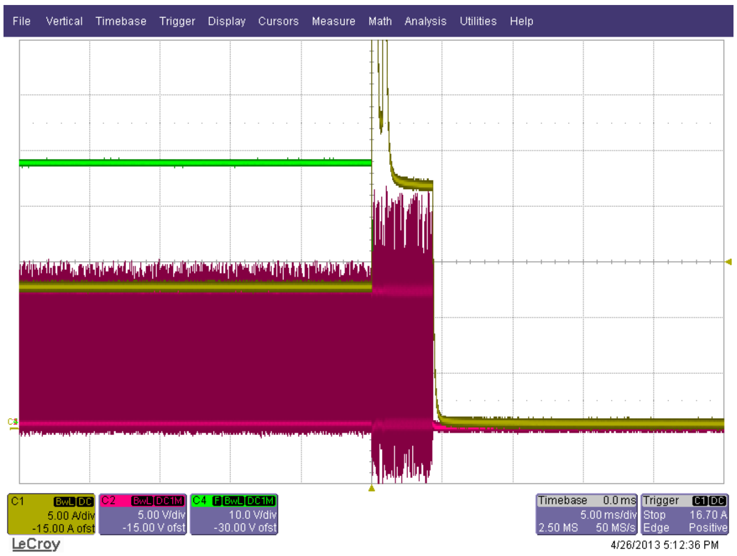

Figure 18 –Over current protection, 385VDC, 600Wto output shorted
Red trace: SR drive, 5V/div, 5ms/div
Green trace: Output voltage 10V/div, 200us/div
Yellow trace: Output current 5A/div

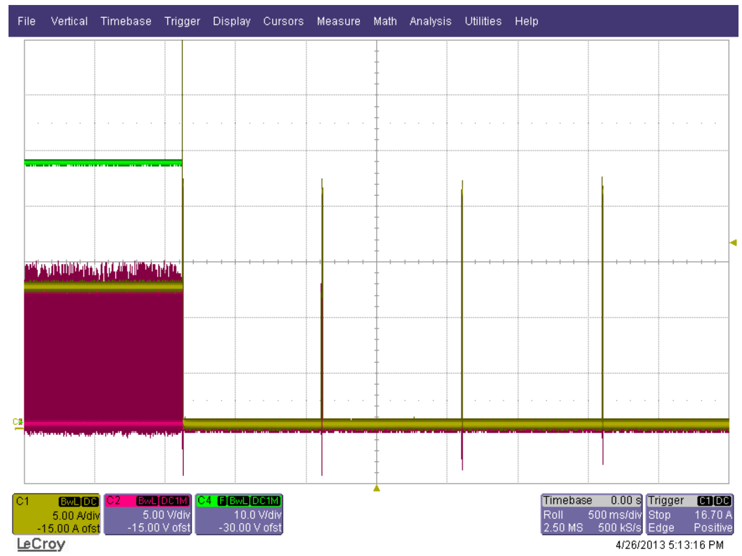

Figure 19 –Over current protection, HICCUP MODE, 385VDC, 600Wto output shorted
Red trace: SR drive, 5V/div, 5ms/div
Green trace: Output voltage 10V/div, 200us/div
Yellow trace: Output current 5A/div

PRIMARY GATE DRIVER DEADTIME

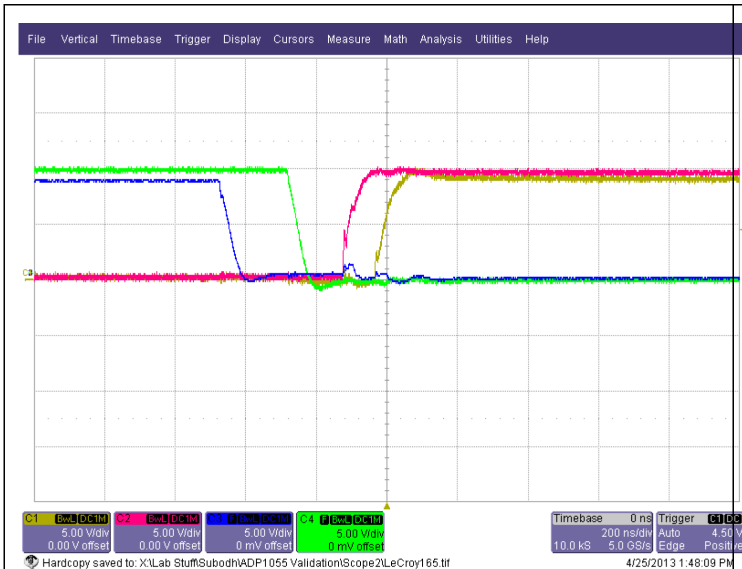

Figure 20 –Primary gate drive voltage at maximum modulation (Output of iCoupler) showing dead time, zoom in, 5V/div, 0.2us/div
Yellow Trace: OUTA
Red Trace: OUTB
Blue Trace: OUTC
Green Trace: OUTD

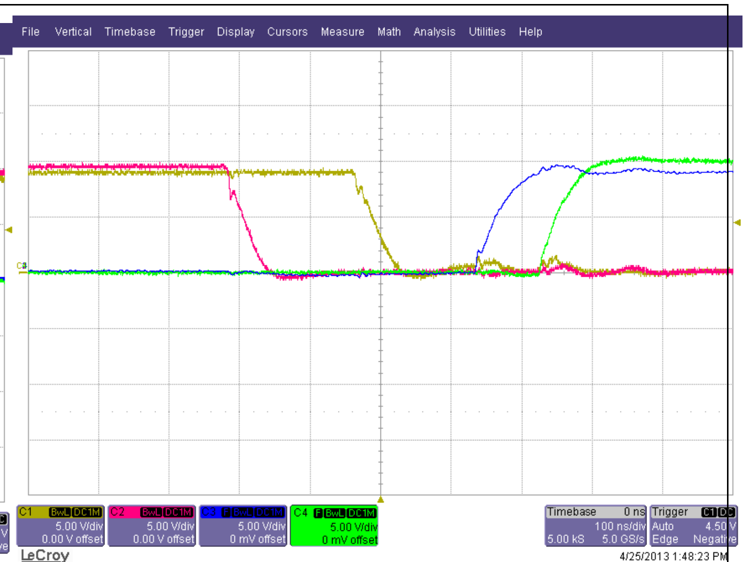

Figure 21 –Primary gate drive voltage at maximum modulation (Output of iCoupler)
showing dead time, zoom in, 5V/div, 0.2us/div
Yellow Trace: OUTA
Red Trace: OUTB
Blue Trace: OUTC
Green Trace: OUTD

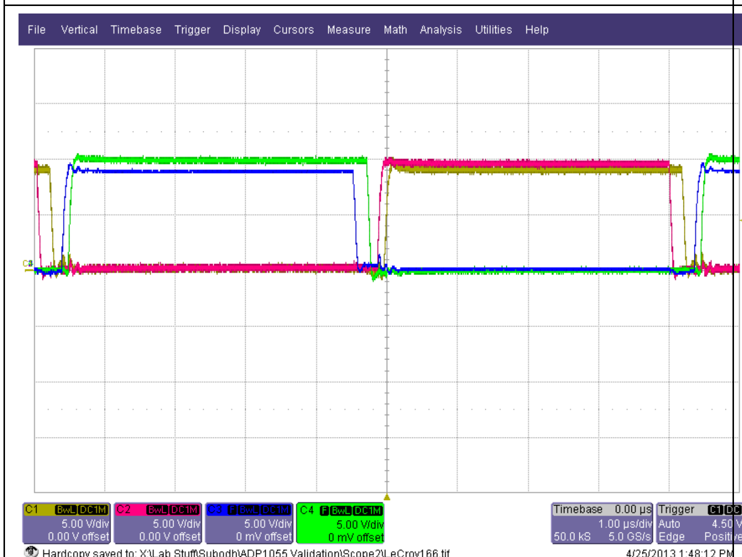

Figure 22 –Primary gate drive voltage at MAXIMUM modulation (Output of iCoupler)
5V/div, 1us/div
Yellow Trace: OUTA
Red Trace: OUTB
Blue Trace: OUTC
Green Trace: OUTD

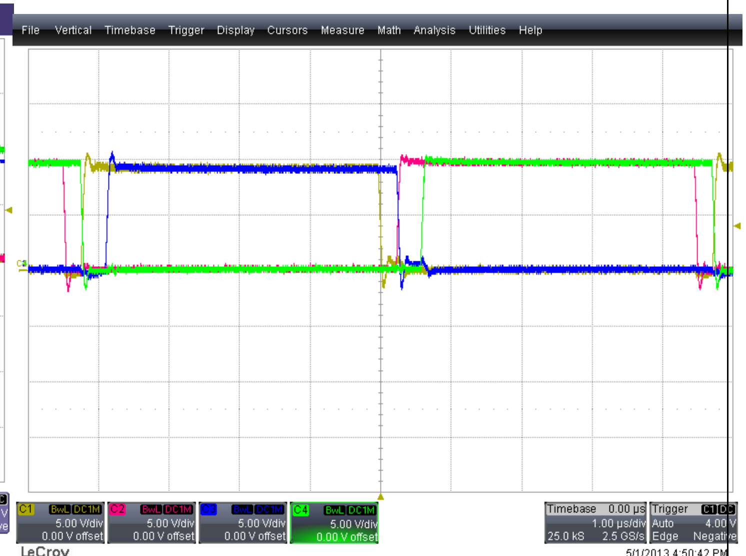

Figure 23 –Primary gate drive voltage at MINIMUM modulation (Output of iCoupler)
5V/div, 1us/div
Yellow Trace: OUTA
Red Trace: OUTB
Blue Trace: OUTC
Green Trace: OUTD

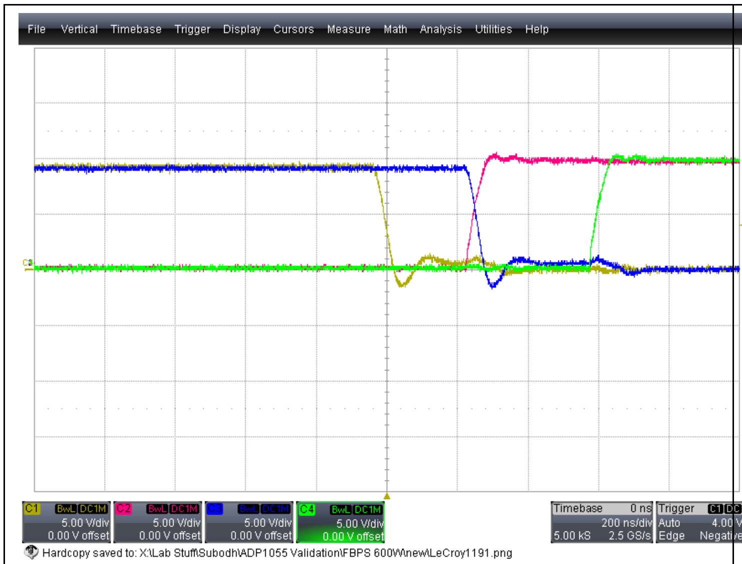

Figure 24 –Primary gate drive voltage at MINIMUM modulation (Output of iCoupler) showing dead time, zoom in, 5V/div, 0.2us/div
Yellow Trace: OUTA
Red Trace: OUTB
Blue Trace: OUTC
Green Trace: OUTD

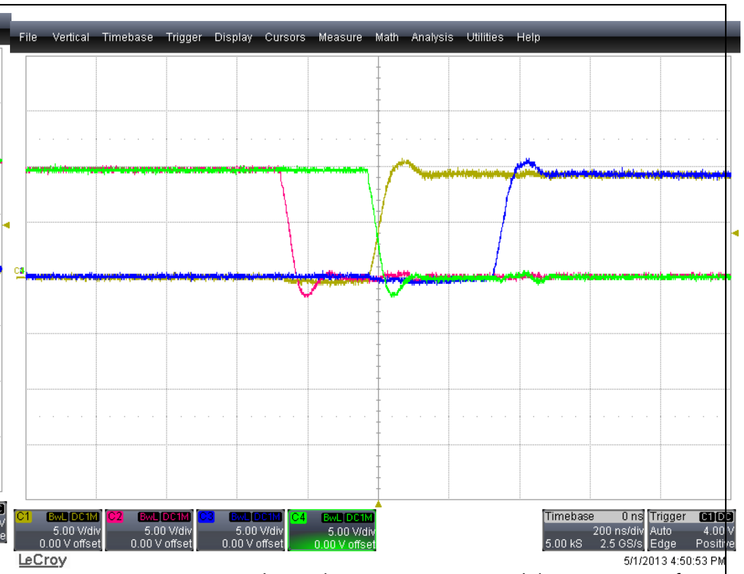

Figure 25 –Primary gate drive voltage at MINIMUM modulation (Output of iCoupler) showing dead time, zoom in, 5V/div, 0.2us/div
Yellow Trace: OUTA
Red Trace: OUTB
Blue Trace: OUTC
Green Trace: OUTD

CS1 PIN VOLTAGE (PRIMARY CURRENT)

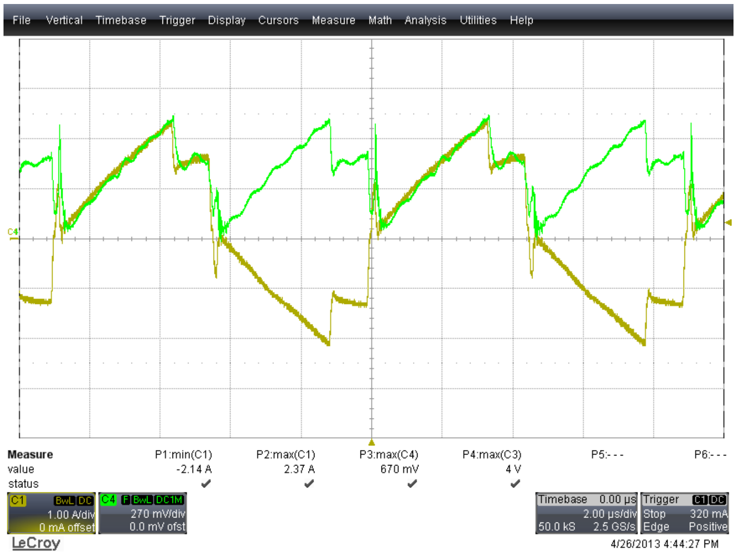

Figure 26 – Primary current at 385VDC, 300W load, 2us/div
Yellow trace: Primary current half effect probe 1A/div
Green trace: CS1 pin voltage, 270mV/div

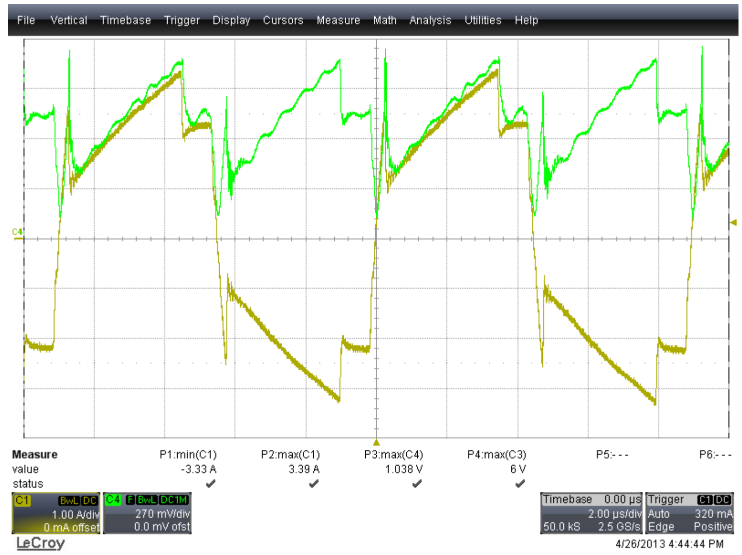

Figure 27 – Primary current at 385VDC, 600W load, 2us/div
Yellow trace: Primary current half effect probe 1A/div
Green trace: CS1 pin voltage, 270mV/div

SYNCHRONOUS RECTIFIER PEAK INVERSE VOLTAGE

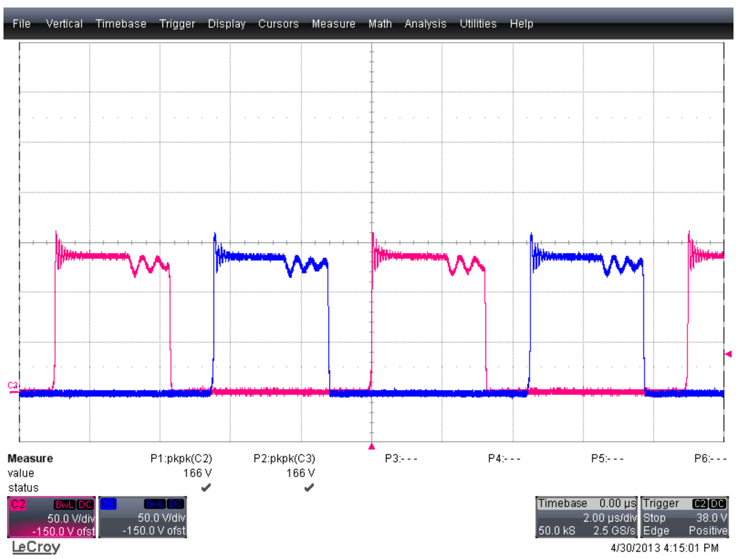

Figure 28 – Synchronous rectifier MOSFET Peak reverse voltage at 600W load, 385VDC, 50V/div, 2us/div

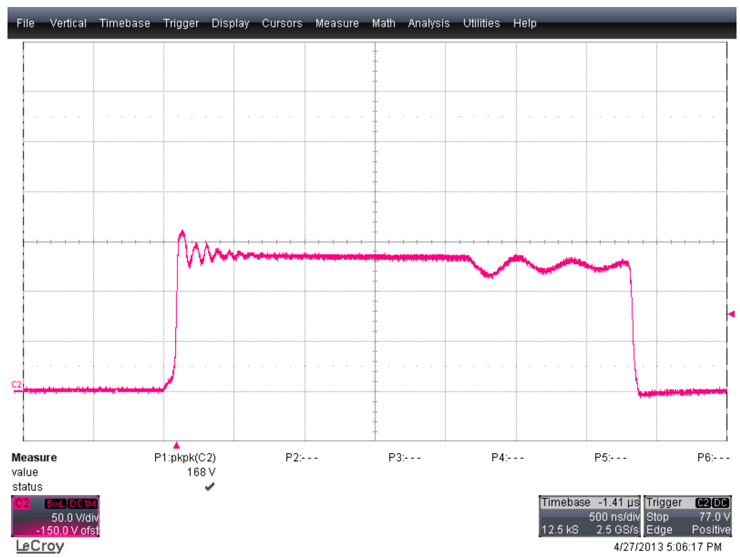

Figure 29 – Synchronous rectifier MOSFET Peak reverse voltage at 600W load, 385VDC, 50V/div, 500ns/div

OUTPUT VOLTAGE RIPPLE

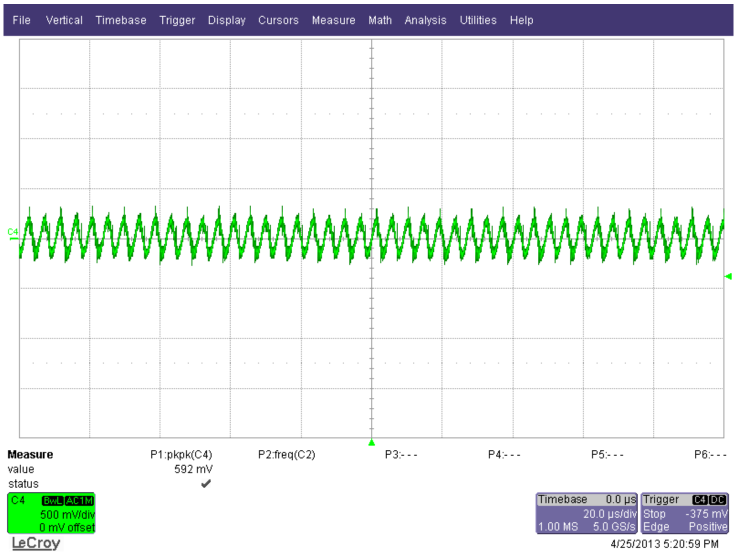

Figure 30 – Output voltage AC coupled
385VDC, 12.5A, 500mV/div, 20us/div. High frequency component.

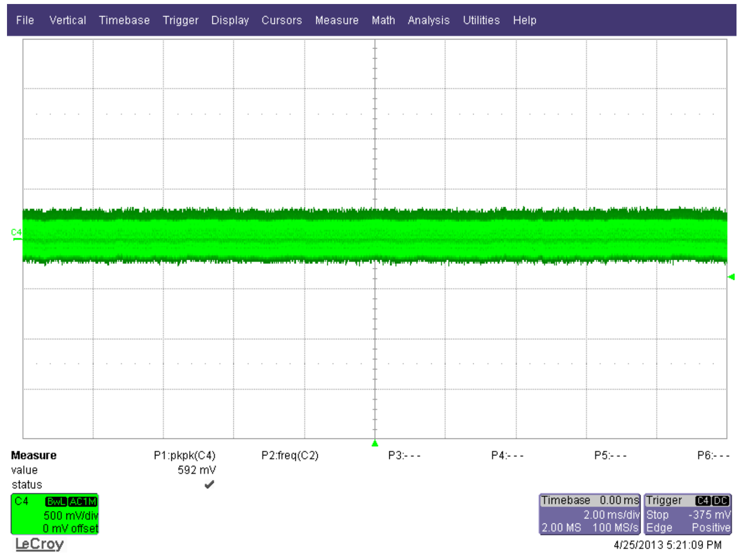

Figure 31 – Output voltage AC coupled
385VDC, 12.5A, 500mV/div, 2ms/div. Low frequency component.

TRANSIENT VOLTAGE AT 385VDC (NOMINAL VOLTAGE)

LOAD STEP OF 15-50%

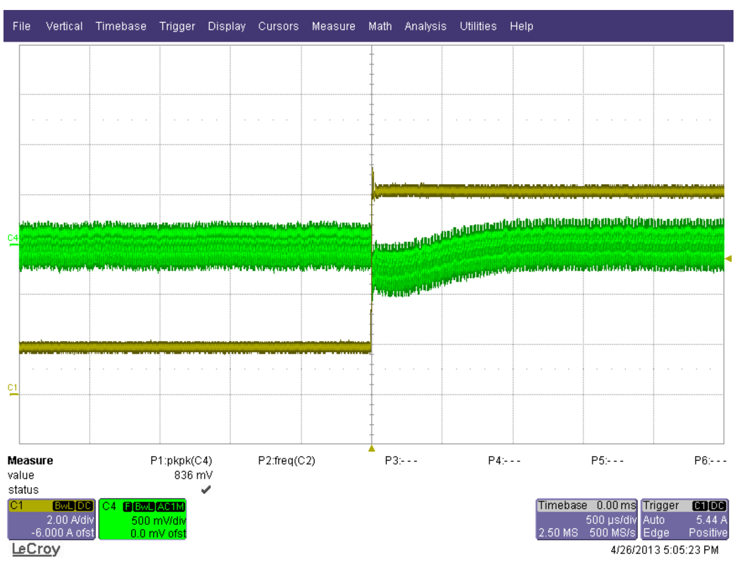

Figure 32 – Output voltage transient, 500us/div
Yellow trace: Load current, 2A/div
Green trace: Output voltage (AC coupled), 500mV/div

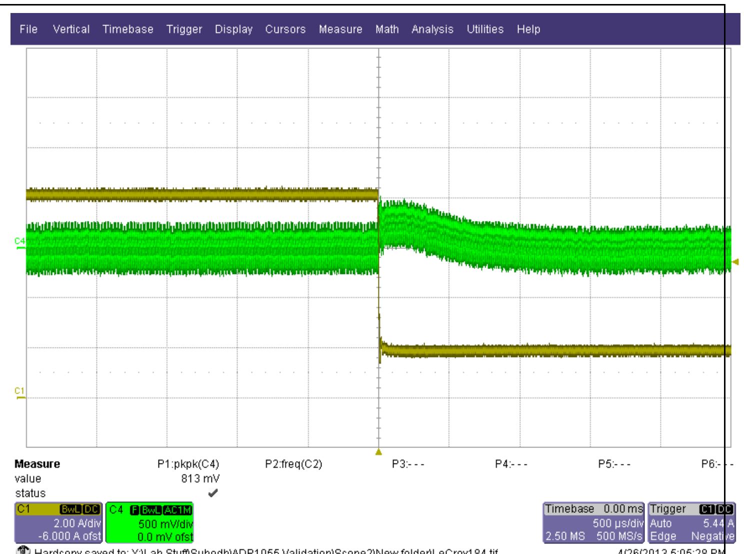

Figure 33 – Output voltage transient, 500us/div
Yellow trace: Load current, 2A/div
Green trace: Output voltage (AC coupled), 500mV/div

LOAD STEP OF 50-100%

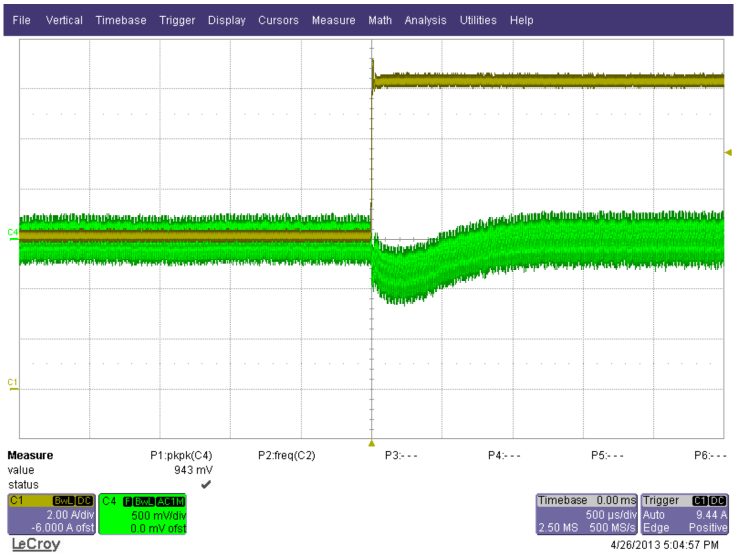

Figure 34 – Output voltage transient, 500us/div
Yellow trace: Load current, 2A/div
Green trace: Output voltage (AC coupled), 500mV/div

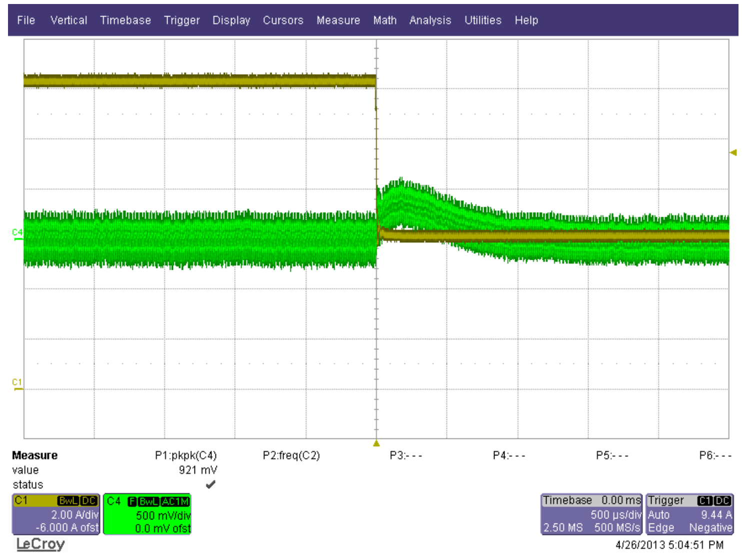

Figure 35 – Output voltage transient, 500us/div
Yellow trace: Load current, 2A/div
Green trace: Output voltage (AC coupled), 500mV/div

LOAD STEP OF 0-50%

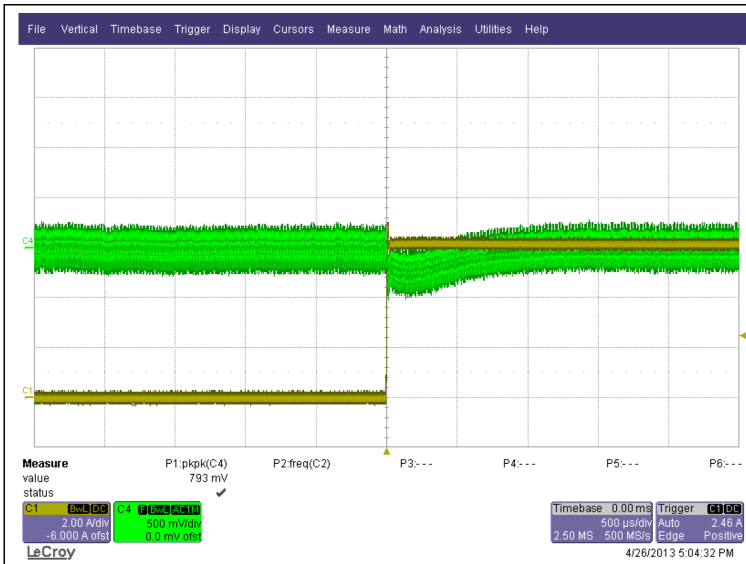

Figure 36 – Output voltage transient, 500us/div
Yellow trace: Load current, 2A/div
Green trace: Output voltage (AC coupled), 500mV/div

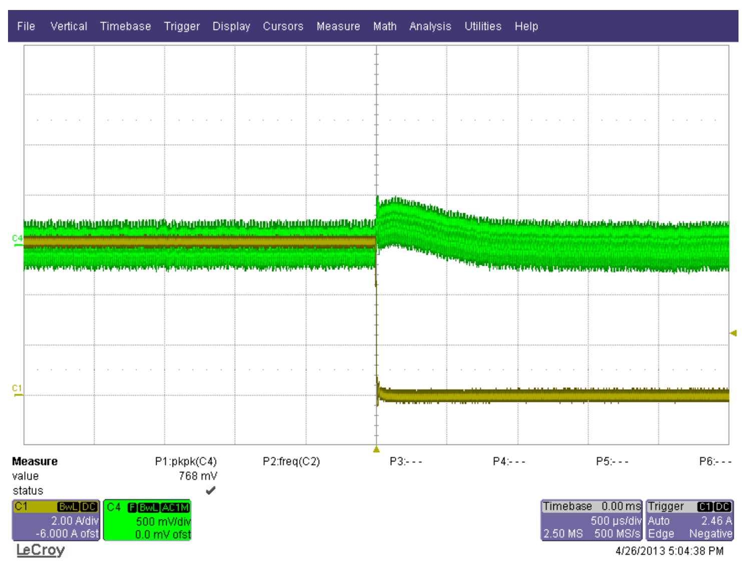

Figure 37 – Output voltage transient, 500us/div
Yellow trace: Load current, 2A/div
Green trace: Output voltage (AC coupled), 500mV/div

HOLD UP TIME AND VOLTAGE DROP OUT

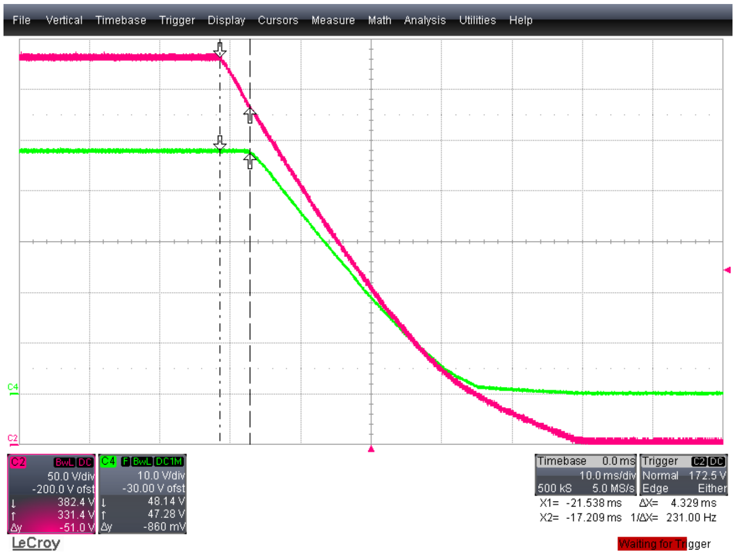

Figure 38 –Minimum input voltage of ~330VDC before output regulation is lost at 600W, 10ms/div
Red trace: Input voltage step 50V/div
Green trace: Output voltage, 10V/div

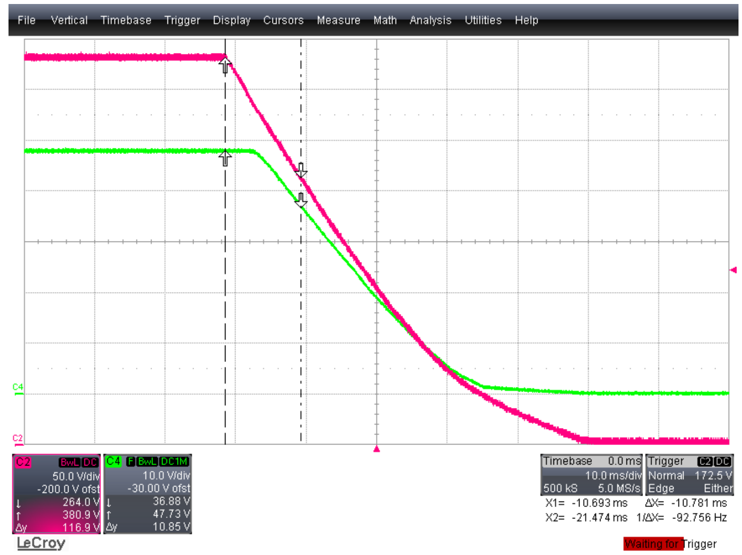

Figure 39 –Hold up time of ~10.781ms before output voltage reaches 36V (minimum telecom input) at 600W, 100uF input capacitor,10ms/div
Red trace: Input voltage step 50V/div
Green trace: Output voltage, 10V/div

LINE VOLTAGE FEEDFORWARD

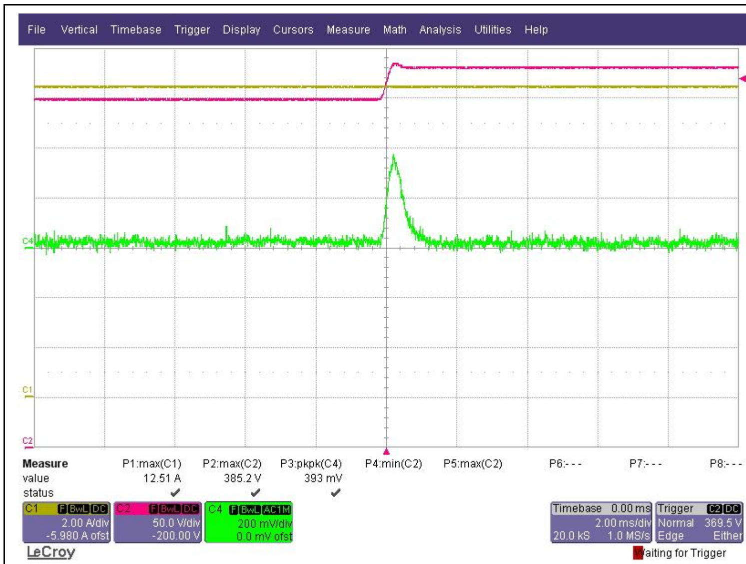

Figure 40 – Line voltage Feed forward DISABLED, 600W load
Red trace: Input voltage step 350-385VDC, 50V/div
Green trace: Output voltage (AC Coupled), 200mV/div

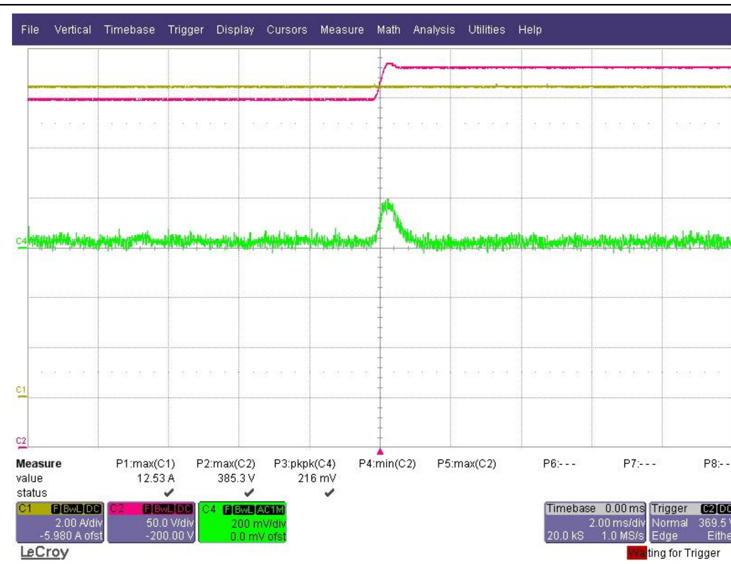

Figure 41 – Line voltage Feed forward ENABLED, 600W load
Red trace: Input voltage step 350-385VDC, 50V/div
Green trace: Output voltage (AC Coupled), 200mV/div

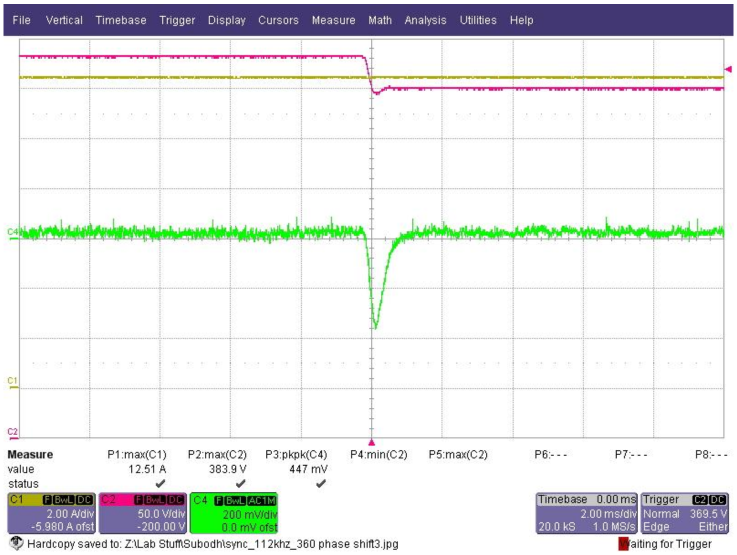

Figure 42 – Line voltage Feed forward DISABLED, 600W load
Red trace: Input voltage step 350-385VDC, 50V/div
Green trace: Output voltage (AC Coupled), 200mV/div

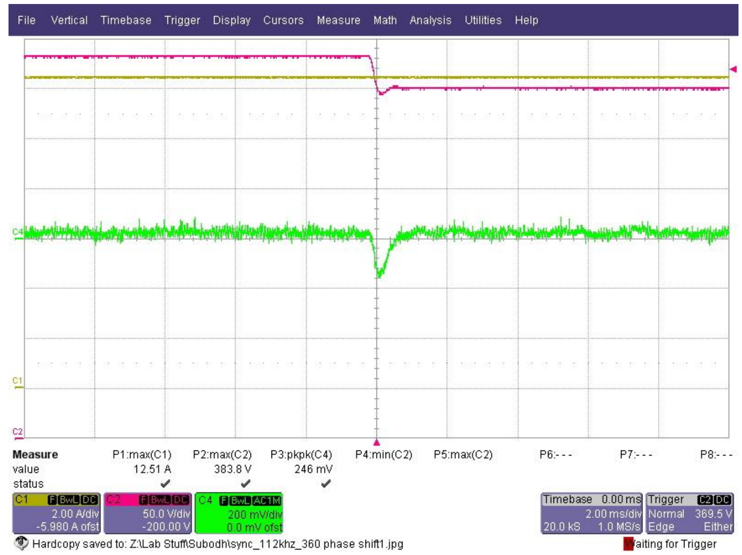

Figure 43 – Line voltage Feed forward ENABLED, 600W load
Red trace: Input voltage step 350-385VDC, 50V/div
Green trace: Output voltage (AC Coupled), 200mV/div

ZVS WAVEFORMS FOR QA (PASSIVE TO ACTIVE TRANSITION)

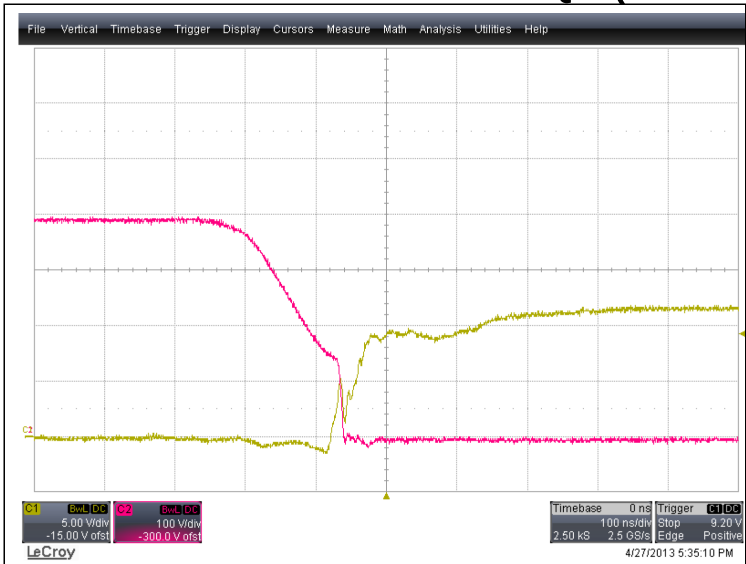

Figure 44 –Resonant transition at no load, 100ns/div
Red trace: VDS of QA, 100V/div
Yellow trace: VGS of QA, 5V/div

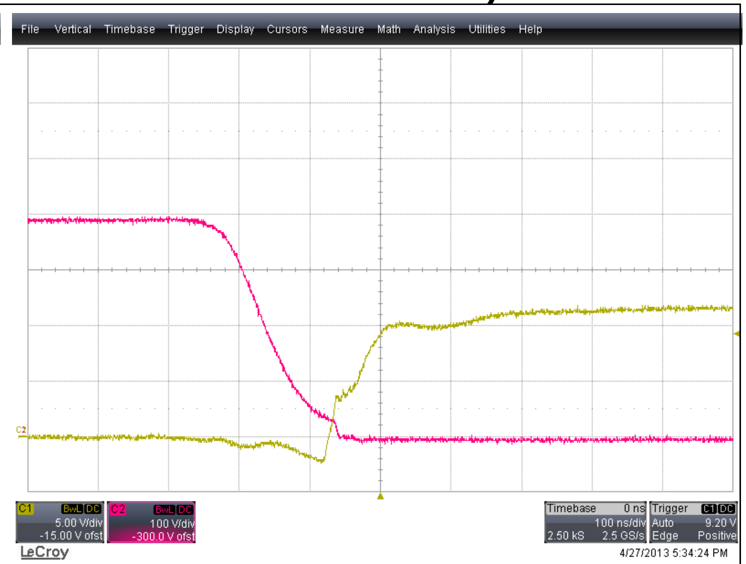

Figure 45 –Resonant transition at 48W load, 100ns/div
Red trace: VDS of QA, 100V/div
Yellow trace: VGS of QA, 5V/div

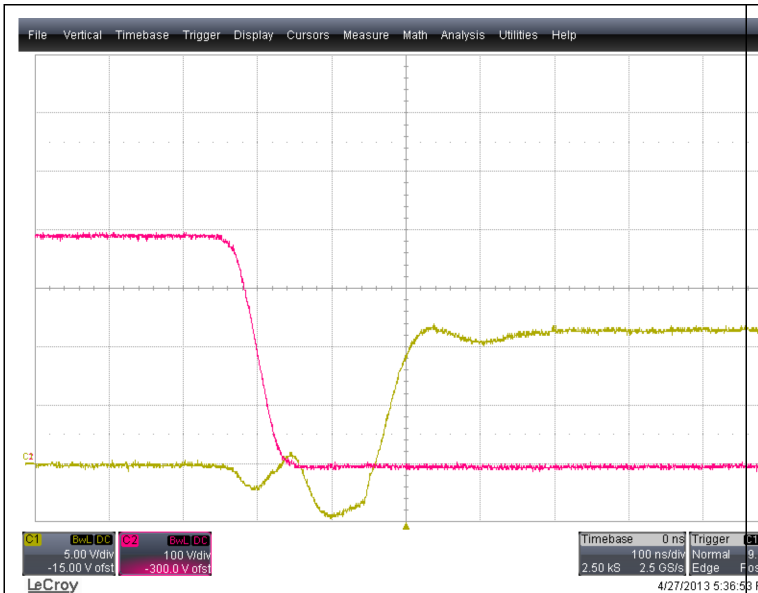

Figure 46 –Resonant transition at 300W load, 100ns/div
Red trace: VDS of QA, 100V/div
Yellow trace: VGS of QA, 5V/div

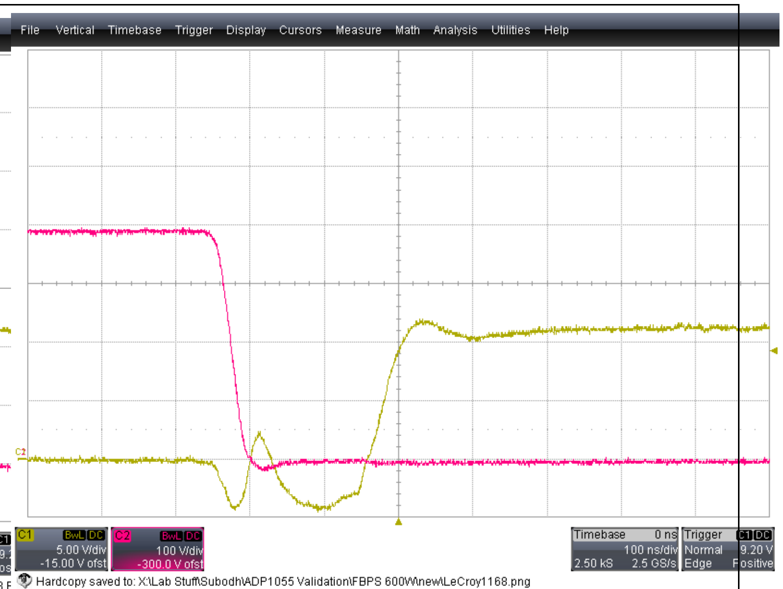

Figure 47 –Resonant transition at 600W load, 100ns/div
Red trace: VDS of QA, 100V/div
Yellow trace: VGS of QA, 5V/div

ZVS WAVEFORMS FOR QB (PASSIVE TO ACTIVE TRANSITION)

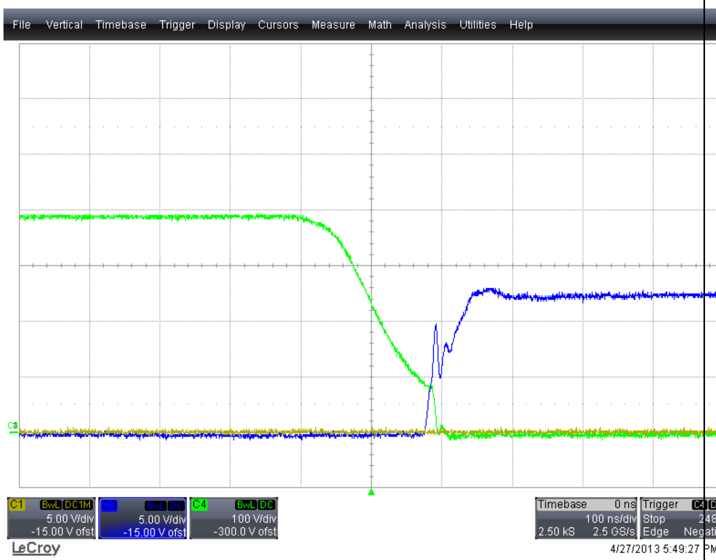

Figure 48 –Resonant transition at no load, 100us/div
Red trace: VDS of QB, 100V/div
Yellow trace: VGS of QB, 5V/div

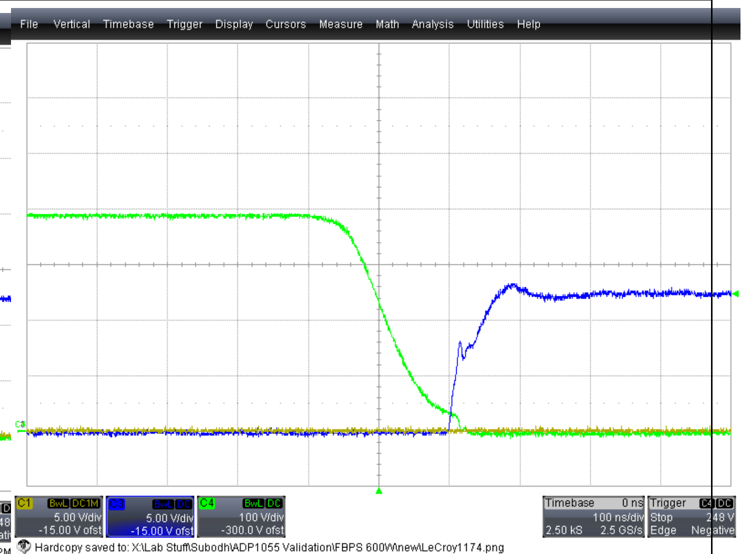

Figure 49 –Resonant transition at 48W load, 100us/div
Red trace: VDS of QB, 100V/div
Yellow trace: VGS of QB, 5V/div

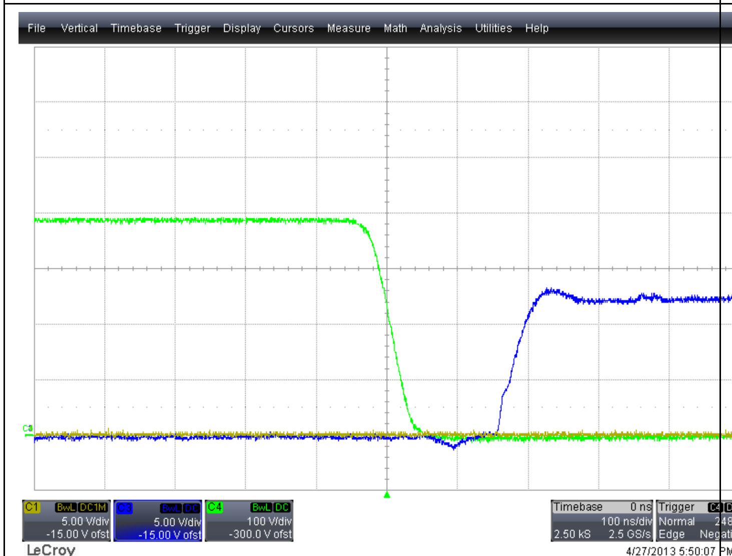

Figure 50 –Resonant transition at 300W load, 100us/div
Red trace: VDS of QB, 100V/div
Yellow trace: VGS of QB, 5V/div

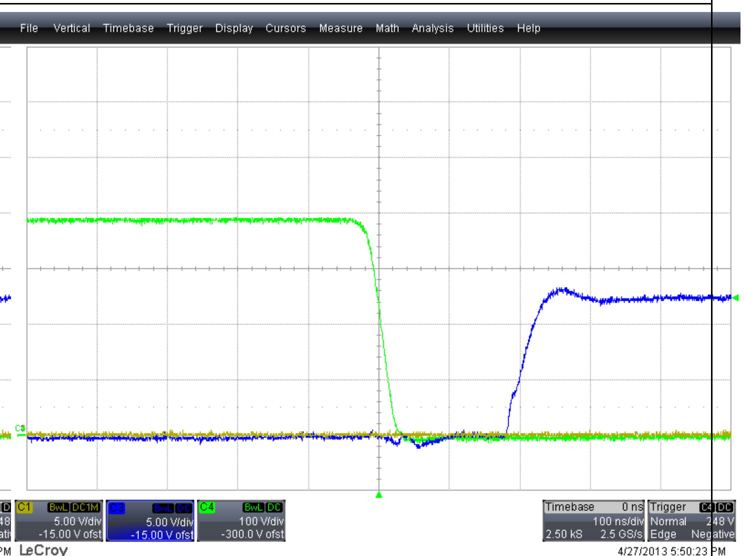

Figure 51 –Resonant transition at 600W load, 100us/div
Red trace: VDS of QB, 100V/div
Yellow trace: VGS of QB, 5V/div

ZVS WAVEFORMS FOR QC (ACTIVE TO PASSIVE TRANSITION)

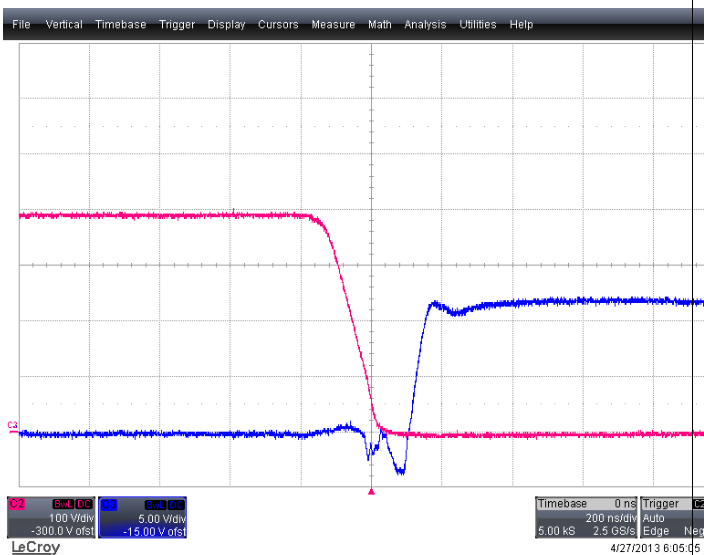

Figure 52 –Resonant transition at 300W load, 200us/div
Red trace: VDS of QC, 100V/div
Yellow trace: VGS of QC, 5V/div

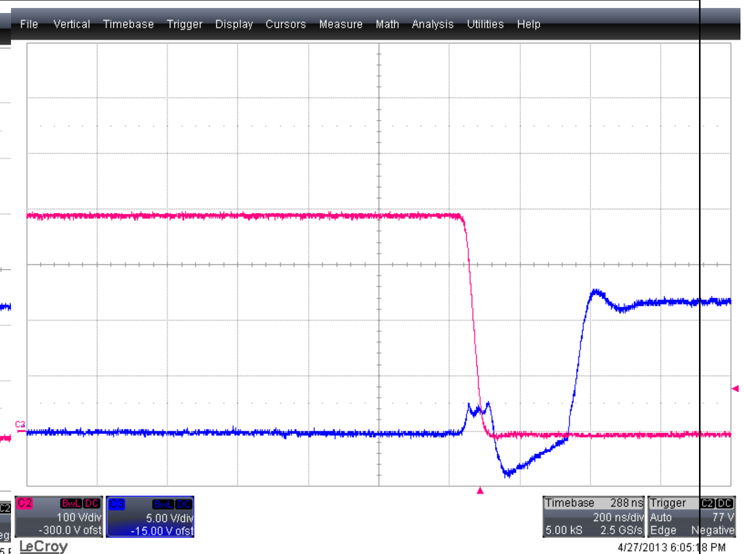

Figure 53 –Resonant transition at 300W load, 200us/div
Red trace: VDS of QC, 100V/div
Yellow trace: VGS of QC, 5V/div

ZVS WAVEFORMS FOR QD (ACTIVE TO PASSIVE TRANSITION)

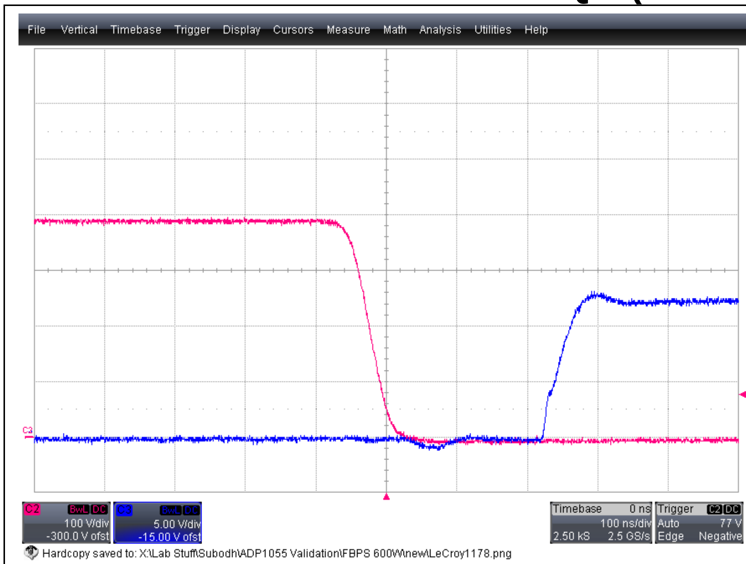

Figure 54 –Line Feed forward at 0A load
Red trace: Input voltage step 42-60V, 10V/div, 200us/div
Green trace: Output voltage (AC coupled), 500mV/div, 200us/div

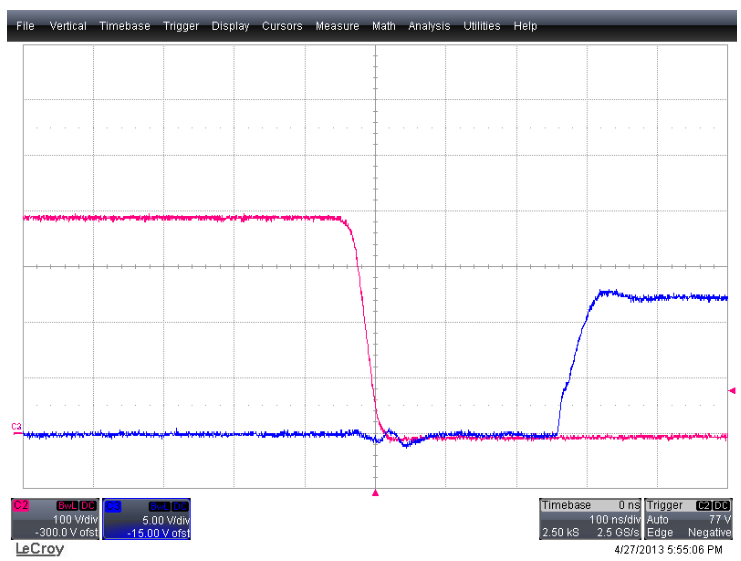

Figure 55 – Line Feed forward at 0A load
Red trace: Input voltage step 60-42V, 10V/div, 200us/div
Green trace: Output voltage (AC coupled), 500mV/div, 200us/div

CLOSED LOOP FREQUENCY RESPONSE

A network analyzer (AP200) was used to test the bode plots of the system. A continuous noise signal of 300mV was injected across the entire frequency range across a 10Ω resistor in series (R35) with the output voltage divider using an isolation transformer. The operating condition was 385VDC input and a load condition of 600W with a soaking time of 45 minutes.

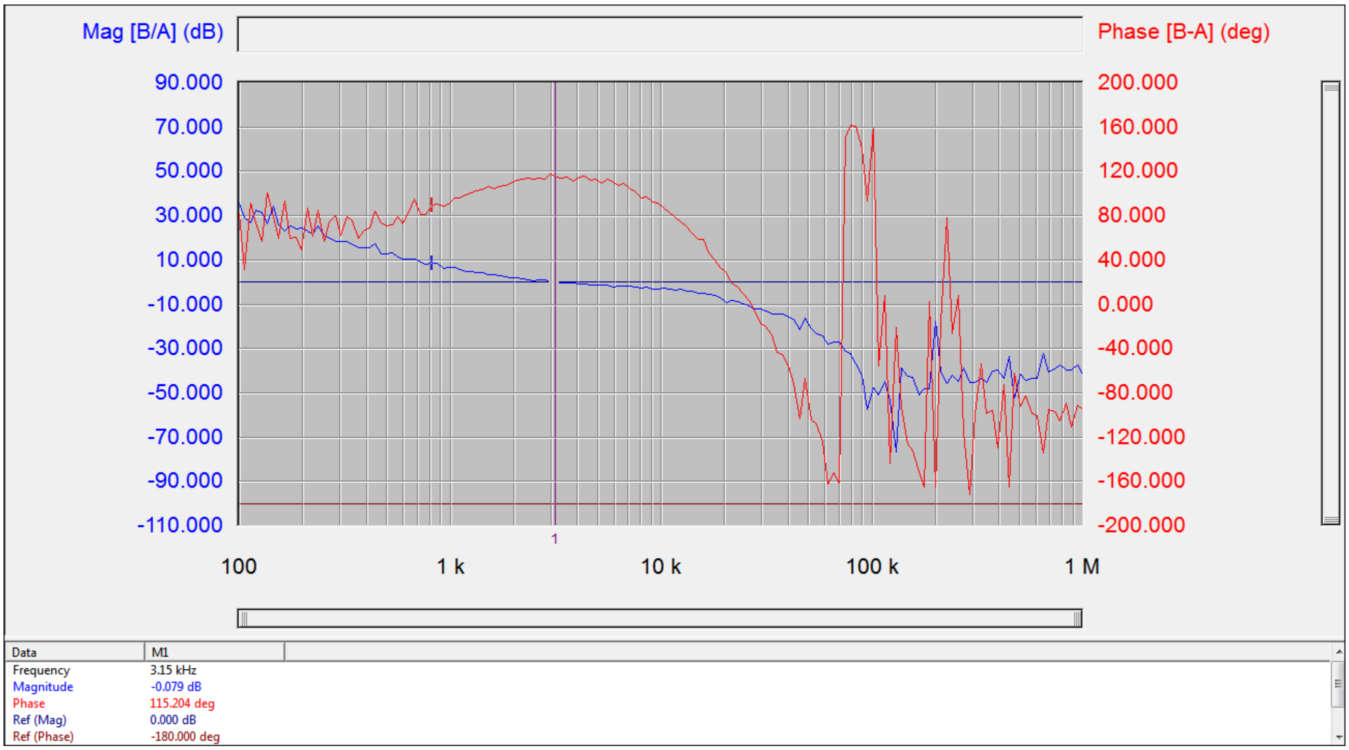

Figure 56 – Bode Plots, 385VDC input, 12.5A load,
Blue trace: Gain in dB
Red trace: Phase in degrees
Crossover frequency= 3.15KHz
Phase margin= 115.2°

EFFICIENCY

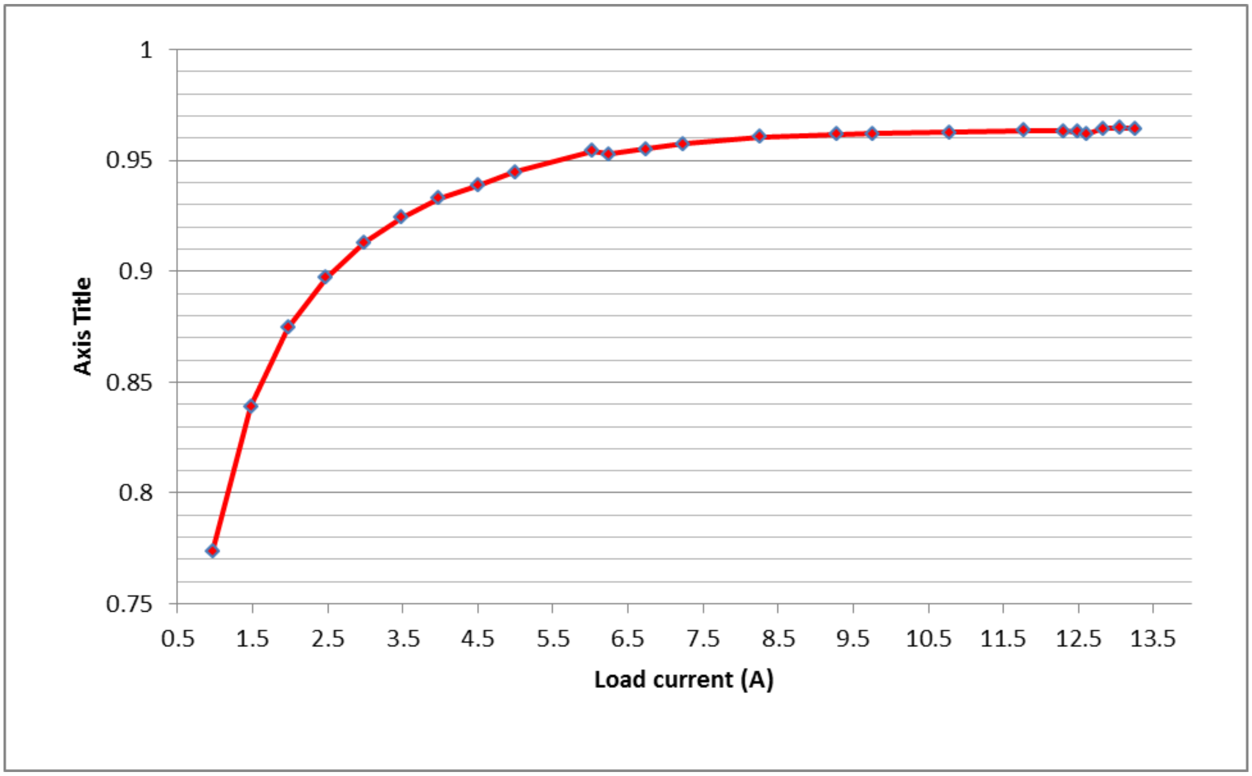

Figure 57 – Efficiency vs Load at 385VDC, 45 minutes soaking time, with on board air flow

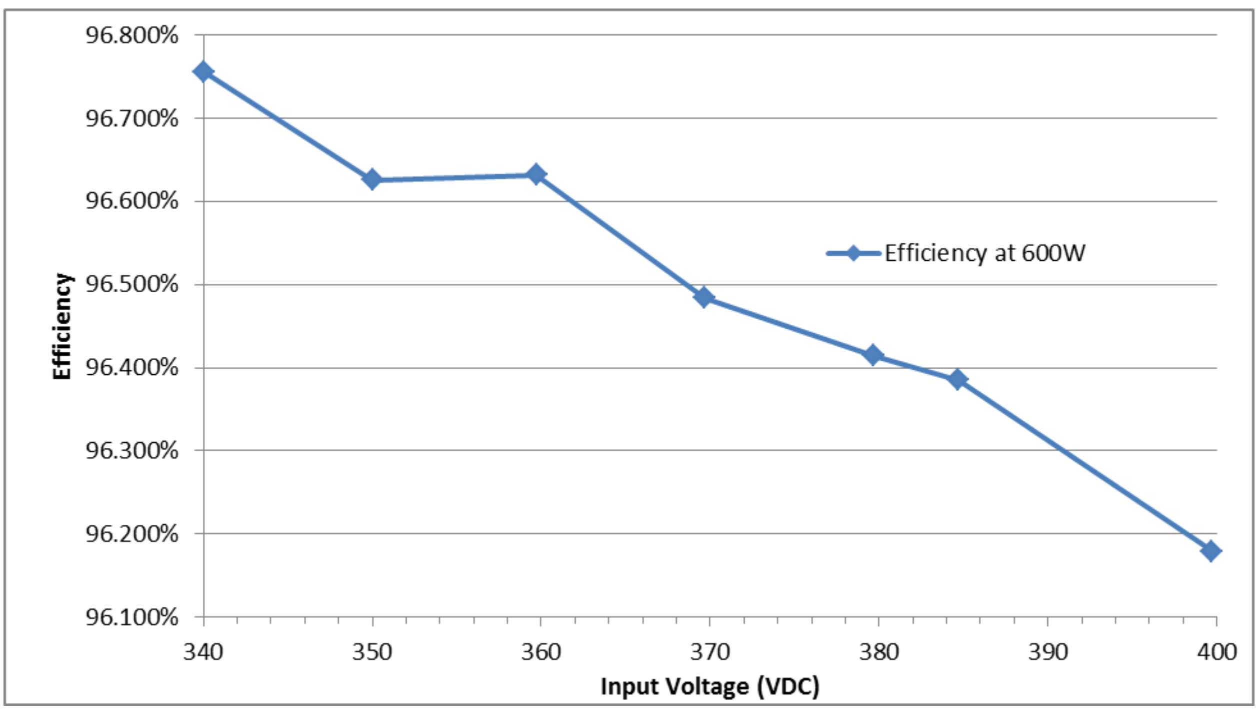

Figure 58 – Efficiency vs Line voltage at 600W load

TRANSFORMER SPECIFICATION

PARAMETER	*MIN*	*TYP*	*MAX*	*UNITS*	*NOTES*
Core and Bobbin					PQ3535, Magnetics Inc R Material or equivalent
Primary inductance		3.316		mH	Pins 1 to pin 6
Leakage inductance		4		µH	Pins 1 to pin 6 with all other windings shorted
Resonant frequency	850			KHz	Pins 1 to pin 6 with all other windings open

Table 5 - Transformer specifications

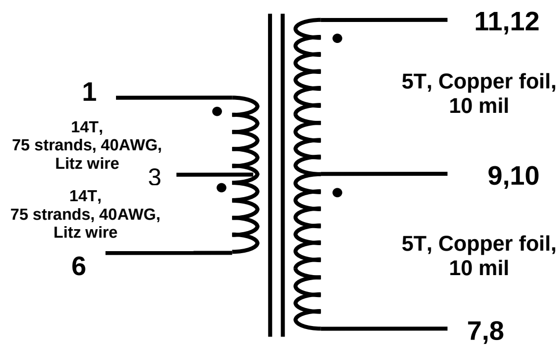

Figure 59 - Transformer electrical diagram

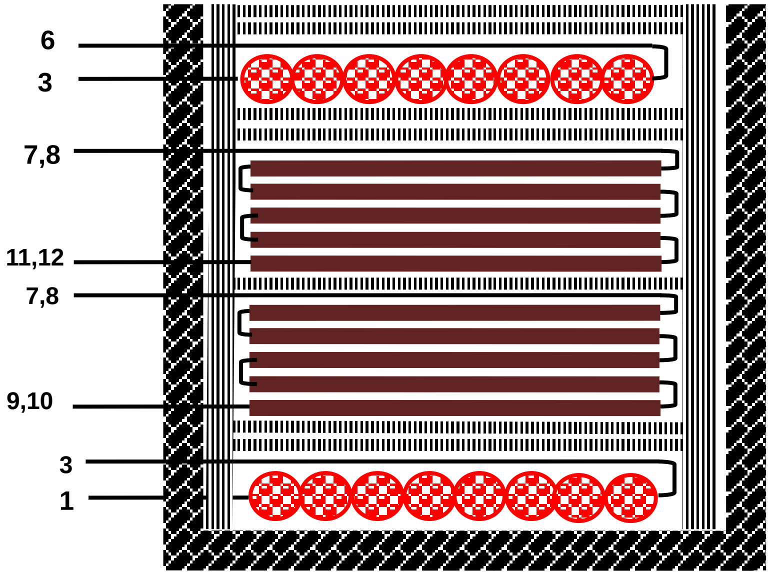

Figure 60 - Transformer construction diagram

THERMAL TEST DATA

A thermal snapshot of the unit was taken after running at 600W with a 45 minute soaking time.

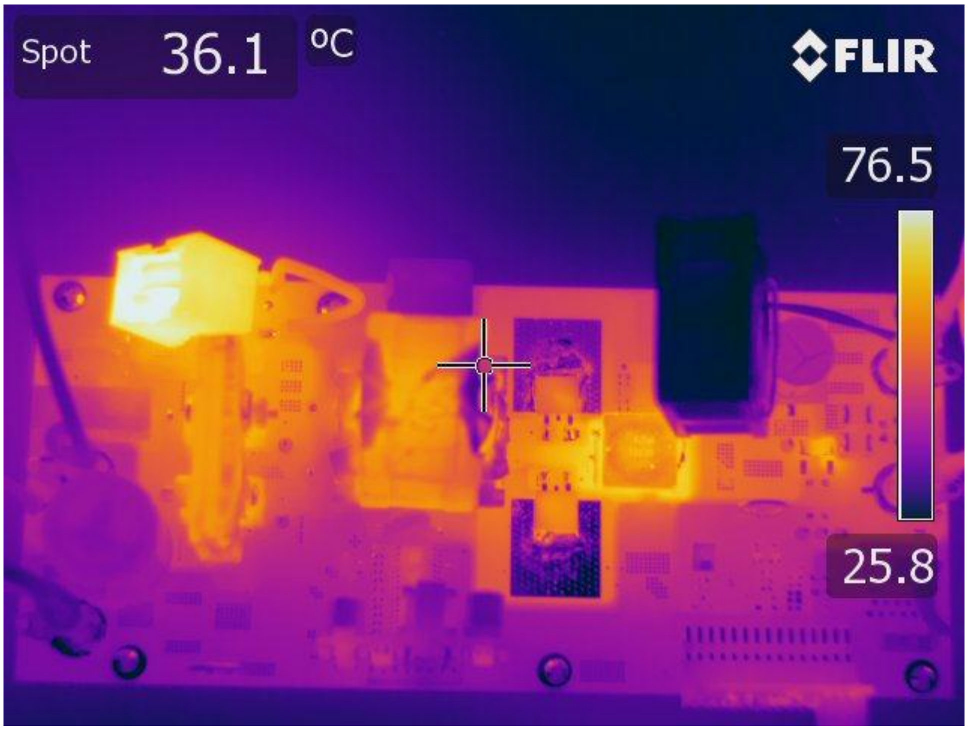

Figure 61 – Thermals, complete board

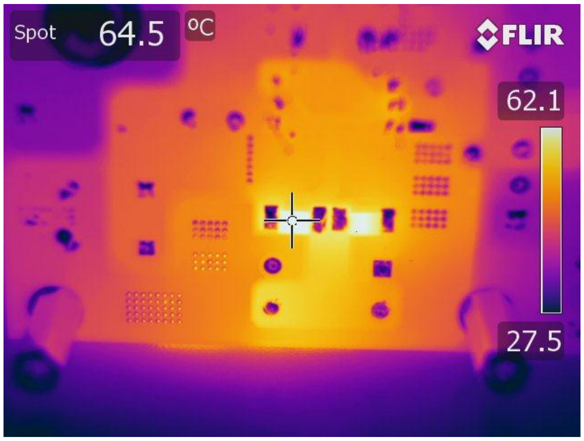

Figure 62 – Thermals, Primary clamp diode

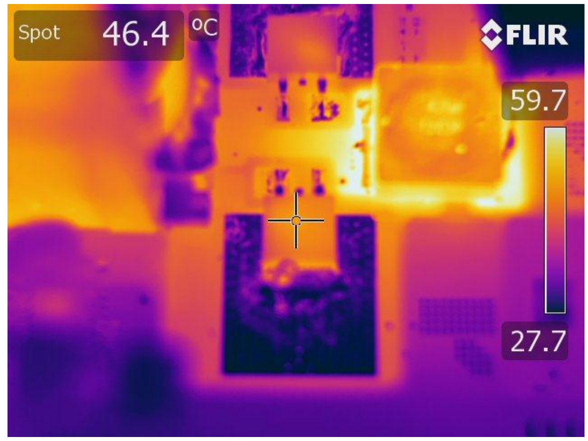

Figure 63 – Thermals, Synchronous Rectifier

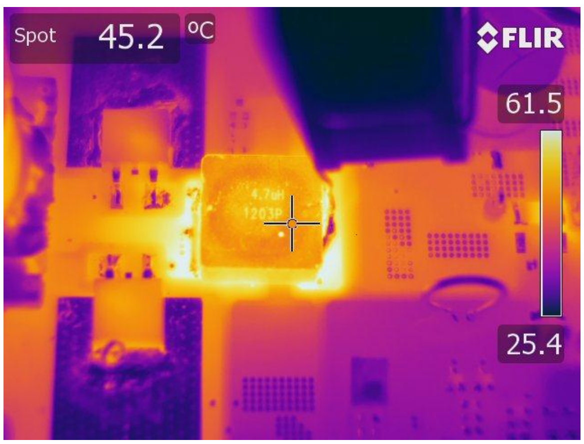

Figure 64 – Thermals, Output inductor

Figure 65 – Thermals, output current sense resistor

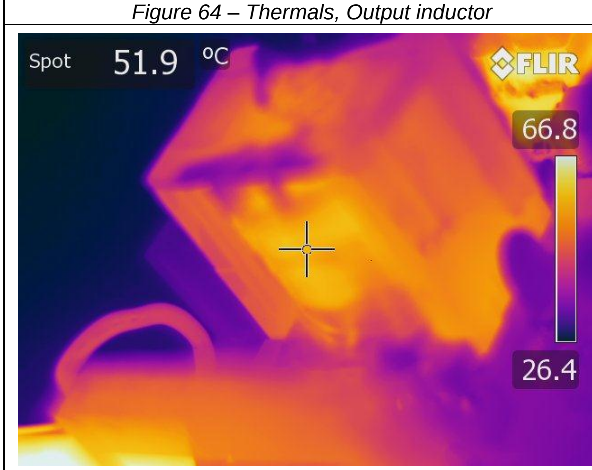

Figure 66 – Thermals, Transformer

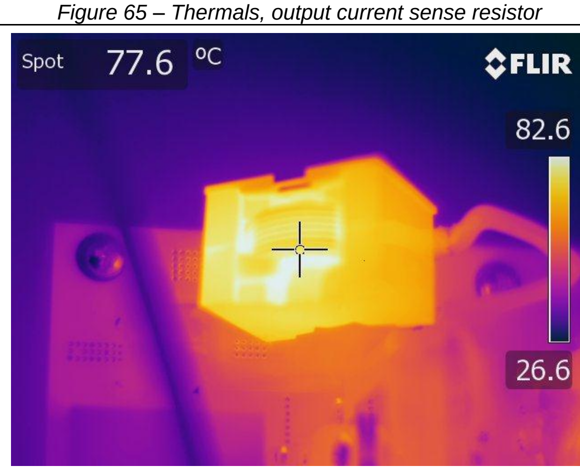

Figure 67 – Thermals, Resonant inductor

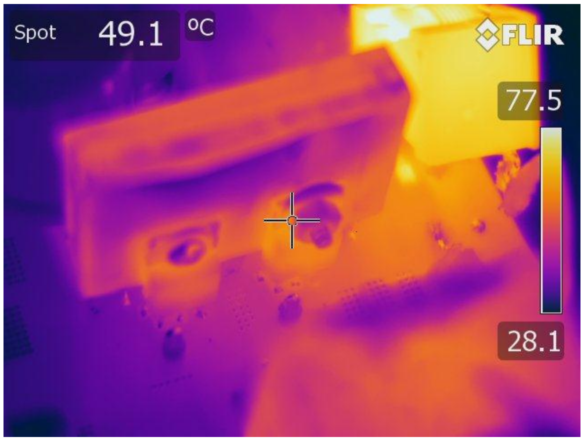

Figure 68 – Thermals, Primary MOSFET

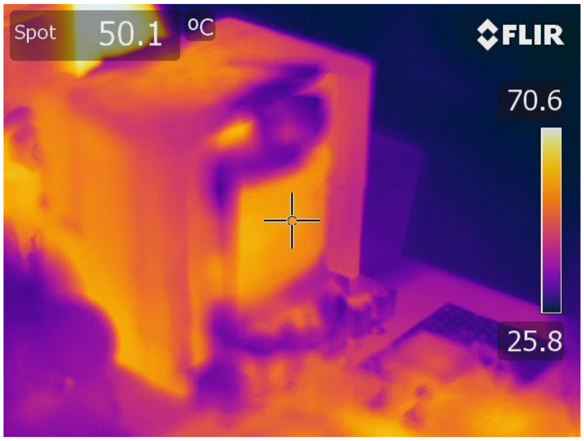

Figure 69 – Thermals, Transformer

APPENDIX I –SCHEMATICS (MAIN, DAUGHTER CARD, AND TOPLEVEL)

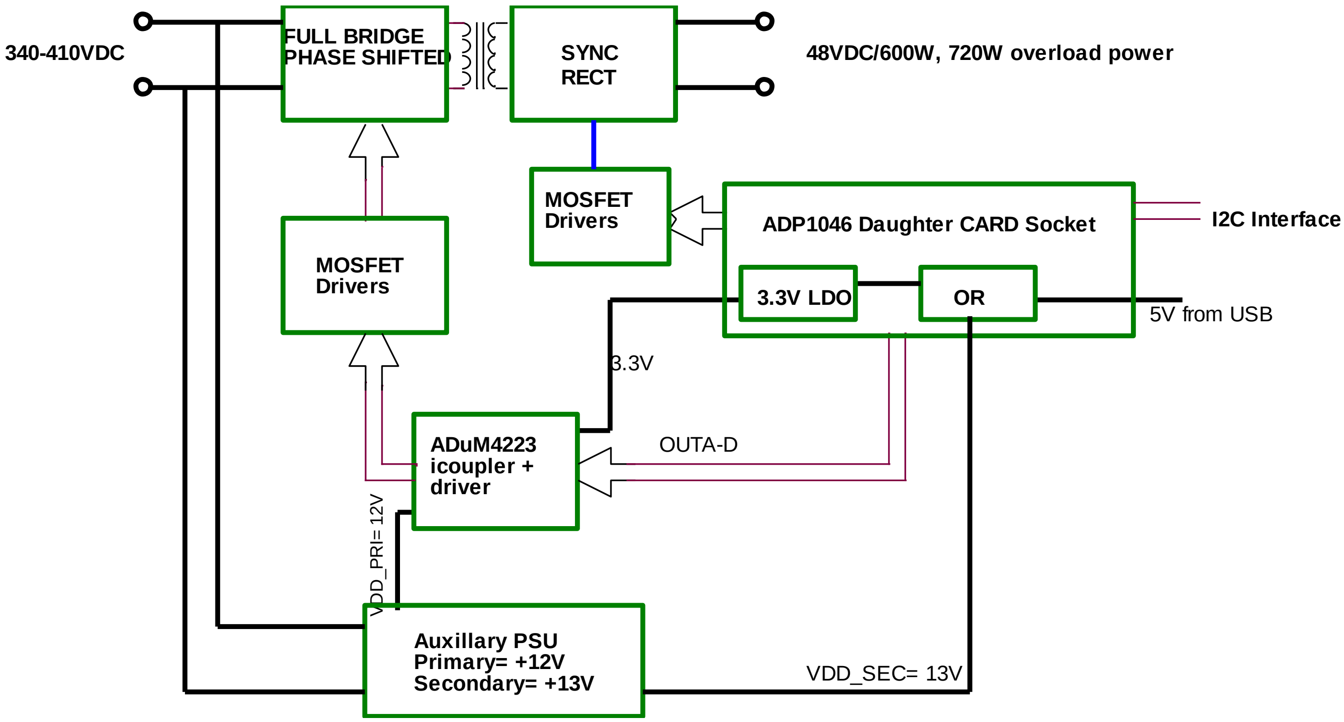

Figure 70 – Schematic – Top Level Schematic

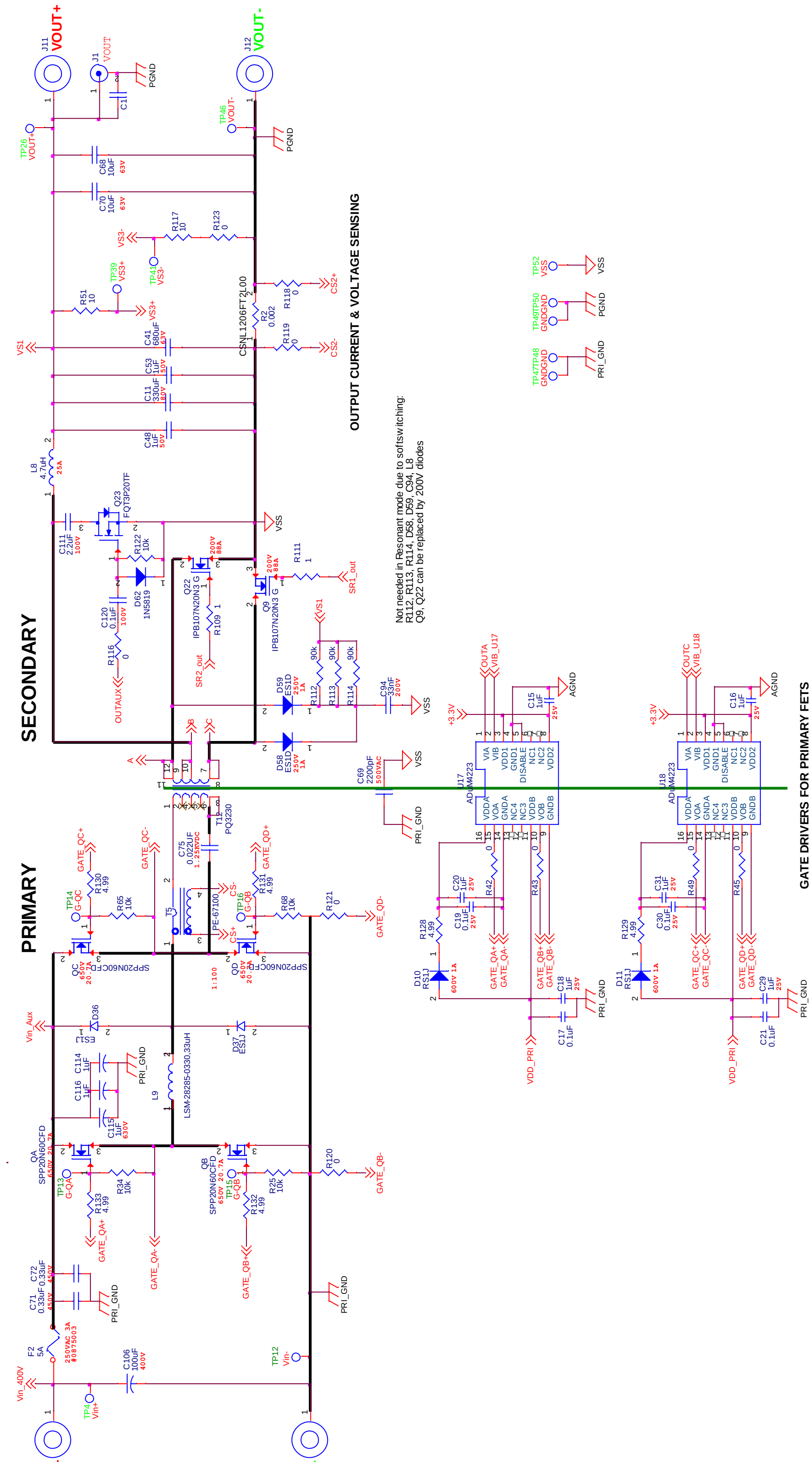

Figure 71 – Schematic – Main power train

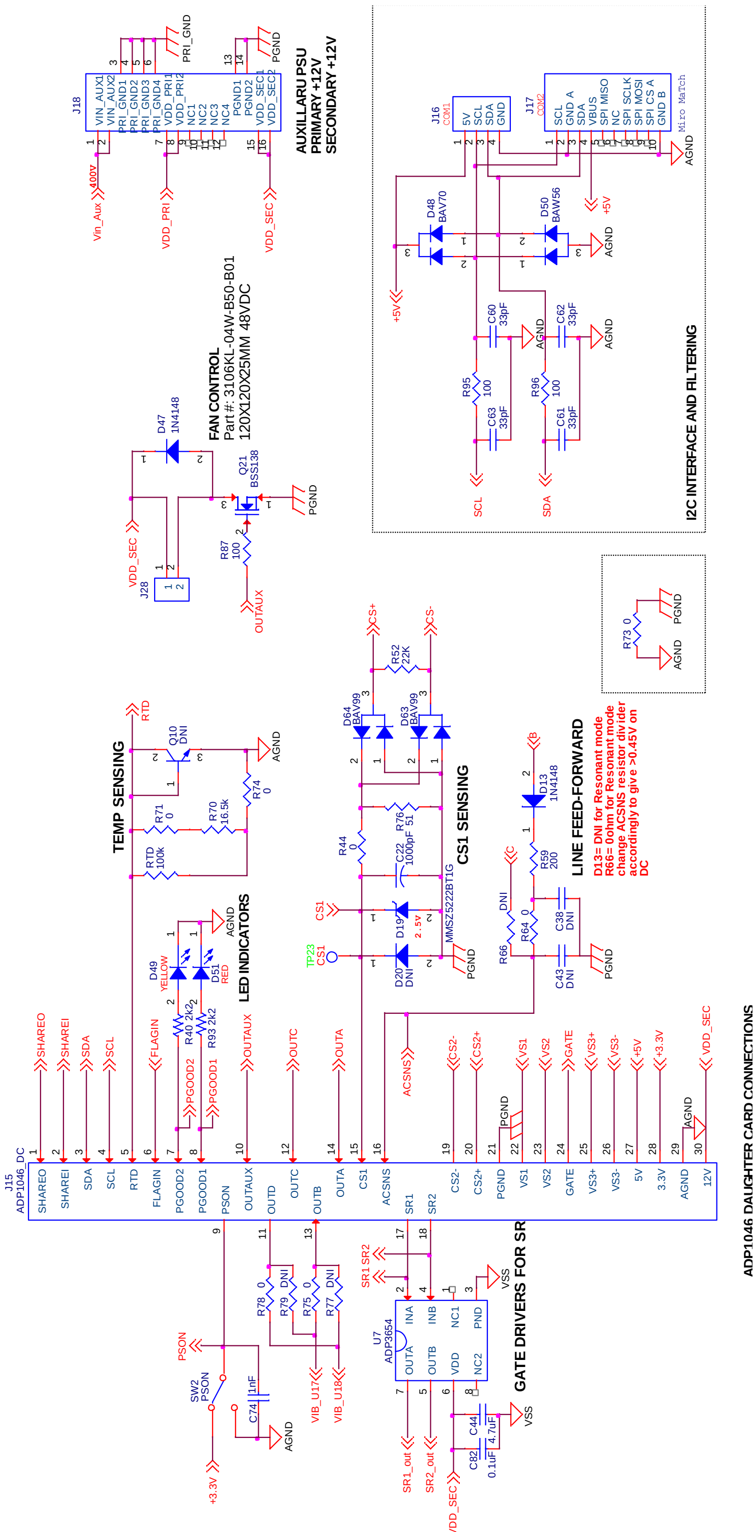
ADP1046 DAUGHTER CARD CONNECTIONS
GATE DRIVERS FOR SR
TEMP SENSING
LED INDICATORS
CS1 SENSING
LINE FEED-FORWARD
D13= DNI for Resonant mode
R66= 0ohm for Resonant mode
change ACSNS resistor divider
accordingly to give >0.45V on
DC
FAN CONTROL
Part #: 3106KL-04W-B50-B01
120X120X25MM 48VDC
AUXILLARU PSU
PRIMARY +12V
SECONDARY +12V
I2C INTERFACE AND FILTERING

Figure 72 – Schematic – Miscellaneous

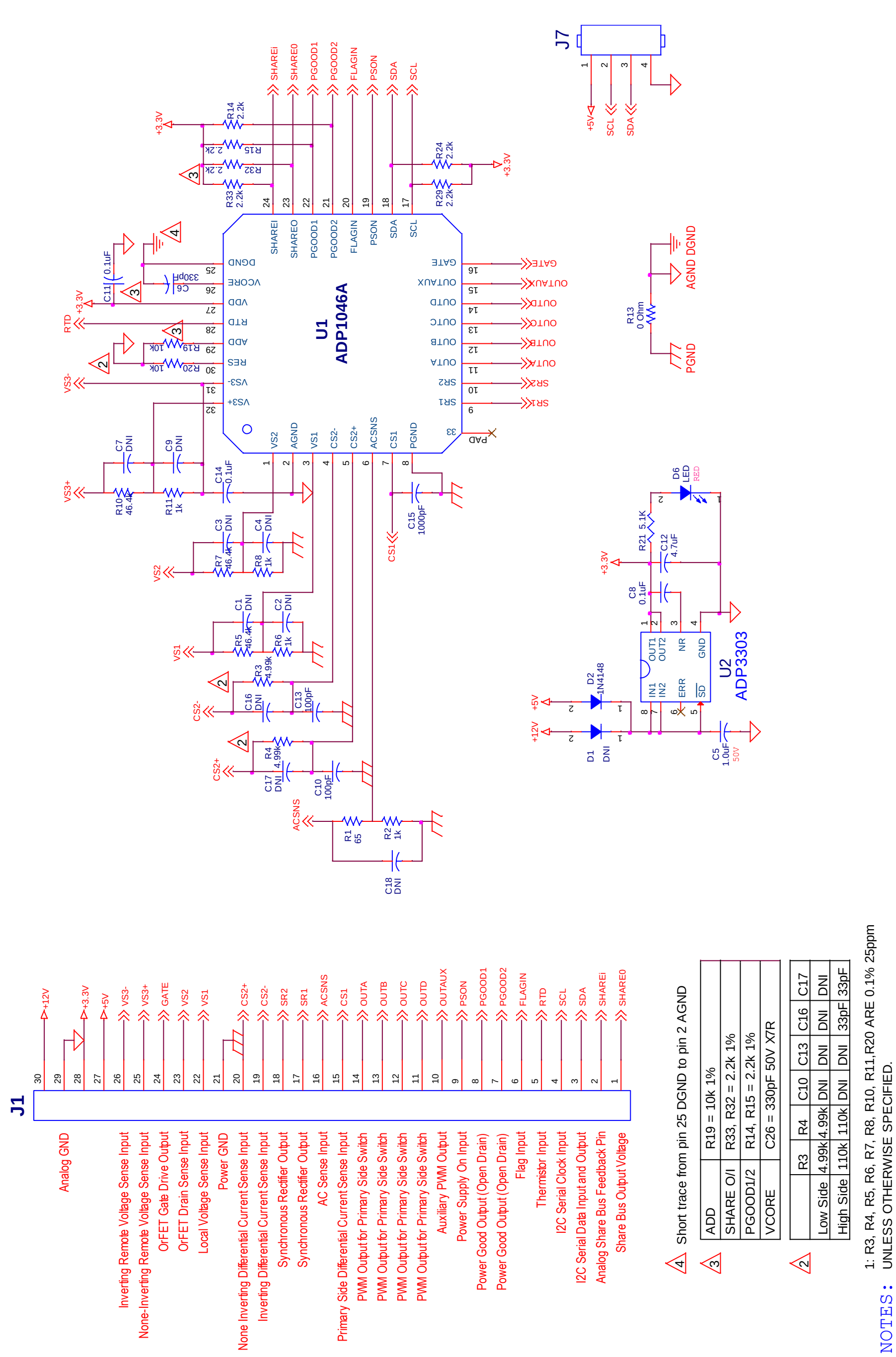

Figure 73 – Schematic – ADP1046A daughter card

APPENDIX IV – LAYOUT

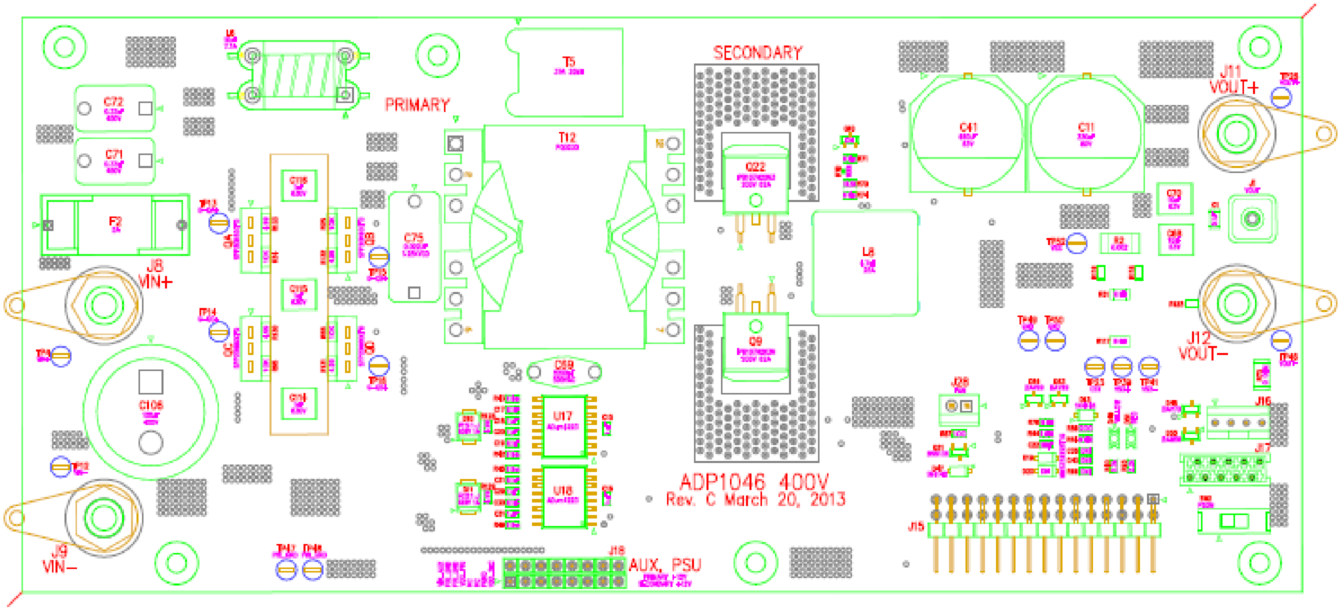

Figure 74 – Top side placement of components

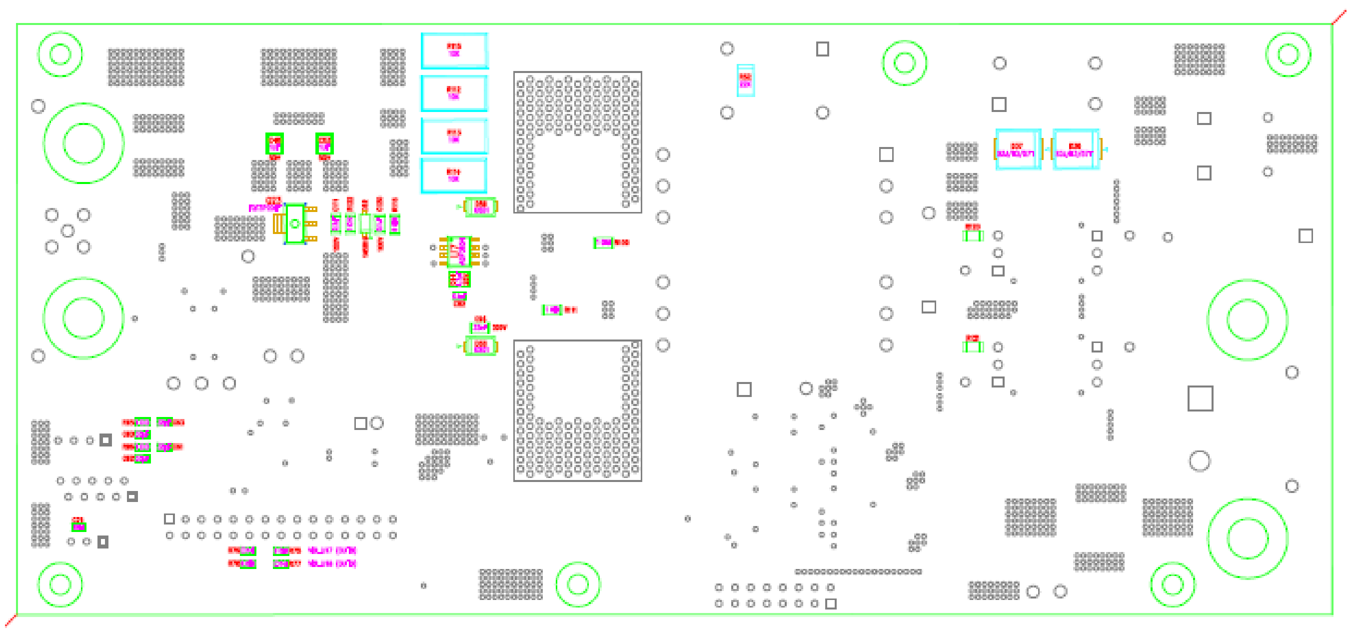

Figure 75 – Bottom side placement of components

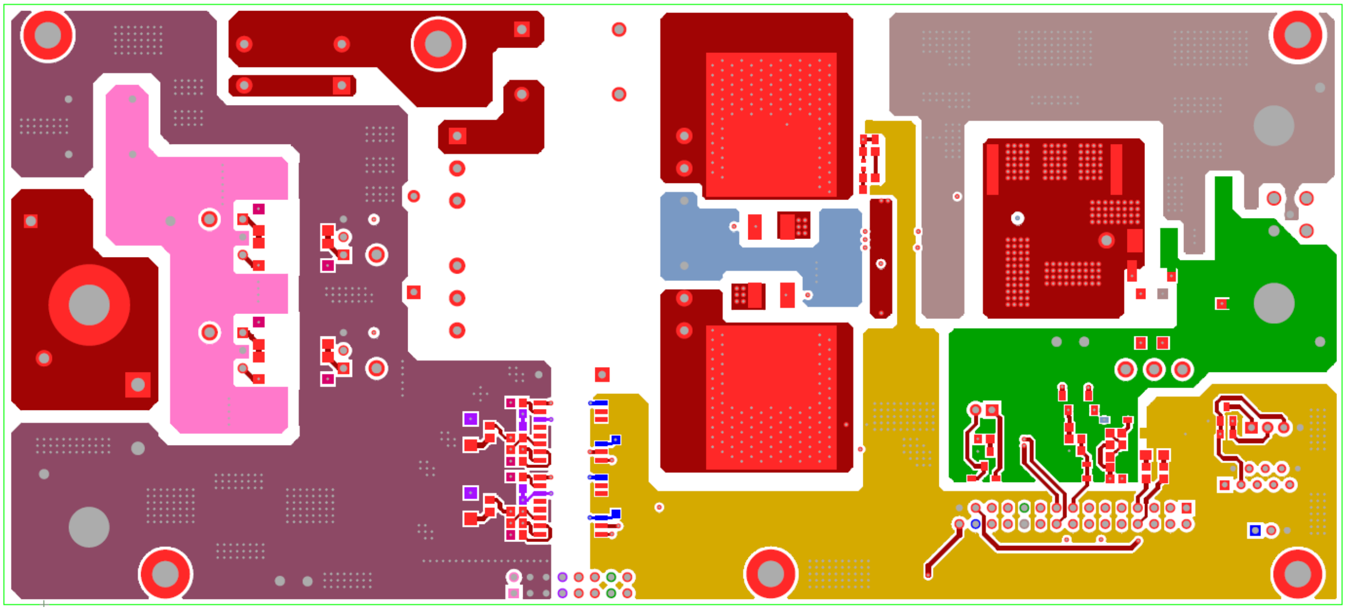

Figure 76 – Layout Layer 1

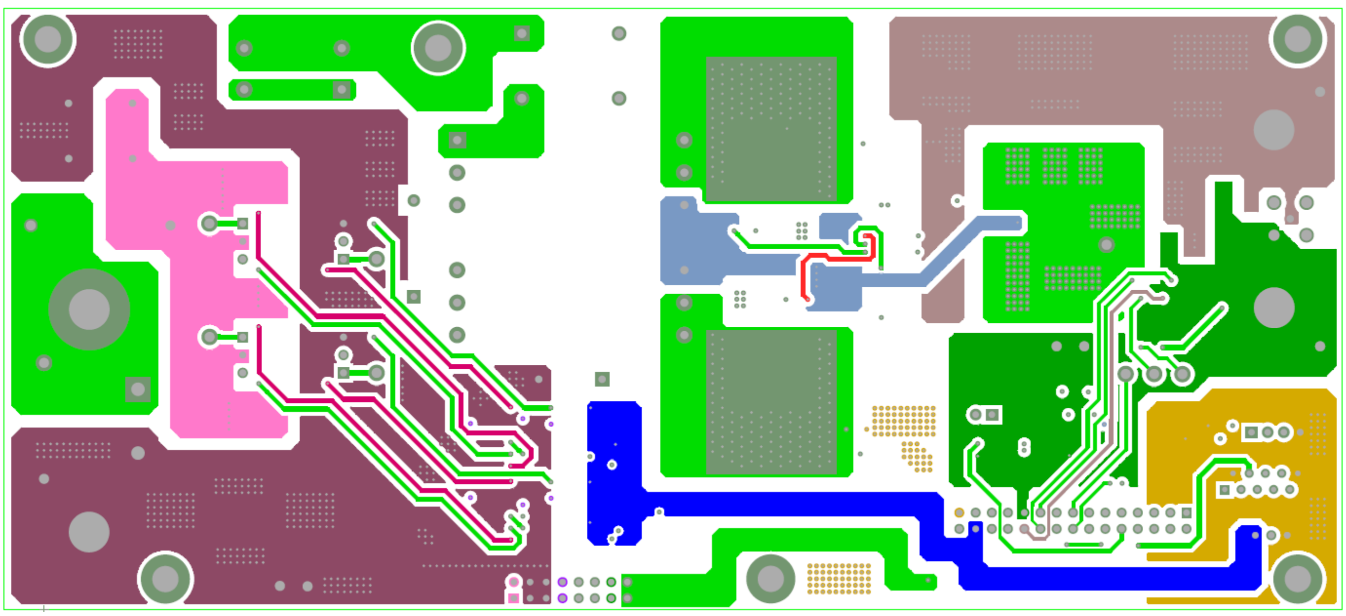

Figure 77 – Layout Layer 2

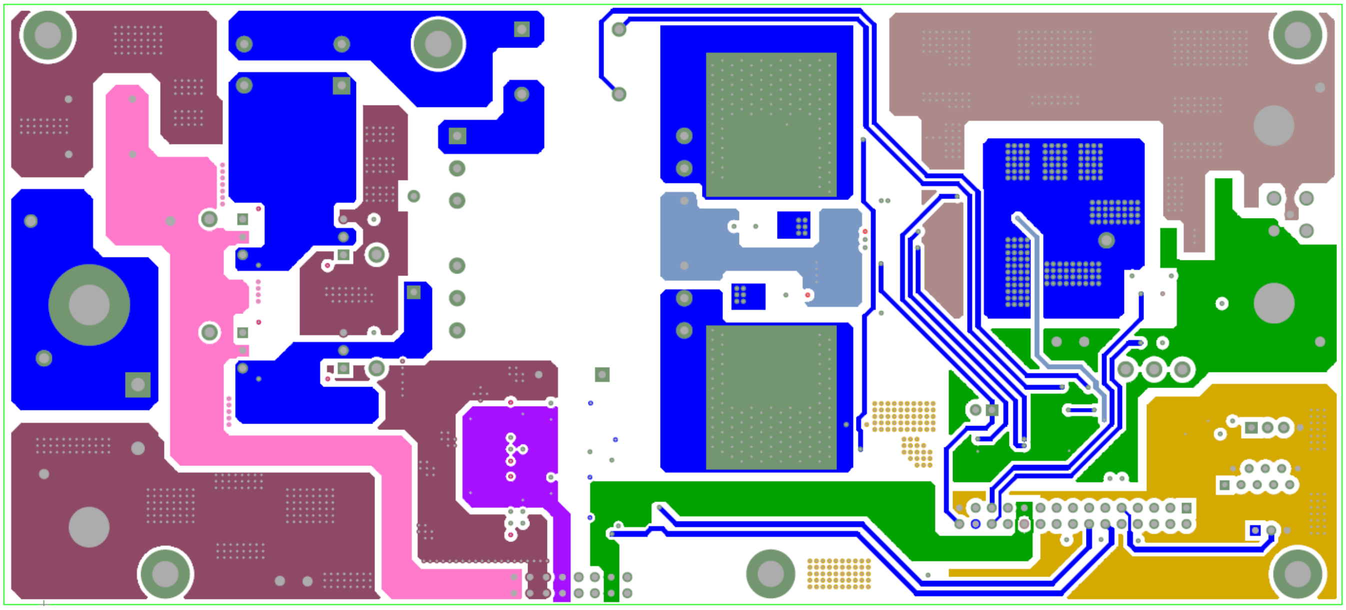

Figure 78 – Layout Layer 3

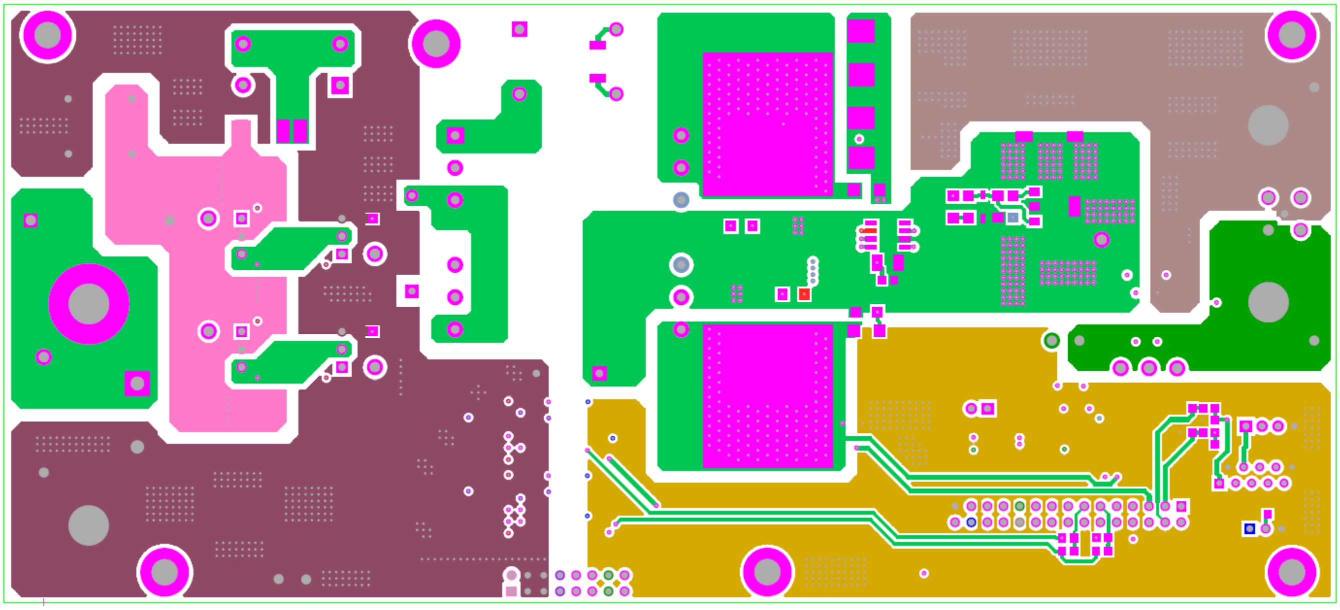

Figure 79 – Layout Layer 4

NOTES

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