ANALOG DEVICES

ADP1055-EVALZ User Guide
UG-710

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Evaluating the 240 Watts ADP1055 Digital Controller for Isolated Power Supply with PMBus Interface

FEATURES

- Full support evaluation kit for the ADP1055
- 240 W full bridge topology (adjustable to phase shifted full bridge topology)
- Rated power of 12 V dc, 20 A
- PMBus Revision 1.2 compliant with PEC and extended manufacturer specific commands
- 32-bit password protection with command masking
- 64 address selections (16 base addresses, expandable to 64)
- 6 PWM control signals, 625 ps resolution
- Duty cycle double update rate
- Fast line voltage feedforward
- Redundant programmable OVP
- Frequency synchronization
- Soft-start and soft-stop functionality
- Droop current sharing
- On-board tests for housekeeping functions
- PMBus communication
- Software GUI

EVALUATION KIT CONTENTS

- ADP1055-EVALZ evaluation board
- ADP1055DC1-EVALZ daughter card

ADDITIONAL EQUIPMENT NEEDED

- The USB-I²C connector, ADP-I2C-USB-Z, with Driver CD (must order separately from Analog Devices, Inc.)

GENERAL DESCRIPTION

This evaluation board, together with a daughter card, allows you to evaluate the ADP1055 as a power supply application. With the USB to I²C connector, and the graphical user interface (GUI), the ADP1055 on the evaluation board can be interfaced with a PC via a USB port.

The evaluation board is set up to act as an isolated PSU with a rated load of 12 V, 20 A from a 38 V dc to 60 V dc source.

Connectors on the evaluation board provide synchronization, as well as share bus and PMBus™ interfaces, allowing direct parallel evaluation when multiple evaluation boards are connected in parallel to a common bus.

Multiple test points allow easy access to all critical points/pins.

EVALUATION BOARD SETUP

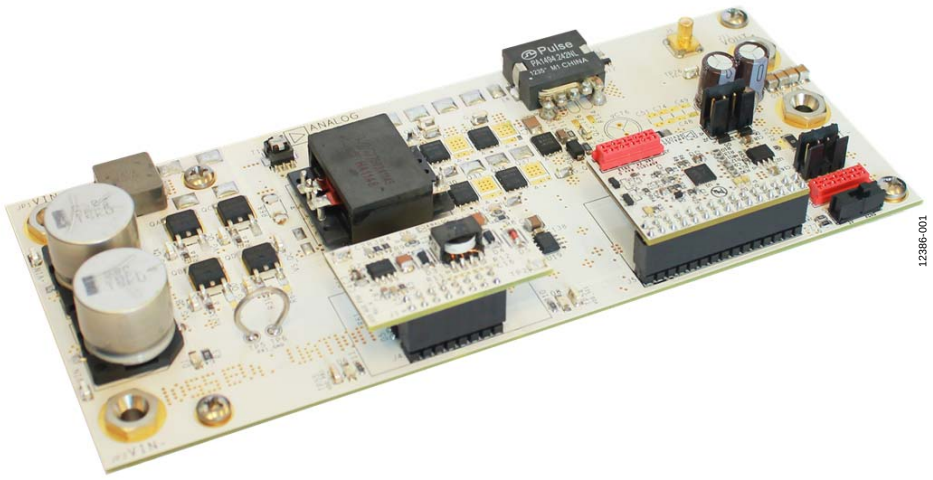

Figure 1. ADP1055 Evaluation Board

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REVISION HISTORY

4/15—Rev. A to Rev. B

Changes to Figure 91 ... 31
Changes to Figure 92 ... 32
Changes to Table 5 ... 39

2/15—Rev. 0 to Rev. A

Added Figure 47; Renumbered Sequentially ... 16
Changes to Figure 83 Caption and Figure 84 Caption ... 23
Changes to Figure 85 Caption and Figure 86 Caption ... 24
Change to Figure 92 ... 32
Change to Table 5 ... 39

6/14—Revision 0: Initial Version

EVALUATION BOARD OVERVIEW

This ADP1055-EVALZ evaluation board and ADP1055DC1-EVALZ daughter card feature the ADP1055 in a dc-to-dc switching power supply in full bridge topology with synchronous rectification operating at 125 kHz switching frequency.

Figure 4 shows the block diagram of the evaluation board. The circuit is designed to provide a rated load of 12 V, 20 A from a dc input voltage source of 38 V dc to 60 V dc. The ADP1055 provides functions, including output voltage regulation, synchronization, constant current control, pre-bias start up, and comprehensive protection functions.

The evaluation kit consists of a power board, daughter card, and the auxiliary circuit board.

POWER BOARD AND POWER TRAIN OVERVIEW

The power board is shown in Figure 1. Referring to the Schematics and Artwork section, the circuit components are described as follows. The primary and secondary H bridges are formed with MOSFETs QA through QD (primary side) and MOSFETs Q30, Q34, Q38, and Q40 (secondary side). Transformer T2 provides the isolation. The output filter consists of L8 and a capacitor bank (C48, C49, C51, C70, C73, and C74). This is the main power stage. The active snubber is made up of clamp capacitor C192, MOSFET Q23 (pMOS), and driver U19.

Additional circuitry around the power train is described as follows. The input filter consists of a single state LC (L10 and C6-13). Components U2 and U5 are half bridge 4 A drivers based on the Analog Devices, Inc., *i*Coupler technology that provides gate drive for driving the primary H bridge. Secondary side H bridge drivers consist of U20 and U21.

The primary current is sensed using a current transformer T1 that provides primary fast and accurate over current protection whereas the secondary side current (that is, the load current) is sensed using a sense resistor (R5, R9).

ADP1055 DAUGHTER CARD

The daughter card is shown in Figure 2. The ADP1055 daughter card consists of a 3.3 V LDO that powers the ADP1055 IC. The PWMs for the primary switches (OUTA to OUTD) and for the secondary switches (SR1 and SR2) are connected from the daughter board to the power board

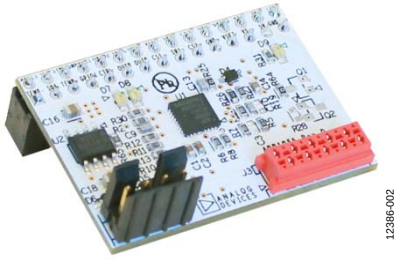

Figure 2. ADP1055 Mounted on Daughter Card

AUXILARY POWER BOARD CIRCUIT

The auxiliary power board, included in the kit, is shown in Figure 3. The auxiliary power circuit provides 9 V on the primary side and 9 V and 5 V (derived using a Zener diode) on the secondary side. The approximate minimum operating voltage of the auxiliary power board is 30 V.

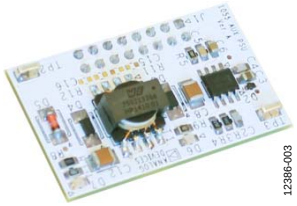

Figure 3. Auxiliary Power Board

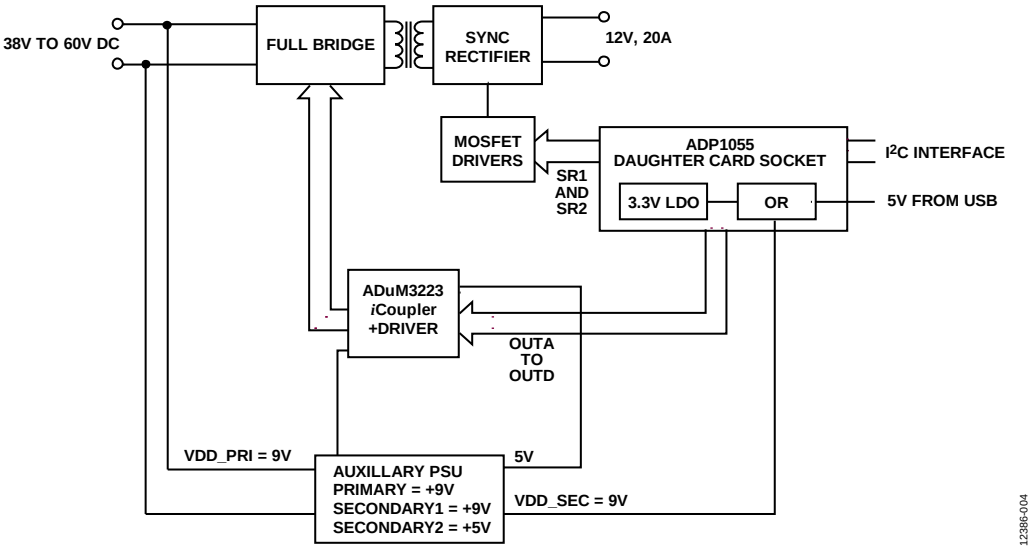

Figure 4. ADP1055-EVALZ Evaluation Board Block Diagram

APPLICATIONS

High efficiency, high power density, isolated dc-to-dc power supplies include

- Intermediate bus converters
- Paralleled power supply systems
- Server, storage, industrial, networking, and infrastructure

CONNECTORS

The connections to the ADP1055-EVALZ evaluation board are shown in Table 1. Table 2 shows the details about these connectors.

Table 1. Evaluation Board Connections

Connector	Function
JP1	VIN+, dc Input
JP2	VIN−, ground return for dc input
J12	VOUT+, dc output
J12	VOUT−, return for dc output
J5	ADP1055 daughter card connector
J6, J7	I²C connector
J4	Auxiliary power board connector

I²C/PMBus Connector on ADP1055 Daughter Card

Table 2. J6 Connections (Left to Right)

Pin	Function
1	5 V
2	SCL
3	SDA
4	AGND

SPECIFICATIONS

Table 3. Evaluation Board Connection Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comment
Input Voltage	V_{IN}	38	48	60	V	
Output Voltage	V_{OUT}		12		V	
Output Current	I_{OUT}			20	A	
Operation Temperature	T_A		25	50	°C	Natural convection
			25	85	°C	Airflow = 200 LFM or above
Efficiency	η		94		%	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A
Switching Frequency	f_{sw}		125		kHz	
Output Voltage Ripple			200		mV	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A
Dimension						Excluding standoff
Length			7.12		in	
Width			3.06		in	
Component Height			0.7		in	

GETTING STARTED

CAUTION

This evaluation board uses high voltages and currents. Extreme caution should be taken, especially on the primary side, to ensure your safety. It is strongly advised to switch off the evaluation board when not in use. A current limited, isolated dc source is recommended at input.

HARDWARE

Evaluation Equipment

- DC power supply capable of 38 V dc to 60 V dc, 10 A.
- Electronic load capable of 12 V, 25 A input.
- Oscilloscope capable of 500 MHz bandwidth or above, 2 to 4 channel.
- PC with Microsoft Windows® XP (32 bit), or Vista (32 bit), Windows 7 (32/64 bit), and Windows 8 (32 bit).
- Precision digital multimeters (HP34401 or equivalent).
- USB to I²C connector ADP-I2C-USB-Z as shown in Figure 5. This must be ordered from Analog Devices.
- Portable DMM (Fluke Corp.) for measuring up to 25 A dc current (optional).

Evaluation Board Configurations

The evaluation board is preconfigured with the default settings to operate the power supply at the rated load. No additional configuration is necessary other than to turn on the hardware PSON switch. Additional software configuration may be necessary to change thresholds and parameters.

Hardware Connection

Figure 6 shows an example of the test configuration of the hardware.

Figure 5. USB to I²C Interface Connector ADP-I2C-USB-Z

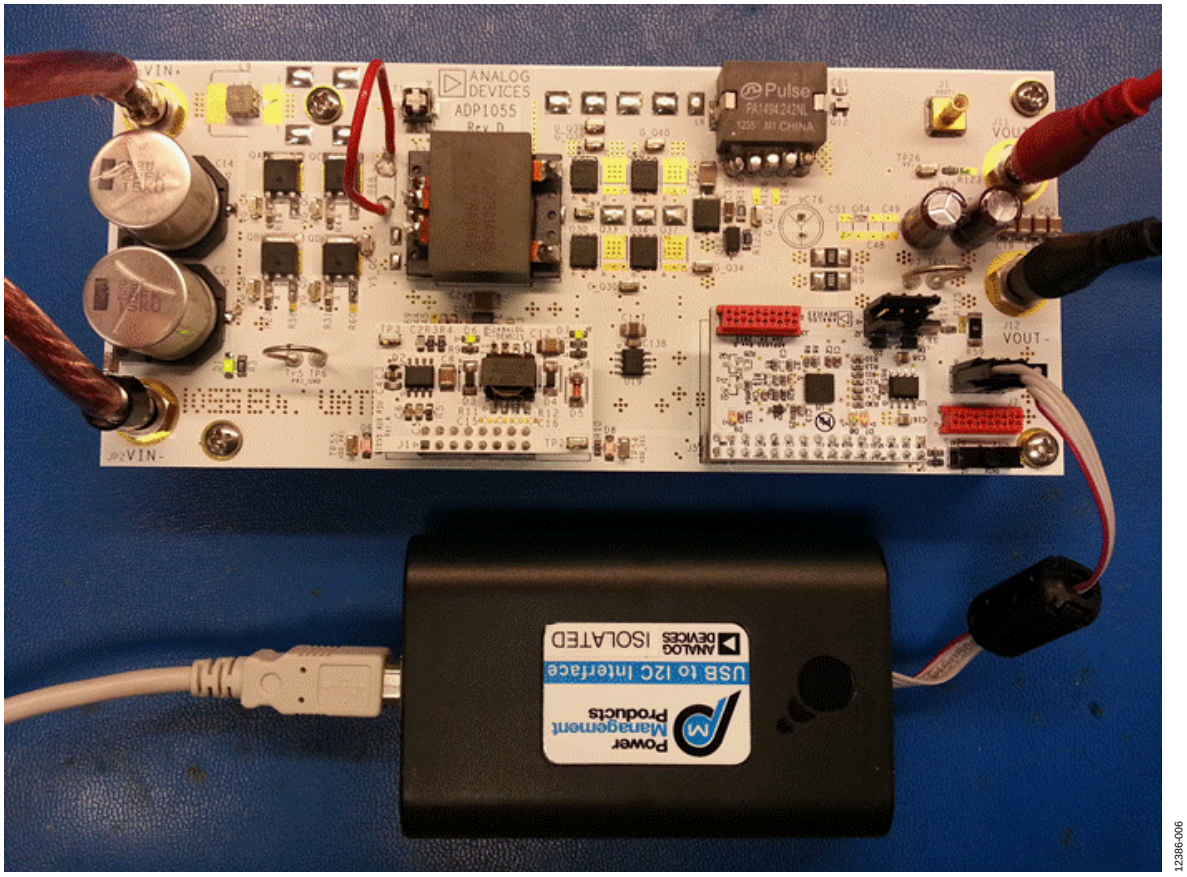

Figure 6. Test Configuration for the Evaluation Board

SOFTWARE GUI

Overview

The ADP1055 GUI is a free software tool for programming and configuring the ADP1055. It can be downloaded from the ADP1055 product page by clicking on the **Design Tools, Models, Drivers & Software** tab.

GUI Installation

Connect the USB cable to the evaluation board only after the software has been installed.

1. Install the ADP1055 software GUI. Double-click the **ADP1055 Setup.msi** installation file to start the installation. Click **Next**.

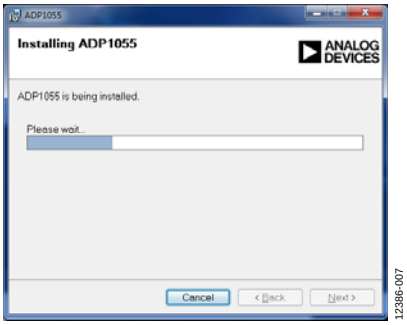

Figure 7. GUI Installation

2. When the **Total Phase USB Setup** window appears, click **Next**. Read the license agreement, check **I accept the terms in the License Agreement**, and then click **Next**.
   - Check the **Install USB driver** option if the driver is not installed.
   - If the driver is installed, uncheck the **Install USB driver** option. Then, click **Install**. After the installation, click **Close** to complete the driver installation.

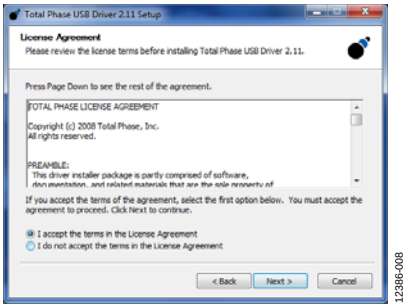

Figure 8. I²C Driver Installation

3. When the **Adobe Flash Player Installer** window appears, check **I have read and agree to the terms of the Flash Player License Agreement** after reading it. Then, click **Install** and then **Done** to exit setup.

A pop-up window shows a notification of successful installation.

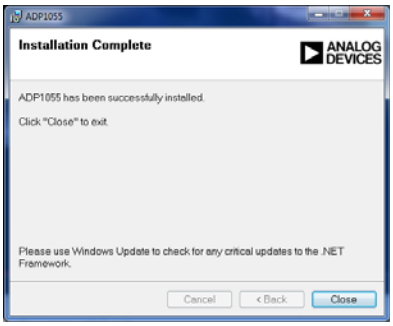

Figure 9. Successful GUI Installation

Launching the GUI

1. Ensure that the evaluation board, the auxiliary power board, and the daughter card are already plugged into the main power board. If they are mishandled during shipment, ensure that they are properly attached as per Figure 1.
2. Ensure that the CTRL switch or hardware PSON (SW2) is turned to the Off position (switch position on the right).
3. Plug one end of the USB to I²C adapter in Jumper J6 or in the connector on the daughter card, and plug the other end in the USB port of the PC.
4. Launch the ADP1055 GUI. The software GUI should report that the ADP1055 has been located with the address. Click **Finish** to proceed.

Figure 10. Address Detection of ADP1055

5. The ADP1055 in the evaluation kit is preprogrammed with the board and command settings, so this step is optional. If you want to load the default command and board settings file from a local folder, click the **Load Command and Board settings from a '.55s' file to ADP1055** icon.

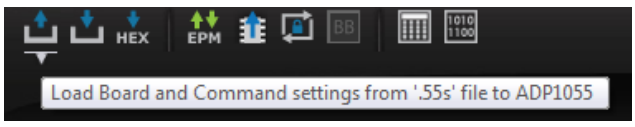

Figure 11. Leftmost Icon Shows Loading of .55s Settings File

6. Select the **ADP1055240W.55s** file. For more information about the ADP1055 GUI, refer to the ADP1055 GUI user guide by clicking on the leftmost question mark icon in the top section of the GUI.

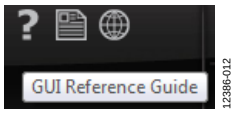

Figure 12. Leftmost Icon Shows GUI Reference Guide

POWERING UP

1. Connect a dc source (voltage range of 38 V dc to 60 V dc) at the input terminals and an electronic load at the output terminals. Refer to Figure 6 for the correct configuration.
2. Connect voltmeters on the input terminals and output terminals separately as shown in Figure 6.
3. Connect the voltage probes at different test pins. Ensure that the differential probes are used and that the ground of the probes are isolated if the measurements are made on the primary and secondary side of the transformer simultaneously.
4. Set the electronic load to 5 A.
5. Turn the CTRL switch (SW2) to the On position.

The evaluation board should now be up and running, and ready for evaluation. The output should now read 12 V dc.

After successful startup when the PSU is in steady state condition, LEDs provide the status of the board.

Table 4. LED Indicators on the Evaluation Board

LED	Function
D1	Input voltage
D6 (Auxiliary Board)	Auxiliary 9 V voltage on primary side
D7	Auxiliary 9 V voltage on secondary side
D9	3.3 V that powers ADP1055 IC
D7 (Daughter Board)	GPIO1
D9 (Daughter Board)	GPIO2

After completing the programming of the ADP1055, click the **Program command and board contents into EEPROM** icon to program the command and board settings into EEPROM to save the settings in the part.

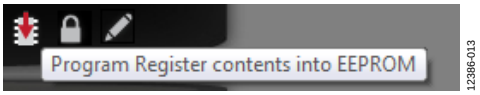

Figure 13. Leftmost Icon Shows Store to EEPROM Option

Use the **Save Command and Board settings from ADP1055 to a '.55s' file** icon to generate a .55s file to save the commands and board settings.

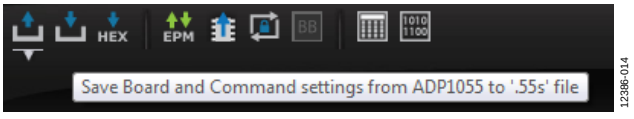

Figure 14. Second Icon from the Left Shows Save to File Option

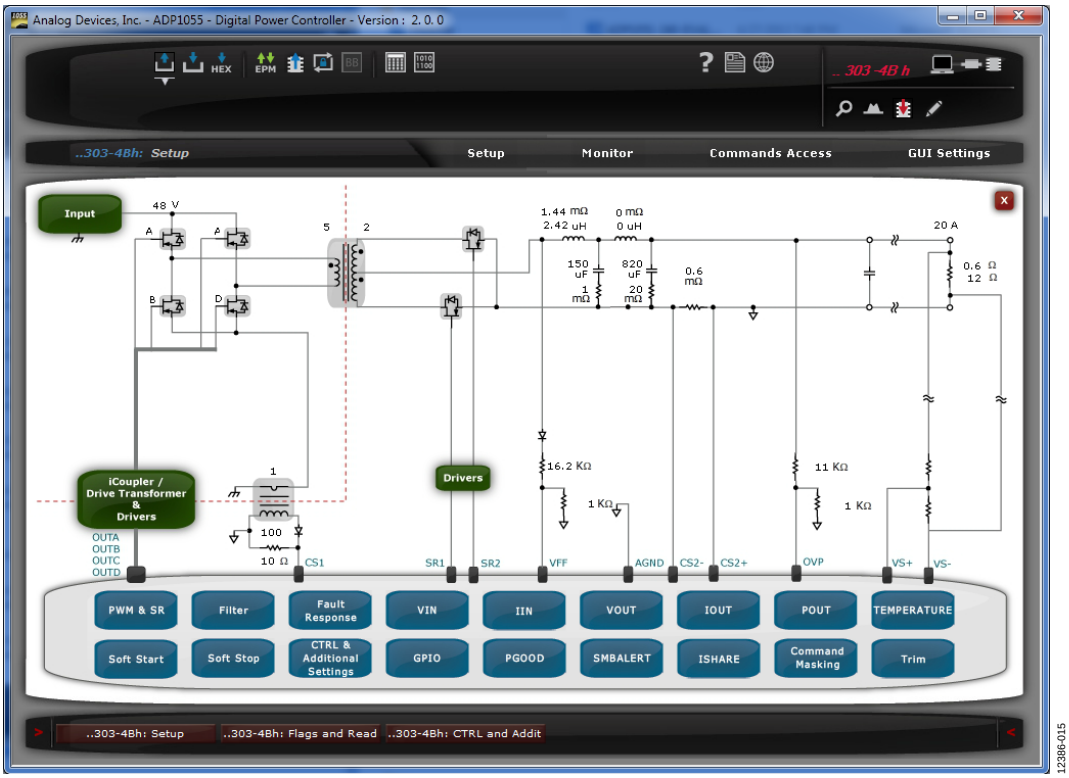

Figure 15. Main Setup Window of the ADP1055 GUI

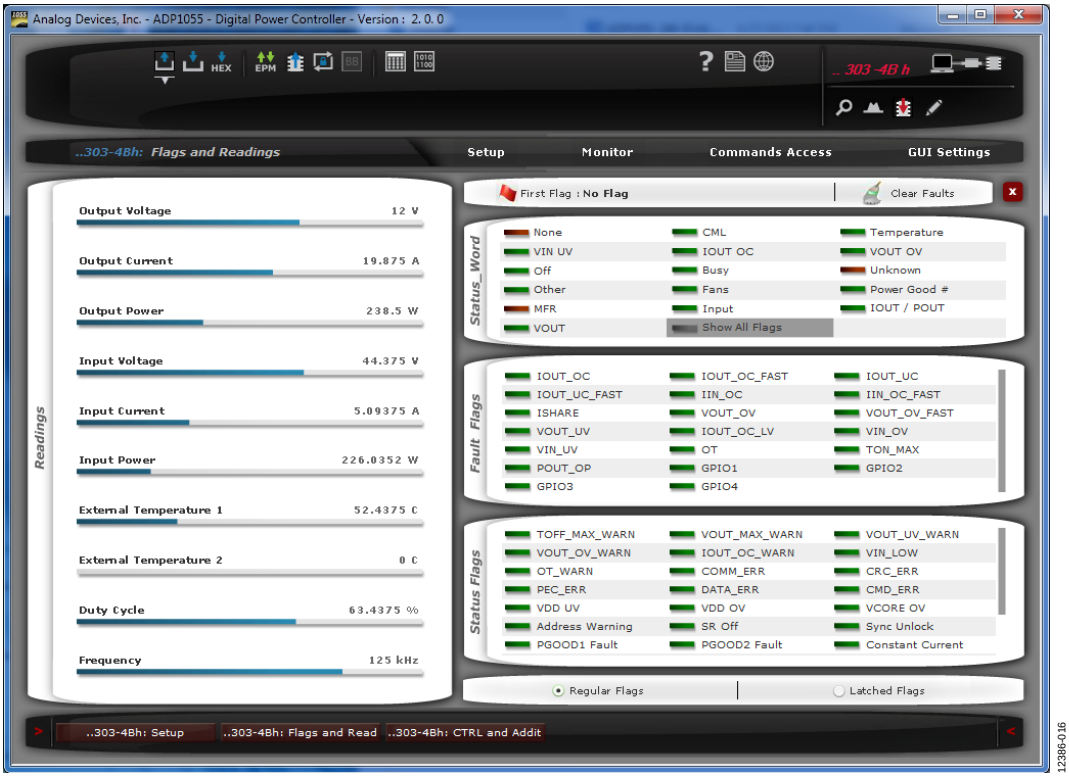

Figure 16. Monitor Window in the GUI

For more information on the board settings, refer to the GUI reference guide (see Figure 12).

EVALUATING THE ADP1055

The goal of this user guide is to familiarize you with the GUI and to describe the flexibility available with the extensive programming options provided by the ADP1055. Several test points on the evaluation board allow easy monitoring of the various signals. You can use the GUI software to program multiple responses for the various fault conditions. The following sections provides a description of the typical features and results realized when evaluating this device.

PWM AND SR WINDOW

The PWM and SR window shows the PWM settings for the switches on the primary side and the synchronous rectifier in the **General** tab at the top left corner of the window. Other tabs program the **Modulating Edges**, prevent transformer saturation (**Volt Second Balance**), and perform other functions as described in this section of the user guide (**Sync**, **Snubber**, and **Adaptive Dead Time**). This tab programs the switching frequency, SR phase in speed, pulse skipping, maximum duty cycle, and so on.

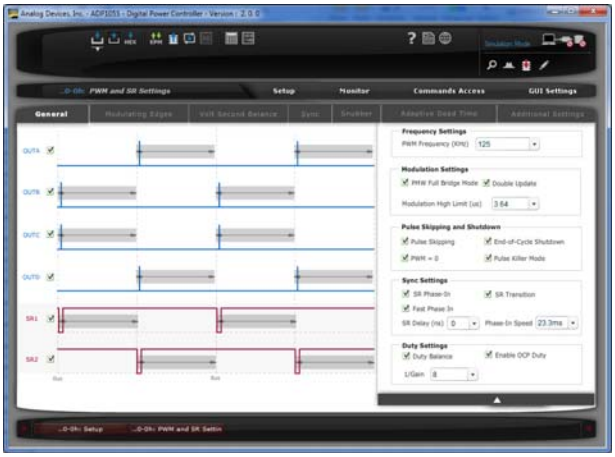

Figure 17. PWM and SR Window (Full Bridge Hard Switching)

Note the following:

- All the signals shown in Figure 17 represent the signals at the output pins of the IC.
- Although the switching frequency can be increased, the software does not account for the dead times; these have to be programmed manually by measuring the propagation delays between the output of the ADP1055 and the gate of the MOSFET. A 200 ns delay is conservative for the evaluation board.

In Figure 17, a typical PWM configuration for a full bridge hard switching topology is provided with modulation on the falling edges of OUTA to OUTD and on the rising edge of SR1 and SR2. The synchronous rectifiers in light load mode (LLM) have an independent setting as shown in Figure 18.

Figure 18. SR1 and SR2 in Light Load Mode (LLM)

The PWM window can be used to set up several different topologies, notably the full bridge phase shifted topology whose PWM settings are shown in Figure 19.

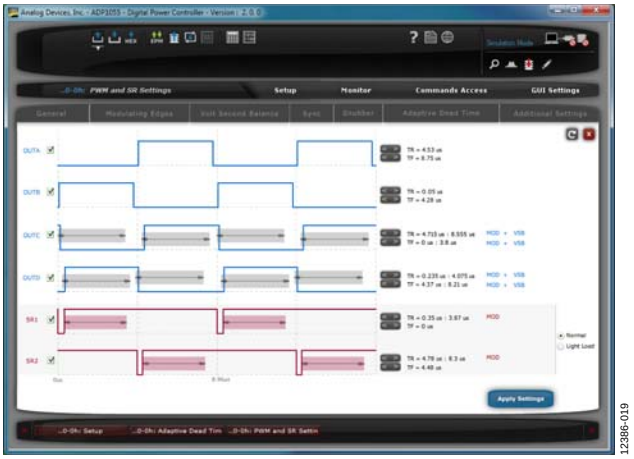

Figure 19. PWM and SR Window (Full Bridge Phase Shifted)

The PWM settings can be changed in a simple drag-and-drop fashion or by checking/unchecking the respective function. The **Apply Settings** button is highlighted in red whenever a change is made. Changes take place after **Apply Settings** is clicked and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

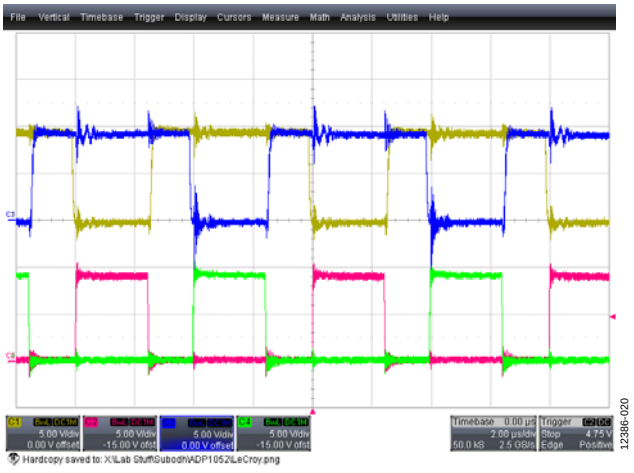

Figure 20. PWM Example Under 10 A Load
Top 2 Waveforms: SR1 and SR2
Bottom 2 Waveforms: OUTB and OUTD

Volt Second Balance Tab

Refer to the ADP1055 data sheet for detailed operation and manual setup of the volt second balance feature.

It is recommended to use the **Auto Setup** feature to setup the PWMs in hard switching mode.

For full bridge phase shifted topology, use the settings shown in Figure 21.

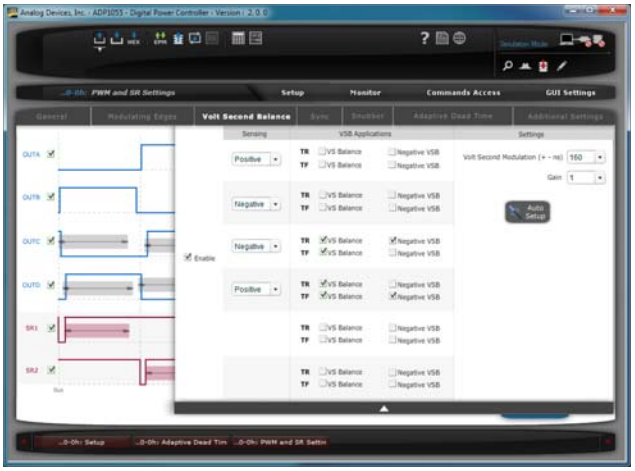

Figure 21. PWM and SR Window (Full Bridge Phase Shifted)

What follows is an example that shows the effectiveness of the volt second balance feature. A deliberate extra on time was added to one leg of the H bridge creating an imbalance in the transformer.

Figure 22. 100 ns Extra On Time Added to OUTB and OUTC

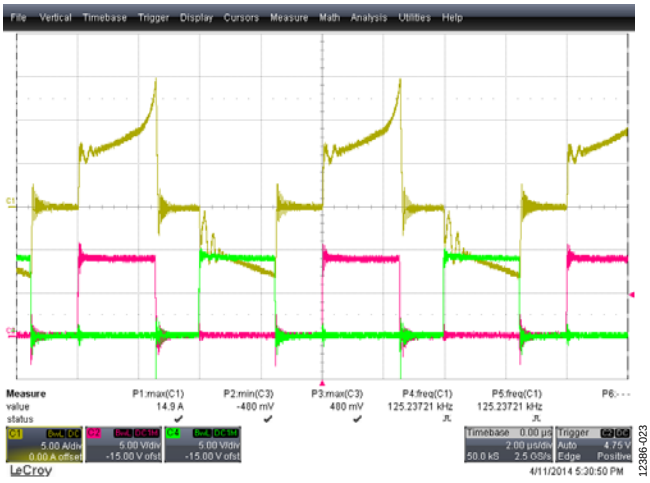

Figure 23. Volt Second Balance Disabled, Duty Balance Disabled
Yellow Trace: Primary Current, 5 A Div
Red and Green Trace: OUTB and OUTD

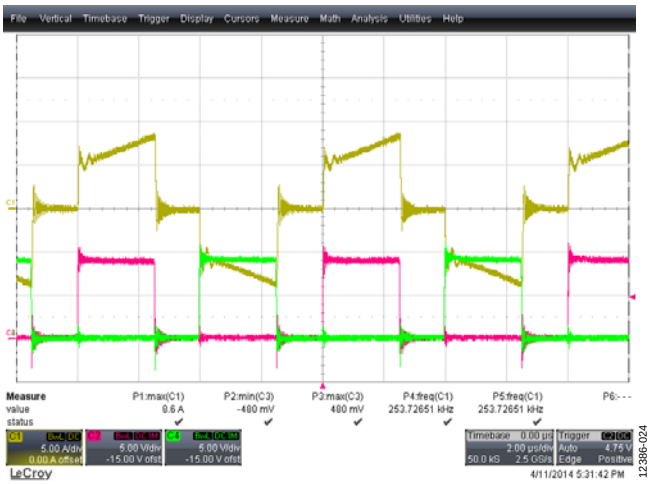

Figure 24. Volt Second Balance Enabled, Duty Balance Disabled
Yellow Trace: Primary Current, 5 A/Div
Red and Green Trace: OUTB and OUTD

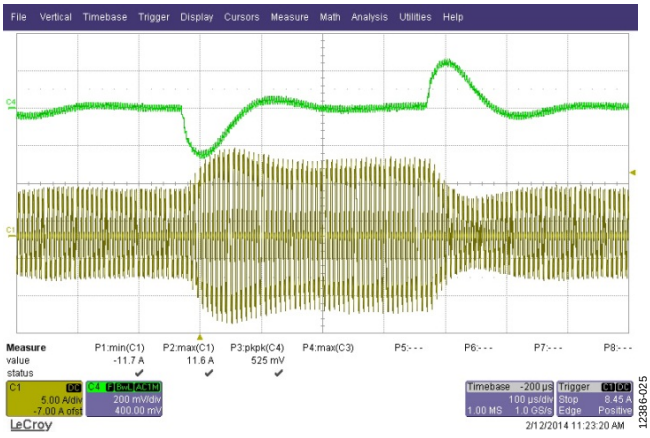

Figure 25. Volt Second Balance During 25% Load Transient

Synchronization Tab

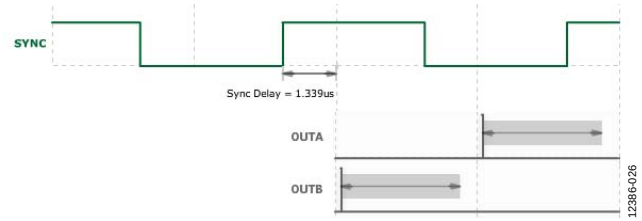

Figure 26. Phase Delay Between SYNC Pulse and PWM Timing

The phase delay, that is, the alignment of the PWM set (OUTA to OUTD and SR1, SR2) with synchronization pulse can be programmed in this tab. For a full description of the SYNC function, refer to the data sheet.

The SYNC settings can be changed in a simple drag-and-drop fashion. The **Apply Settings** button is highlighted in red whenever a change is made. Changes take place after **Apply Settings** is clicked and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

Adaptive Dead Time (ADT) Tab

See the ADP1055 data sheet for detailed operation of the ADT feature. In the example provided in this section, the GUI has programmed the SR edges to become narrower when the load has decreased to increase light load efficiency.

The ADT settings can be changed in a simple drag-and-drop fashion or by merely checking/unchecking the respective function. The **Apply Settings** button is highlighted in red whenever a change is made. Changes take place after the **Apply Settings** is clicked and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

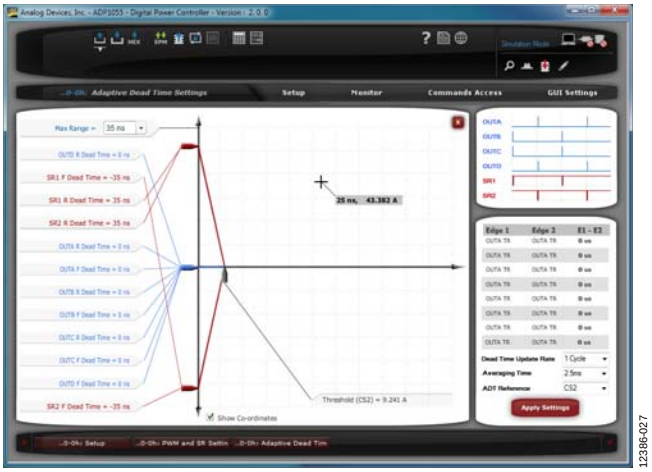

Figure 27. ADT Window

Things to Try

1. Set up PWMs for additional topologies, such as active clamp, isolated boost, and so on.
2. Use the SYNC feature of the ADP1055 to synchronize to an external frequency.

CTRL AND PSON WINDOW

In this window, the configuration of the hardware and software PSON can be programmed. Additional settings, such as the extended slave address selection, voltage overshoot (regulation timeout speed) and write protect mode, can be selected.

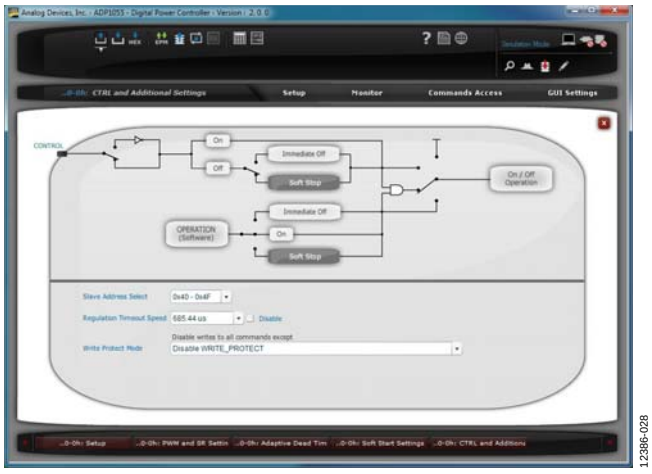

Figure 28. PSON Window

The settings can be changed by simply toggling the switches or by selecting the suitable option from the drop-down menu. Changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

Overshoot Protection (Regulation Timeout) and DIP Test

The ADP1055 provides an overshoot protection feature (regulation timeout). If enabled, a soft-start is run from the precharge function whenever the output voltage is out of regulation for a certain number of switching periods. This prevents the system from overshooting in output voltage, such as in the case of a DIP test where the input voltage dips below nominal and puts the output voltage out of regulation. In Figure 29, the PSU has been given a PSON signal several minutes before the input voltage is above the VIN_UV threshold.

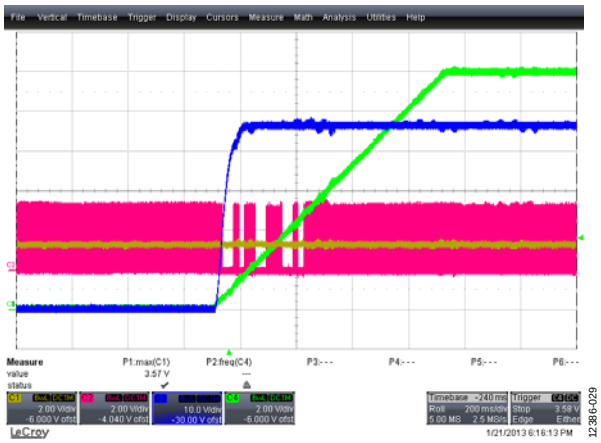

Figure 29. Demonstration of Overshoot Protection at No Load
Green Trace: Output Voltage
Blue Trace: Input Voltage
Red Trace: PWM

SOFT-START WINDOW

This window programs PMBUS functions TON_DELAY, TON_RISE (the soft-start time), and TON_MAX. In the **Additional Settings** tab, several faults can be blanked during soft start and additional features, such as soft start from precharge can be selected.

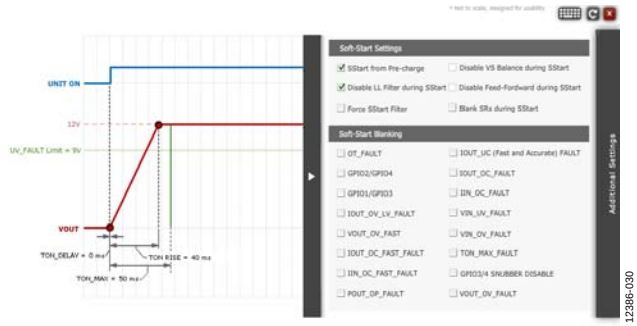

Figure 30. Soft-Start Window

The settings can be changed in a simple drag-and-drop fashion and or by checking/unchecking the checkbox. Changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

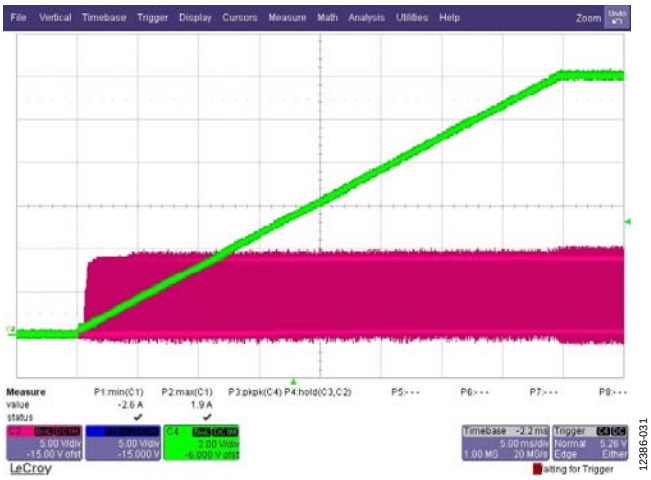

Figure 31. PSU Soft Start at 20 A Load
Green Trace: Output Voltage
Red Trace: PWM

To facilitate a proper soft start from the precharge/prebias condition where the output bus has not yet discharged to zero, the ADP1055 uses the SR phase in and SR transition function to ensure that the output voltage reaches the setpoint value in a monotonic fashion. The SR phase in and SR transition function changes the width of SR1 and SR2 from light load mode setting to the normal mode setting, the setting for continuous conduction mode (CCM), in steps of 5 ns per x switching periods where x ranges from 1 to 1024. This prevents a momentary dip in output voltage when the power supply is turned on.

Figure 32. PSU Soft Start from Precharge
Green Trace: Output Voltage
Blue Trace: Hardware PSON
Yellow Trace: Primary Current

Things to Try

1. Change the soft-start timing in the **Soft-Start** window.
2. Adjust/change the blanking of faults during soft start.

SOFT-STOP WINDOW

Similar to the soft-start window, the soft-stop window features a graphical representation of the TOFF_DELAY, TOFF_MAX, and TOFF_FALL commands. The **Additional Settings** window provides a space to program the blanking of faults during soft stop. Settings for the SR phase in speeds to facilitate soft stop from light load mode are also available here.

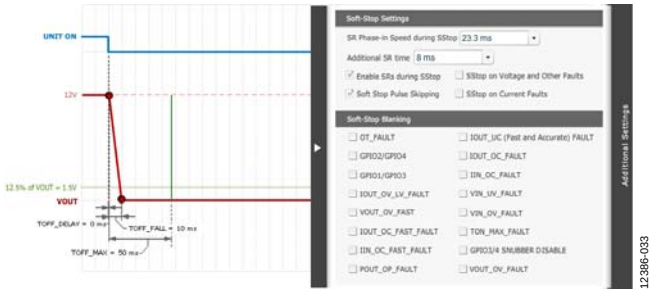

Figure 33. Soft-Stop Window

The settings can be changed in a simple drag-and-drop fashion and or by checking/unchecking the checkbox. Changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

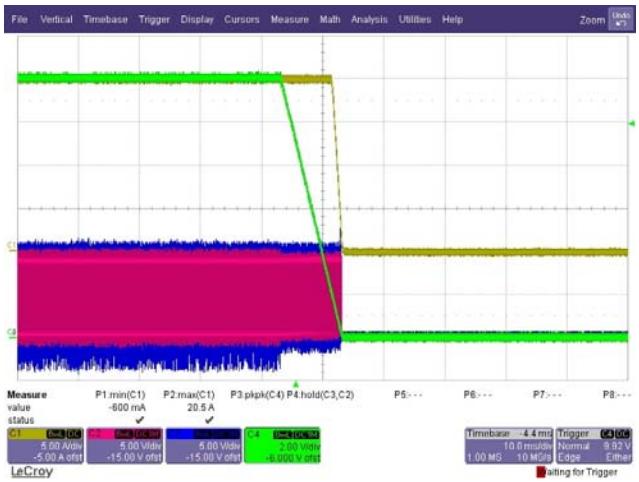

Figure 34. Soft Stop at 20 A Load
Yellow Trace: Load Current
Green Trace: Output Voltage
Red Trace: SR1

When soft stop is initiated from light load mode, SR1 and SR2 are initially off. However, to facilitate soft stop they turn on to discharge the live bus at a controlled rate. The speed at which they turn on and phase in turn soft stop is selectable.

The soft-stop process starts once the SRs have finished phasing in. An additional option of extended SR on time can be selected to ensure that the output voltage stays at 0 V.

Figure 35. Soft Stop from Light Load Mode
Green Trace: Output Voltage
Blue Trace: Hardware PSOFF

Figure 36. Soft Stop with SR on Time Extension (8 ms)
Green Trace: Output Voltage
Red Trace: SR1

Things to Try

1. Change the soft-stop timing in the soft-start window.
2. Adjust/change the blanking of faults during soft stop.
3. Perform a soft start from light load mode with a fast SR phase in speed.

FAULT RESPONSE WINDOW

The **Fault Response** window programs the fault response for all the voltage, current, temperature, and GPIO faults, 22 in total. Each fault has a configuration with a programmable debounce time, and the response to the fault followed by the delay time between consecutive soft starts if the PSU is shutdown as a result of the fault action.

Figure 37. Current Fault Response Monitoring

The first fault ID (FFID) that caused the PSU to shutdown is displayed in a monitoring window.

A complete description of the fault response can be found in the data sheet.

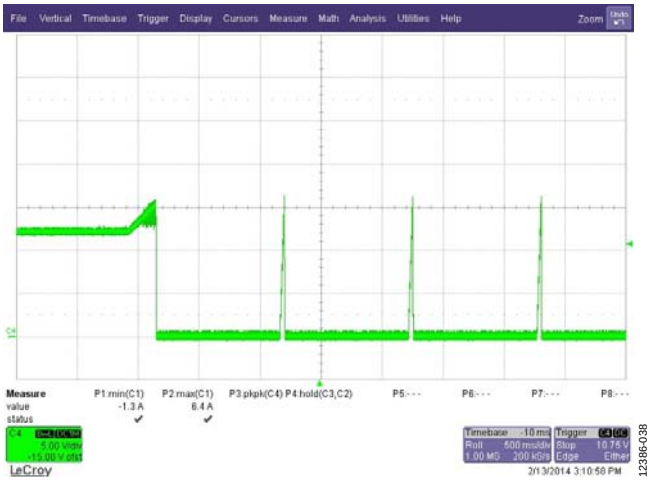

Figure 38. VOUT_OV_FAST_FAULT
Fault Response Set to Shut Down and Retry Indefinitely
Green Trace: Output Voltage

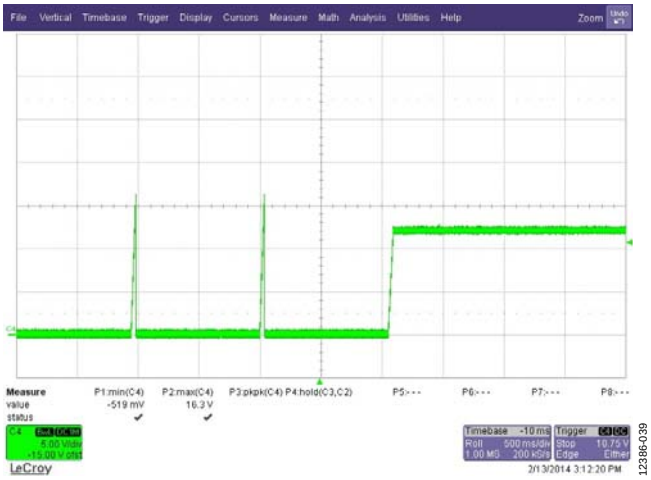

Figure 39. Recovery from VOUT_OV_FAST_FAULT
Green Trace: Output Voltage

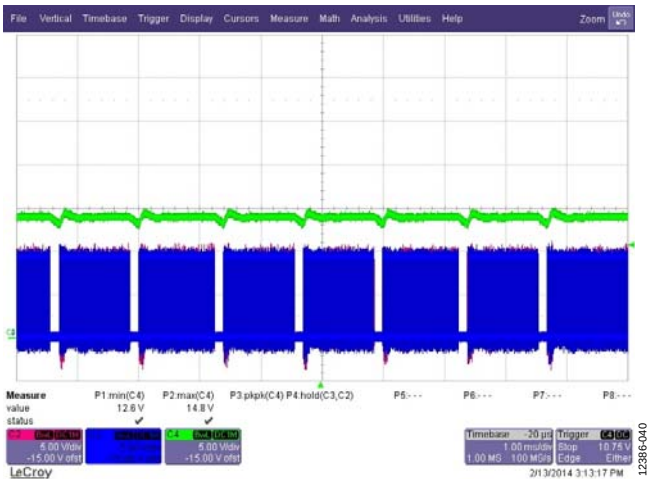

Figure 40. VOUT_OV_FAULT
Fault Response Set to Disable PWMs and Retry when Fault is Cleared
Green Trace: Output Voltage
Red and Blue Trace: PWMs

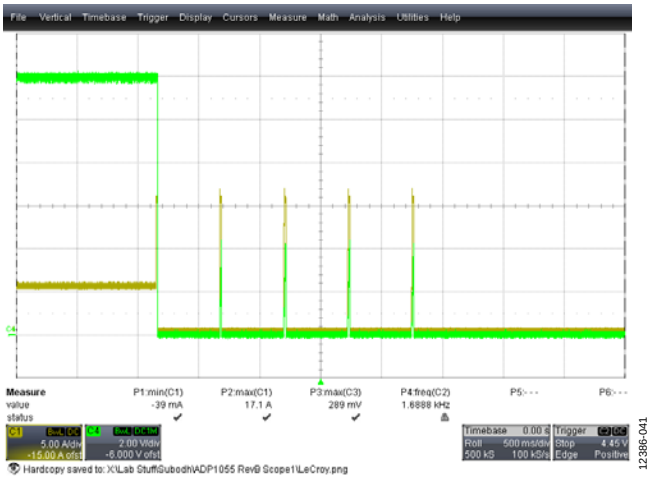

Figure 41. IOUT_OC_FAULT under Short-Circuit
Fault Response Set to Shut Down and Retry 4 Times
Green Trace: Output Voltage
Yellow Trace: Load Current

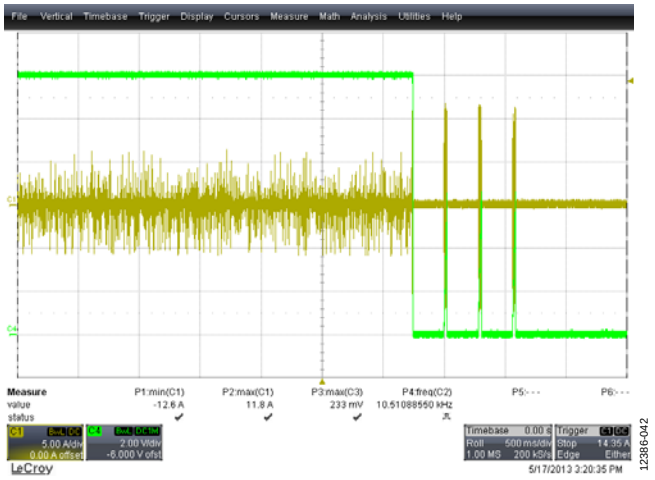

Figure 42. IIN_OC_FAULT under Short-Circuit Fault Response Set to Shut down and Retry 3 Times Green Trace: Output Voltage Yellow Trace: Primary Current

Things to Try

1. Trigger other faults, such as VIN_UV_FAULT, GPIOx_FAULT, IN_OC_FAST, POUT_OP, and TON_MAX.
2. Enable the end of cycle shutdown feature (**PWM** window).

VIN WINDOW

The **VIN** window sets the thresholds for VIN_OV, VIN_UV, VIN_ON, and VIN_OFF. The corresponding faults can be set up in the **Fault Response** window. In the **Additional Settings** bar, the voltage feedforward function can be enabled. Since the ADP1055 is a secondary side controller, the input voltage is not available to the IC before switching begins. Thus, VIN_ON is set to 0 V.

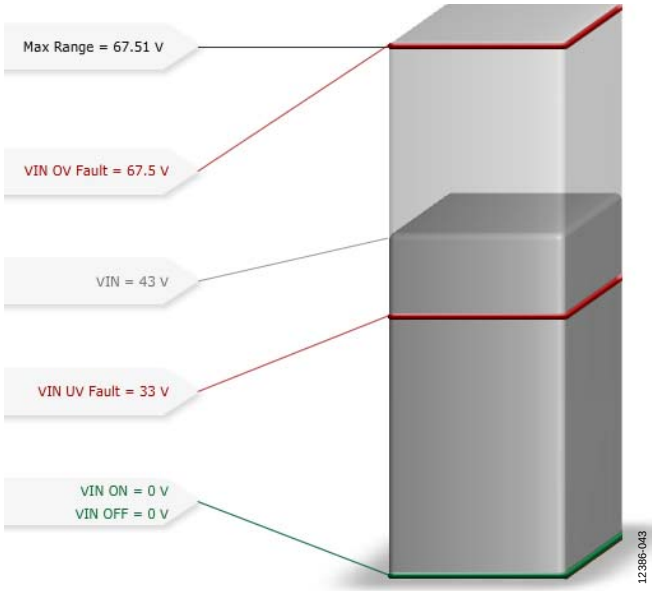

Figure 43. VIN Window

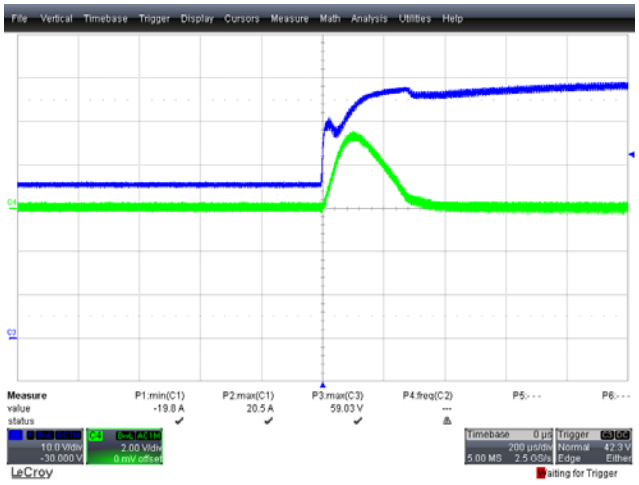

Figure 44. Line Voltage Feedforward DISABLED, 5 A Load Green Trace: AC Coupled Output Voltage Blue Trace: Input Voltage

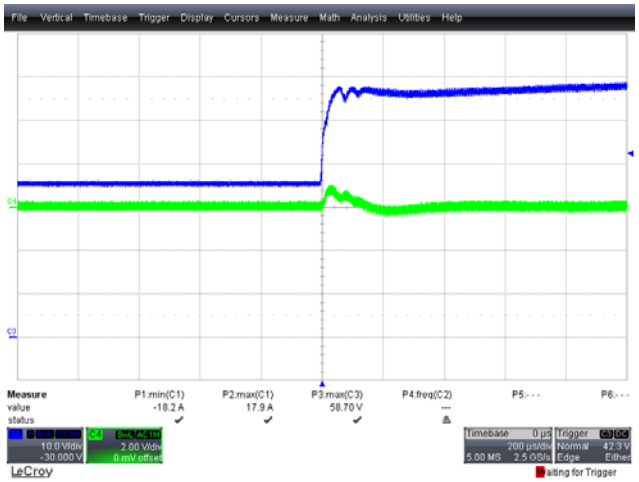

Figure 45. Line Voltage Feedforward Enabled, 5 A Load Green Trace: AC Coupled Output Voltage Blue Trace: Input Voltage

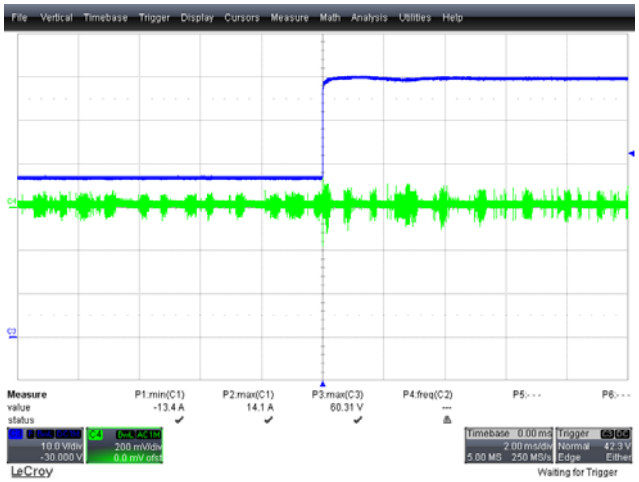

Figure 46. Line Voltage Feedforward Enabled, 0 A Load, Light Load Mode; Green Trace: AC-Coupled Output Voltage; Blue Trace: Input Voltage

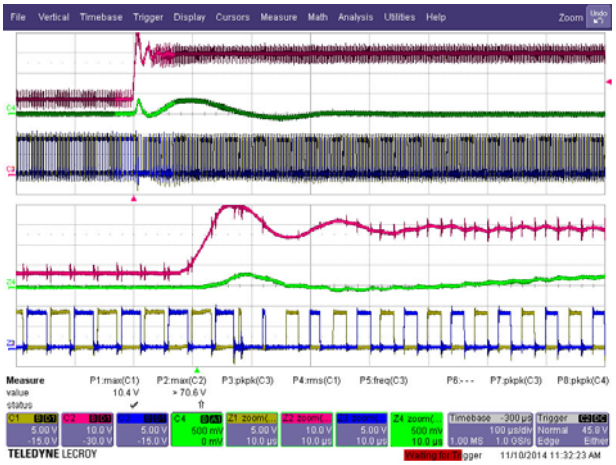

Figure 47. Voltage Line Feedforward;
Red Trace: Input Voltage 10 V/Div;
Green Trace: AC-Coupled Output Voltage;
Blue and Yellow Traces: OUTB and OUTC PWMs

IIN WINDOW

The **IIN** window sets up thresholds for the input current thresholds, namely the IIN_FAST_OC_FAULT_LIMIT and the IN_OC_FAULT_LIMIT. The corresponding faults can be set up in the **Fault Response** window.

There are two ranges for the fast limit (1.2 V or 250 mV). Using the board settings, in particular the current transformer (CT) turns ratio, and termination resistor, the GUI calculates the peak current at which the IIN_FAST_OC_FAULT_LIMIT is triggered. This fault terminates the PWM pulse for the remainder of the switching period depending upon the timeout value (this is set in the **Additional Settings** bar).

For example, a timeout of four switching cycles causes the IN_FAST_OC_FAULT flag to set when the IIN_FAST_OC_FAULT_LIMIT threshold is crossed 4 times consecutively.

This function can be bypassed using GPIO1 as shown in Figure 48.

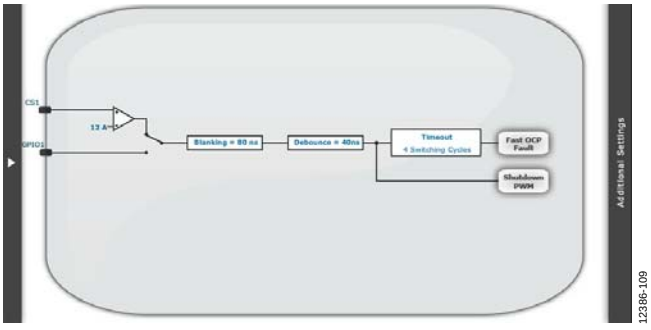

Figure 48. Additional Settings of the IIN Window

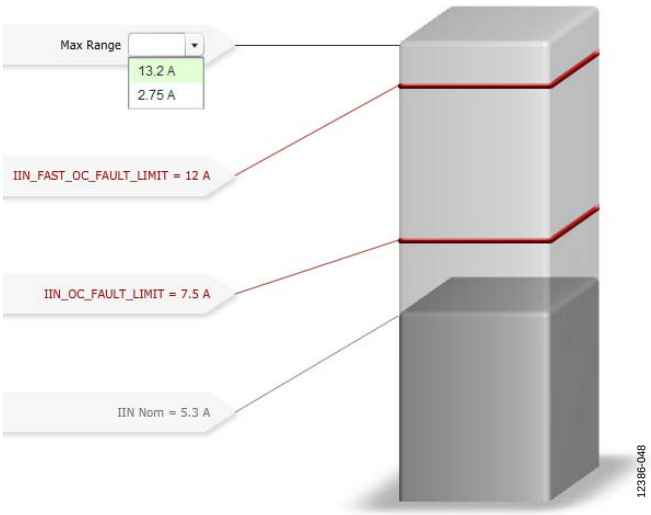

Figure 49. IIN Window

The IN_OC_FAULT is an accurate fault whose threshold can be set simply by dragging and dropping the threshold bar or by entering a value using the keyboard icon on the top right hand corner of the screen. Changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

VOUT WINDOW

The VOUT window programs thresholds for the output voltage set point, over voltage protection (OVP) and warning, and under voltage protection (UVP) and warning.

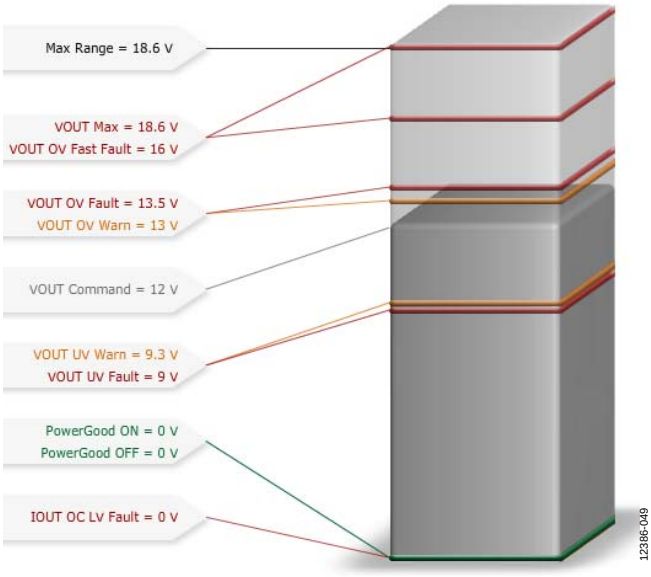

Figure 50. VOUT Window

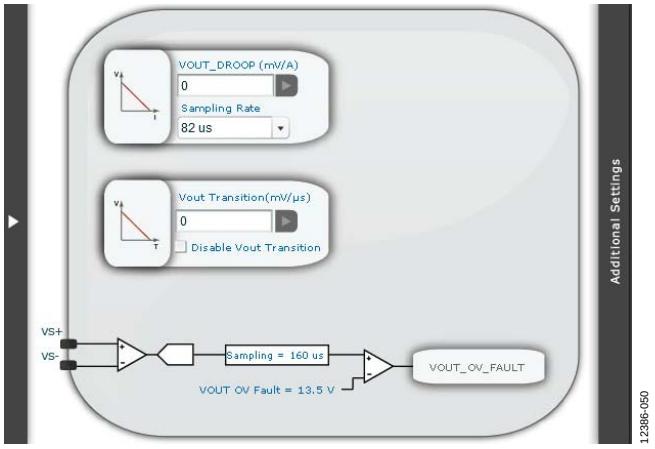

Figure 51. Additional Settings of VOUT Window

The settings can be changed in a simple drag-and-drop fashion and or by selecting the value from the combo box. Changes to the VOUT_DROOP and VOUT_TRANSITION value take place after the button on the right side next to the text box is clicked. Other changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

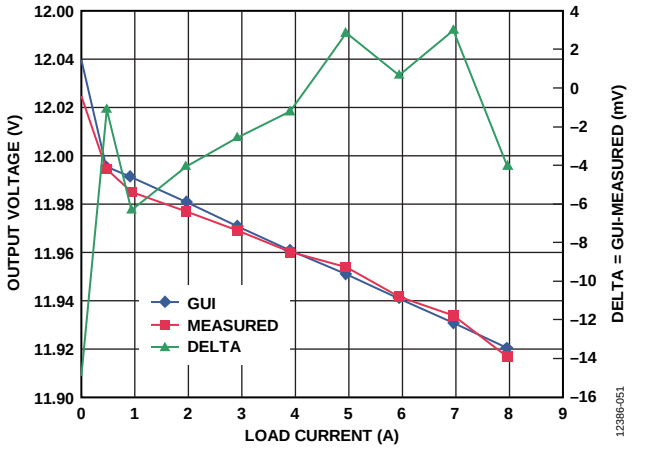

Figure 52. VOUT_DROOP = 10 mV/A

Figure 53. Output Voltage Ripple, 20 A Load
Green Trace: AC Coupled Output Voltage

IOUT WINDOW

The **IOUT** window sets thresholds for the output current. Thresholds for output over current, under current, and constant current can be programmed via this window.

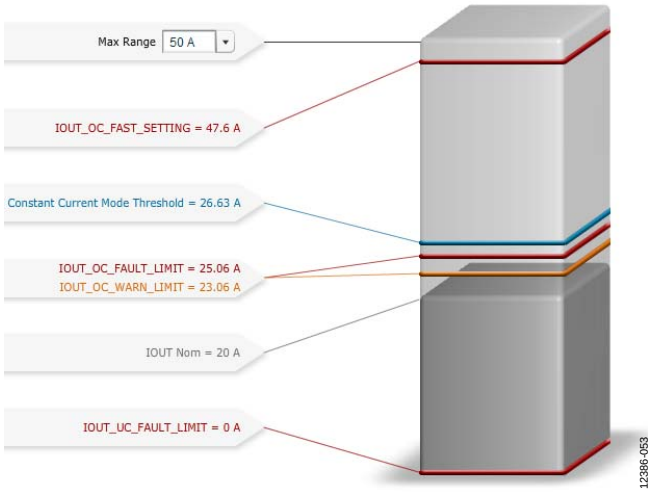

Figure 54. IOUT Window

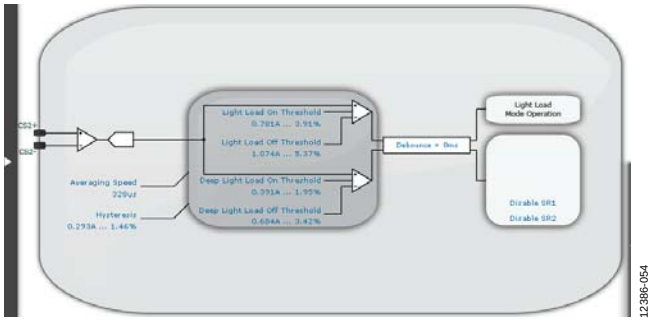

Figure 55. Light Load Settings in IOUT Window

Additionally, settings for the light load mode can also be programmed in this window through the **Light Load Settings** bar on the right side. The thresholds can be programmed from the drop-down list. The deep light load mode can be enabled, if necessary.

It is recommended to use the manufacturer specific mode with the maximum slew rate to control (decrease) the output voltage when the load current crosses the constant current threshold. The constant current threshold is set to a percentage (for example, ±3.125% or ±12.5%) of the IOUT_OC_FAULT_LIMIT.

Figure 56. IOUT_OC_FAULT
PSU is Set to Enter Constant Current Mode at 27 A. Fault Response Set to Wait for a Debounce of 5 Seconds, Shutdown, and Retry Indefinitely.
Green Trace: Output Voltage
Yellow Trace: Load Current

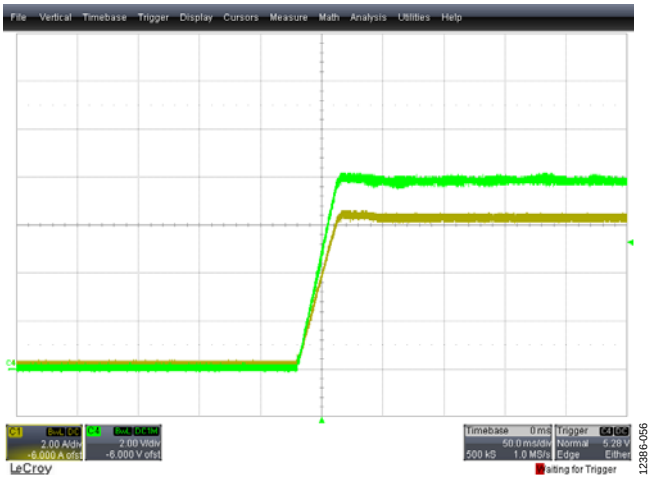

Figure 57. Constant Current Mode in a Load Resistor
Green Trace: Output Voltage
Yellow Trace: Load Current

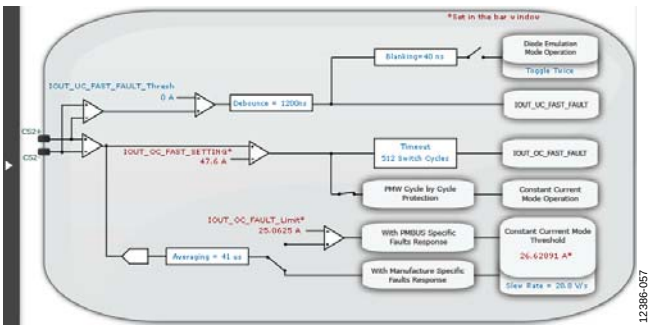

Figure 58. Additional Settings in IOUT Window

In the **Additional Settings** bar, the cycle by cycle protection (over current and reverse current) can be set. Also, the constant current averaging rate and the slew rate can be selected.

POUT WINDOW

The threshold limit for over load power can be set in this window. The settings can be changed in a simple drag-and-drop fashion. Changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

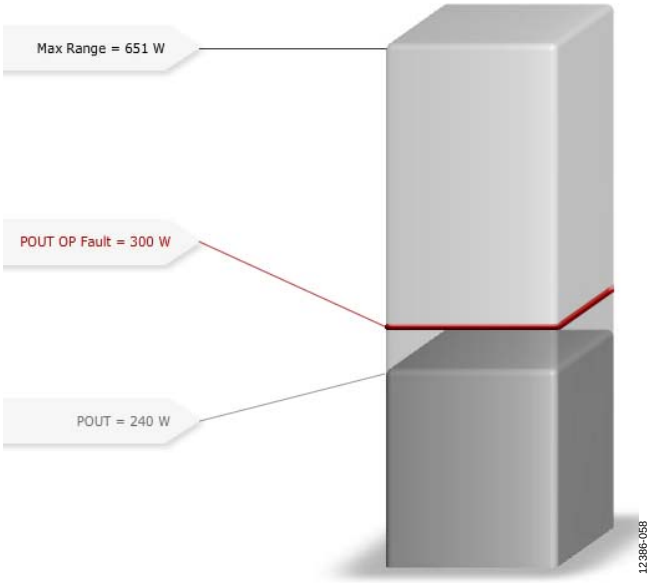

Figure 59. POUT Window

TEMPERATURE WINDOW

In the **Temperature** window, the threshold for overtemperature protection (OTP) and the low temperature threshold can be set. The settings can be changed in a simple drag-and-drop fashion. Changes take place immediately and are stored in the RAM of the IC, but need to be saved to EEPROM for permanent storage.

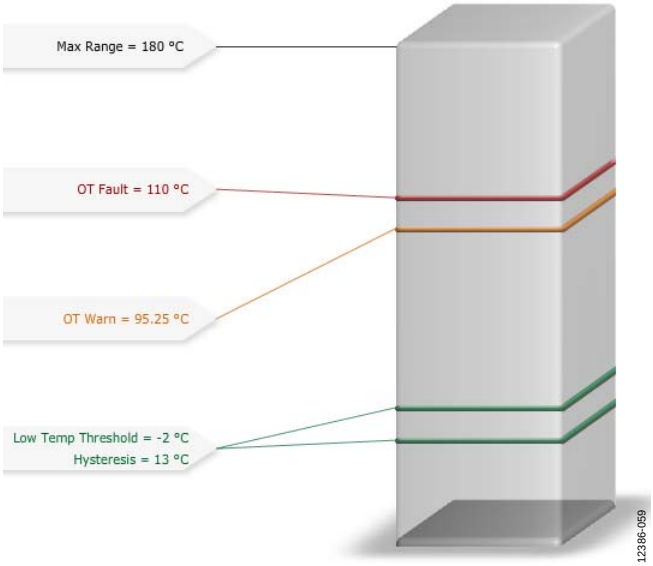

Figure 60. Temperature Window

PGOOD AND GPIO WINDOWS

The **PGOOD** and **GPIO** windows go hand in hand. Several flags, such as IOUT_OC_FAULT and VOUT_OV, can be set into PGOOD1 and PGOOD2 which are internal signals. These can be routed to hardware pins GPIO1 to GPIO4 in the **GPIO** window.

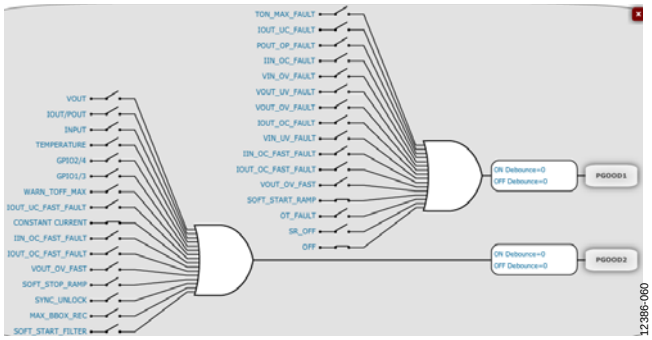

Figure 61. Additional Settings in IOUT Window

The **GPIO** window configures the GPIO1 to GPIO4 pins either as an input or as an output. If selected as an output, the pin can output a logic combination of PGOOD1 and PGOOD2. If selected as an input, then it acts as a digital input whereupon a GPIOx fault can be triggered.

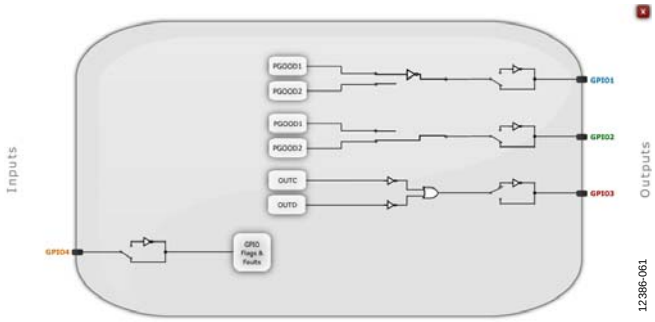

Figure 62. GPIO Window

There are several logic operations available for programming the output as shown in Figure 63.

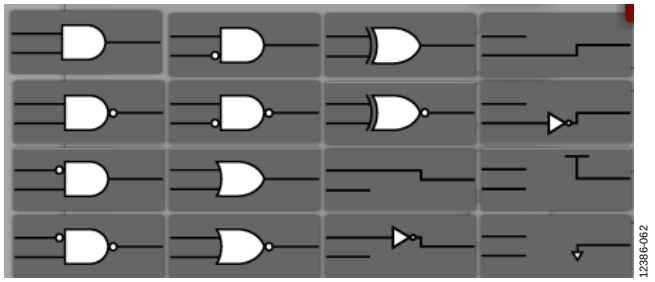

Figure 63. Logic Options for GPIO

32-BIT KEYCODE

The ADP1055 has a 32-bit password protection and extended command masking set.

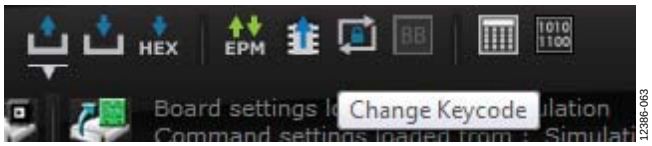

Figure 64. Change Keycode Icon (Sixth from the Left)

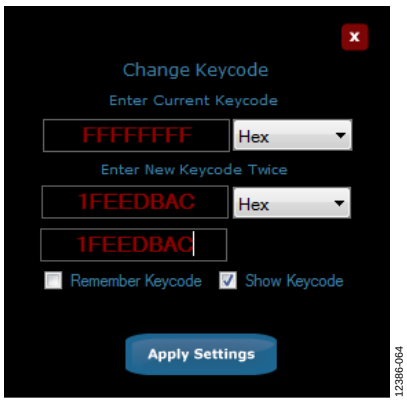

Figure 65. Example of Changing the Keycode Using a Pneumonic for Negative Feedback in Signed Binary Numbers

COMMAND MASKING

The ADP1055 supports command masking that can mask any command (PMBUS command and extended manufacturer specific command). When a read or write is made to a command that is masked, the ADP1055 returns with a NACK.

Commands can be masked in the command masking window by simply clicking on the lock next to the command.

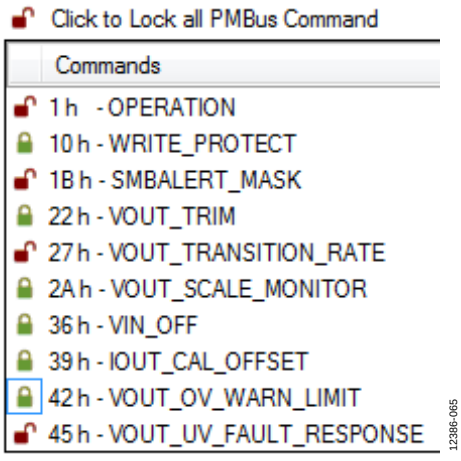

Figure 66. Sample Command Masking Window

The commands that are locked/masked are then blocked out from the GUI and the corresponding settings window is not accessible.

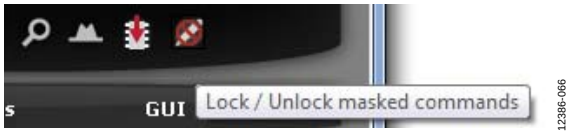

Figure 67. Lock Masked Commands Icon (Rightmost Icon)

ACTIVE CLAMP SNUBBER

GPIO3 and GPIO4 can be configured to have the special function of an active clamp snubber. In this feature, GPIO3 and GPIO4 act as PWM signals that are triggered off a reference PWM which is either

- Falling edge of SR1 and SR2 or
- Falling edge of $\overline{\text{OUTC}}$ and $\overline{\text{OUTD}}$ (that is, rising edge of OUTC and OUTD)

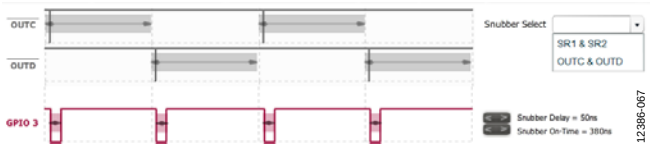

Figure 68. Active Clamp Options Selected in PWM Window, Snubber Tab

The active snubber function has additional options of a programmable on time and a delay from the reference PWM. A complete description of the active snubber function is available in the data sheet.

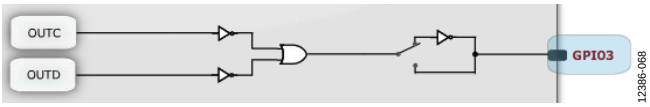

Figure 69. Active Clamp Option in Evaluation Board

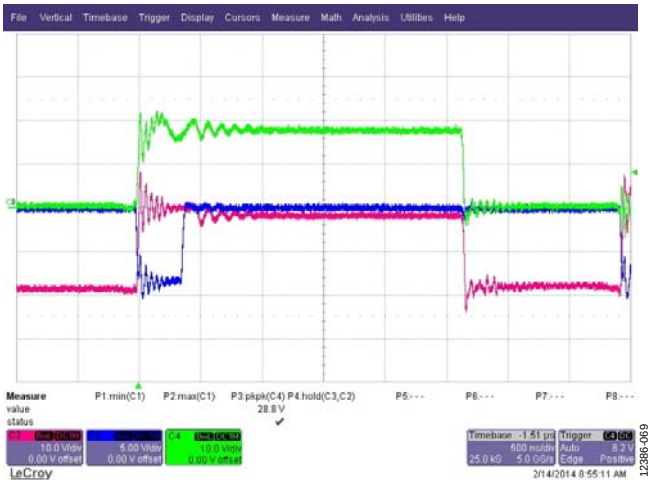

Figure 70. Active Clamp Snubber Enabled, 20 A Load
Green Trace: Drain—Source Voltage of Low Side SR FET
Blue Trace: Gate—Source Voltage of Snubber FET
Red Trace: Drain—Source Voltage of Snubber FET

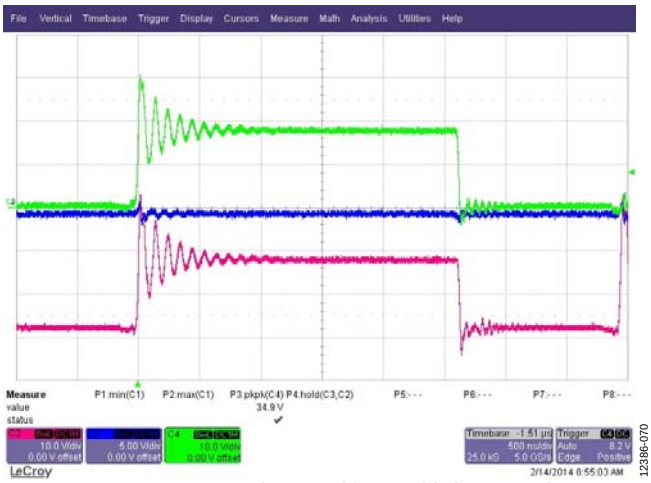

Figure 71. Active Clamp Snubber Disabled, 20 A Load
Green Trace: Drain—Source Voltage of Low Side SR FET
Blue Trace: Gate—Source Voltage of Snubber FET
Red Trace: Drain—Source Voltage of Snubber FET

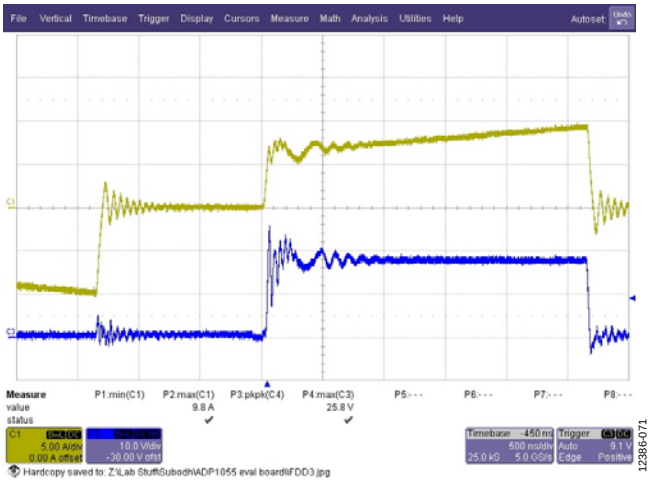

Figure 72. Active Clamp Snubber Enabled, Zoomed In, 20 A Load
Yellow Trace: Primary Current
Blue Trace: Drain Source Voltage of Low Side SR FET

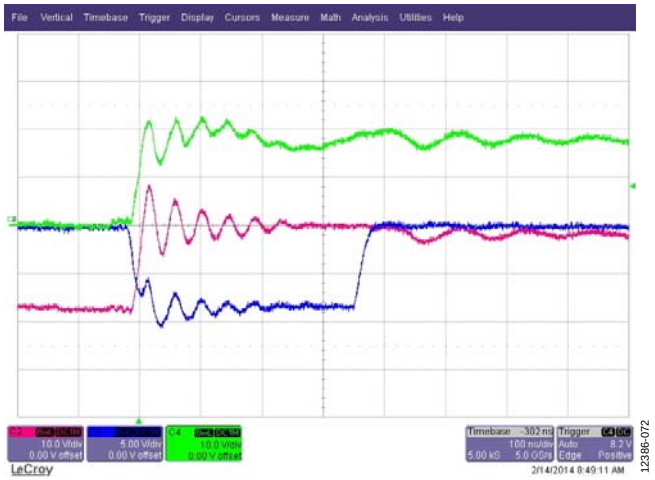

Figure 73. Active Clamp Snubber Enabled, Zoomed In, 20 A Load
50 ns Delay, 380 ns Snubber on Time
Green Trace: Drain—Source Voltage of Low Side SR FET
Blue Trace: Gate—Source Voltage of Snubber FET
Red Trace: Drain—Source Voltage of Snubber FET

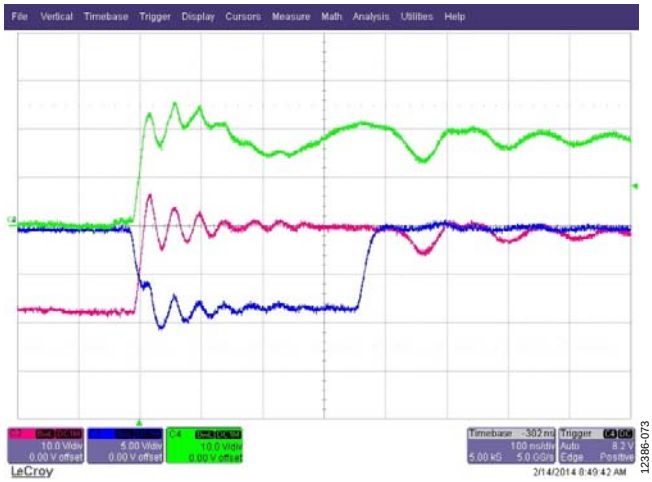

Figure 74. Active Clamp Snubber Enabled, Zoomed In, 15 A Load
50 ns Delay, 380 ns Snubber on Time
Green Trace: Drain—Source Voltage of Low Side SR FET
Blue Trace: Gate—Source Voltage of Snubber FET
Red Trace: Drain—Source Voltage of Snubber FET

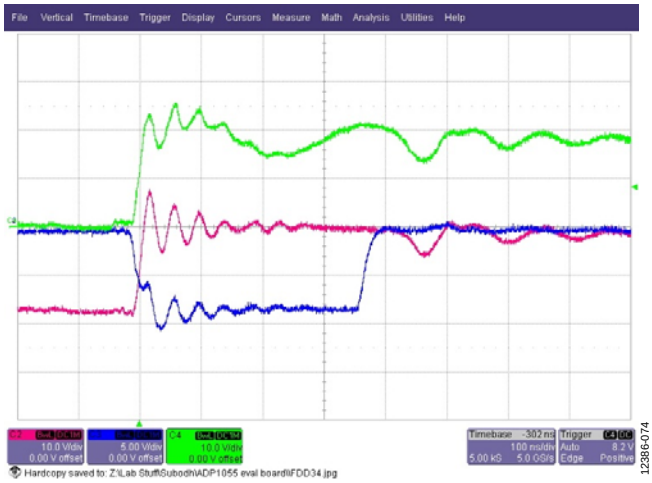

Figure 75. Active Clamp Snubber Enabled, Zoomed In, 10 A Load
50 ns Delay, 380 ns Snubber on Time
Green Trace: Drain—Source Voltage of Low Side SR FET
Blue Trace: Gate—Source Voltage of Snubber FET
Red Trace: Drain—Source Voltage of Snubber FET

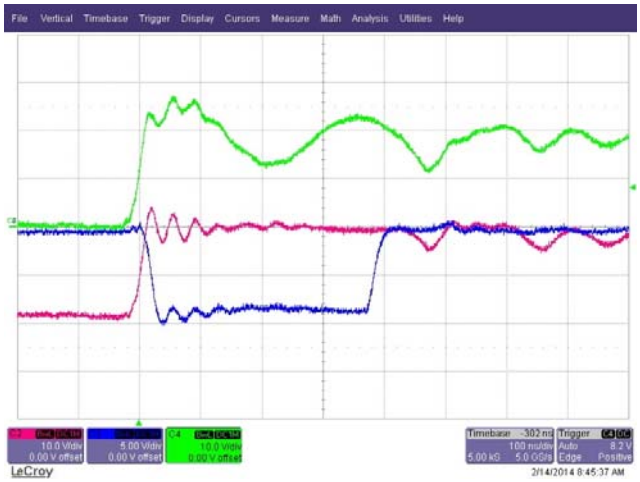

Figure 76. Active Clamp Snubber Enabled, Zoomed In, 5 A Load
50 ns Delay, 380 ns Snubber on Time
Green Trace: Drain—Source Voltage of Low Side SR FET
Blue Trace: Gate—Source Voltage of Snubber FET
Red Trace: Drain—Source Voltage of Snubber FET

DIGITAL CONTROL LOOP

Control Loop Configuration

The control loop configuration procedures can be shown as a series of three steps.

1. The board parameters are set, including topology, turn ratio of main transformer, output LC filter and output voltage feedback network. Using this inform-ation, the ADP1055 generates the Bode plots of LC filter and feedback network.
2. The switching frequency is determined in the PWM settings window. Changing of the switching frequency changes the low frequency gain and the third pole position.
3. You can start to place the zeros and poles, and set the low frequency gain and high frequency gain of the Type-III compensator, based on the stability rules.

Using the loop analyzer, you can validate the programmed control loop as shown in Figure 78. For an easy test on the control loop, the signal from loop analyzer can be injected in J11and TP26 in the schematic.

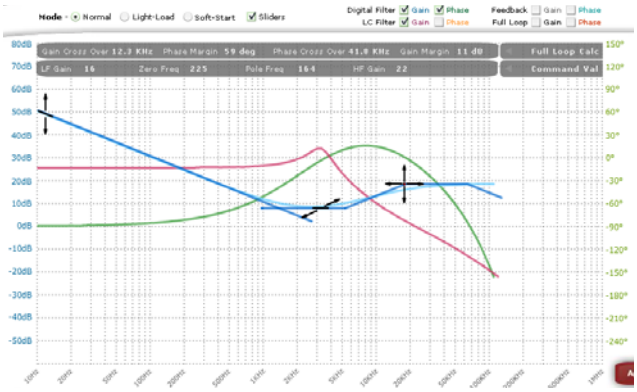

Figure 77. Digital Filter Settings Window

The double update rate feature of the ADP1055 greatly increases the ability to push the bandwidth to higher limits while still retaining a good phase margin.

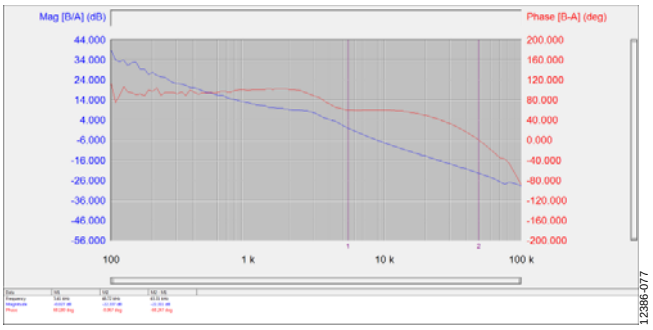

Figure 78. Control Loop Test by AP300 Loop Analyzer
(Double Update Rate Enabled)
Crossover Frequency is 5.41kHz
Phase Margin is 60°
Gain Margin is 22 dB

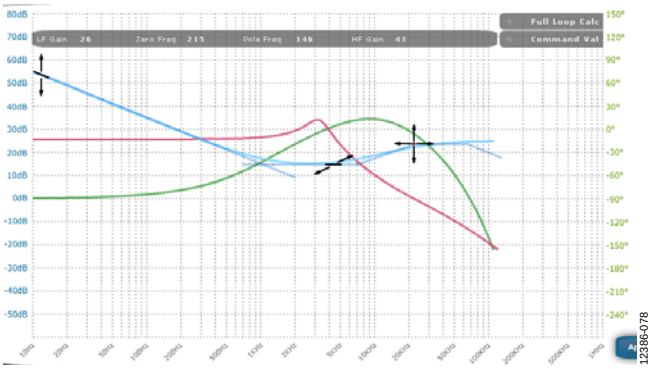

Figure 79. Digital Filter Settings Window
Optimized Filter to Provide Better Crossover Frequency

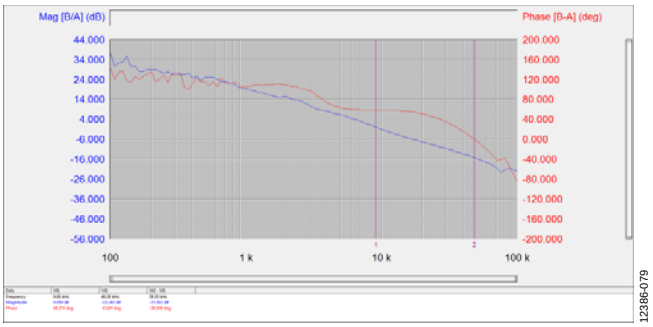

Figure 80. Control Loop Test by AP300 Loop Analyzer
(Double Update Rate Enabled)
Crossover Frequency is 9.08 kHz
Phase Margin is 58°
Gain Margin is 22 dB

Transient Response for the Load Step

A dynamic electronic load can be connected to the output of the evaluation board to evaluate the transient response. Set up an oscilloscope to capture the transient waveform of the power supply output. Figure 81 and Figure 82 show an example of the load transient response.

You can vary the digital filter via the GUI to change the transient response. This evaluation shows you how the digital filter can easily be programmed to optimize the transient response of the PSU.

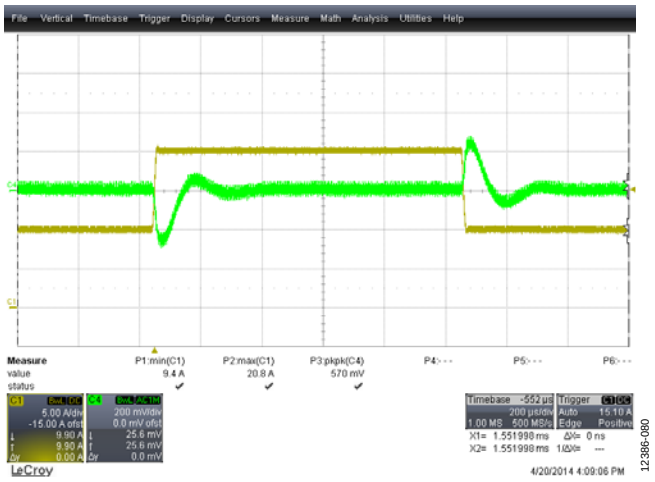

Figure 81. Transient Response with Load Steps: 50% to 100% to 50%
Green Trace: AC Coupled Output Voltage
Yellow Trace: Load Current, 1 A/µs

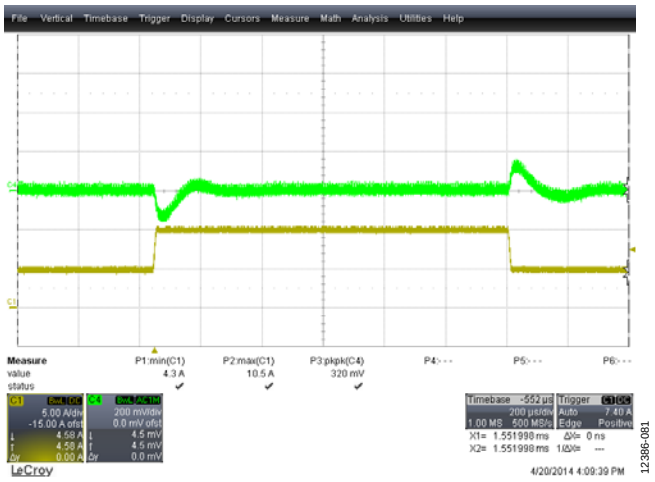

Figure 82. Transient Response with Load Steps: 25% to 50% to 25%
Green Trace: AC Coupled Output Voltage
Yellow Trace: Load Current, 1 A/µs

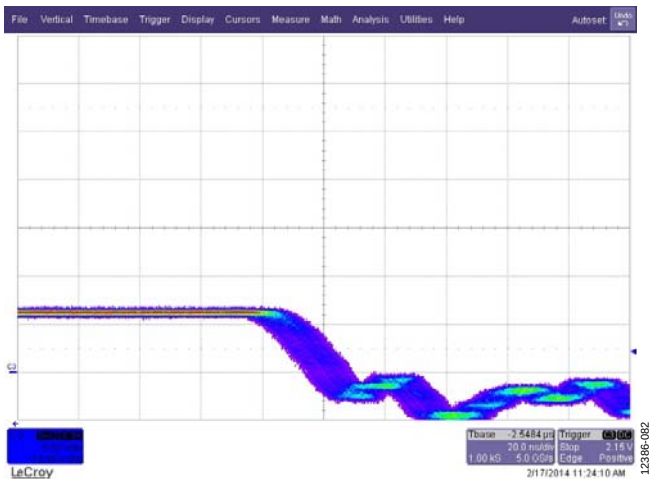

Figure 83. PWM Jitter at 20 A Load with 20 sec Persistence on Oscilloscope

SR Reverse Current Protection

This test can be conducted in the following two ways:

- Enable the diode emulation mode.
- Use the IOUT_UC_FAST comparator.

The test shown in Figure 84 shows the effectiveness of the reverse current protection.

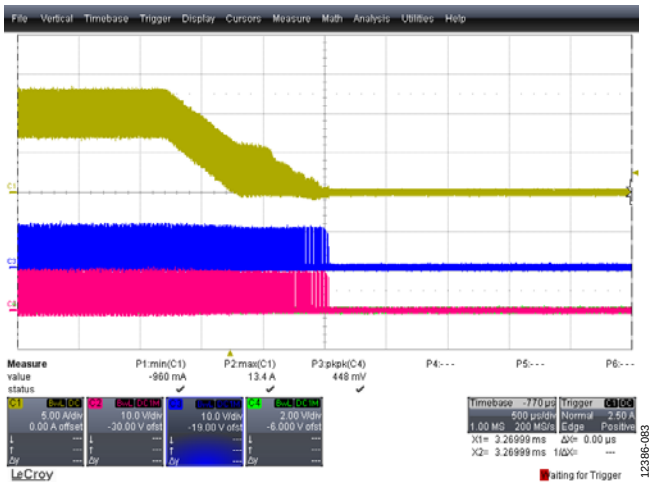

Figure 84. Diode Emulation Mode Active;
Reverse Current Comparator Threshold Adjusted for Best Performance;
Yellow Trace: Output Inductor Current;
Red and Blue Traces: SR1 and SR2

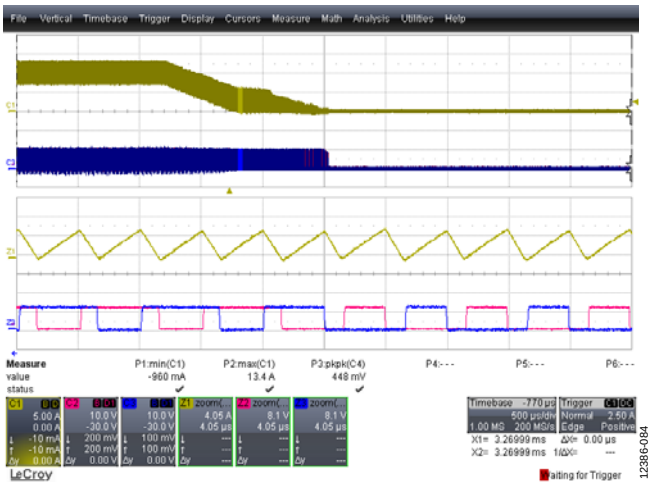

Figure 85. Diode Emulation Mode Active; Threshold Adjusted for Best Performance; Waveform Shows that SR1 and SR2 Move from CCM to Diode Emulation Mode Instantly;
Yellow Trace: Output Inductor Current;
Red and Blue Traces: SR1 and SR2

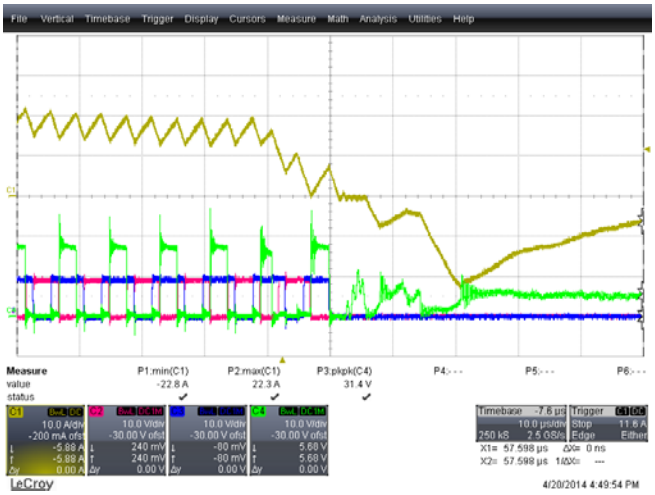

Figure 86. IOUT_UC_FAST_FAULT; Output Inductor Shorted to Ground; The Reverse Current Comparator Threshold Adjusted for Best Performance;
Yellow Trace: Output Inductor Current;
Red and Blue Traces: SR1 and SR2;
Green Trace: Synchronous Rectifier Drain Voltage

Light Load Efficiency Optimization

The ADP1055 can be programmed to optimize performance when the output current drops below a certain level. The light load and deep light load mode thresholds are set in a manner to reduce losses and increase efficiency. A hysteresis for light load mode and deep light load mode is provided on the thresholds to avoid oscillations. The thresholds for light load mode and deep light load mode can also be programmed in the IOUT setting window as shown in Figure 87.

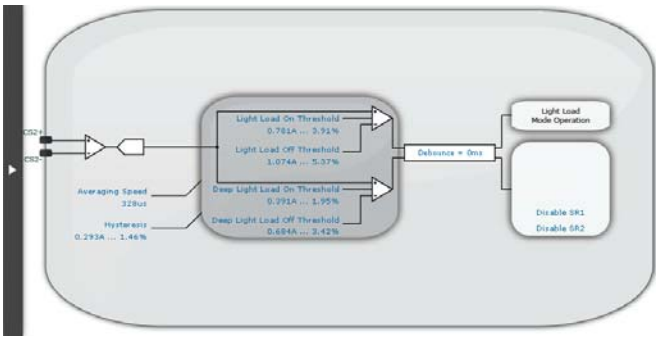

Figure 87. Light Load Mode and Deep Light Load Mode Thresholds

When operating in light load mode or deep light load mode, the light load mode flag is set as shown in the **Monitor** tab. In both situations, the light load filter settings are used. In combination with the pulse skipping function, the standby power consumption can be reduced.

EFFICIENCY CURVES

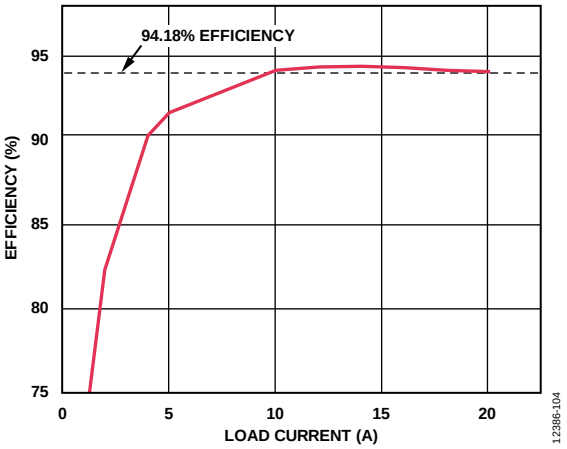

Figure 88. Efficiency Curve at 36 V DC, 48 V DC, 60 V DC, and 75 V DC Input

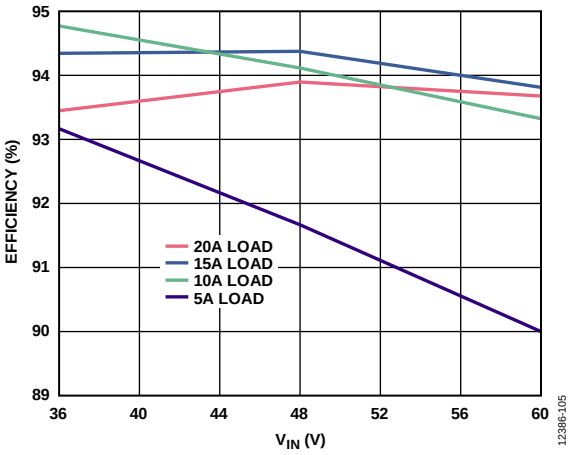

Figure 89. Efficiency vs. Input Voltage

THERMAL PERFORMANCE

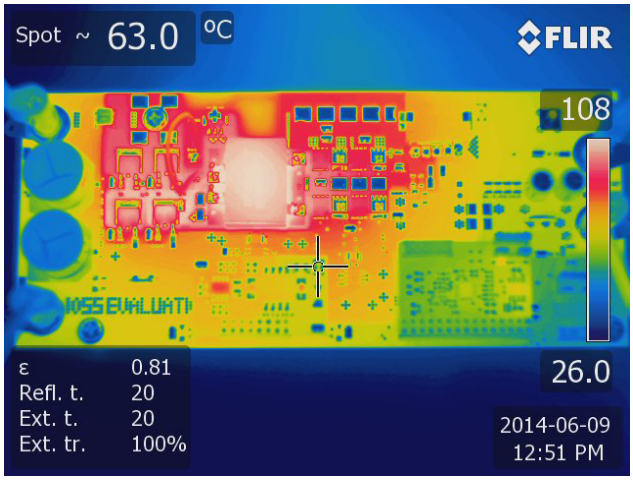

Figure 90. Thermal Image at 48 V DC Input, 20 A Load, No Airflow, 1 Hour Soaking Time

GUI 55S SETTINGS FILE

Copy the contents below into a text file and rename it with using an extension of .55s. Load this file in the GUI using **the Load settings from file** option. Ensure that the last line of the .55s file does not have a carriage return.

```
Reg(1 h) = 80h - OPERATION
Reg(2 h) = 1Fh - ON_OFF_CONFIG
Reg(10 h) = 00h - WRITE_PROTECT
Reg(1B h) = 00780079007A007B007D007E007C0080h - SMBALERT_MASK
Reg(20 h) = 15h - VOUT_MODE
Reg(21 h) = 6000h - VOUT_COMMAND
Reg(22 h) = 0068h - VOUT_TRIM
Reg(23 h) = 0000h - VOUT_CAL_OFFSET
Reg(24 h) = 999Ah - VOUT_MAX
Reg(27 h) = 8000h - VOUT_TRANSITION_RATE
Reg(28 h) = 8000h - VOUT_DROOP
Reg(29 h) = 9AA7h - VOUT_SCALE_LOOP
Reg(2A h) = 9AA6h - VOUT_SCALE_MONITOR
Reg(33 h) = EBE8h - FREQUENCY_SWITCH
Reg(35 h) = E800h - VIN_ON
Reg(36 h) = E800h - VIN_OFF
Reg(37 h) = 0000h - INTERLEAVE
Reg(38 h) = B266h - IOUT_CAL_GAIN
Reg(39 h) = 8000h - IOUT_CAL_OFFSET
Reg(40 h) = 6C00h - VOUT_OV_FAULT_LIMIT
Reg(41 h) = FCh - VOUT_OV_FAULT_RESPONSE
Reg(42 h) = 6800h - VOUT_OV_WARN_LIMIT
Reg(43 h) = 4A65h - VOUT_UV_WARN_LIMIT
Reg(44 h) = 4800h - VOUT_UV_FAULT_LIMIT
Reg(45 h) = 3Ah - VOUT_UV_FAULT_RESPONSE
Reg(46 h) = E991h - IOUT_OC_FAULT_LIMIT
Reg(47 h) = FCh - IOUT_OC_FAULT_RESPONSE
Reg(48 h) = 0000h - IOUT_OC_LV_FAULT_LIMIT
Reg(49 h) = 00h - IOUT_OC_LV_FAULT_RESPONSE
Reg(4A h) = E971h - IOUT_OC_WARN_LIMIT
Reg(4B h) = E800h - IOUT_UC_FAULT_LIMIT
Reg(4C h) = B8h - IOUT_UC_FAULT_RESPONSE
Reg(4F h) = F1B8h - OT_FAULT_LIMIT
Reg(50 h) = FFh - OT_FAULT_RESPONSE
Reg(51 h) = F17Dh - OT_WARN_LIMIT
Reg(55 h) = EA1Ch - VIN_OV_FAULT_LIMIT
Reg(56 h) = 3Ch - VIN_OV_FAULT_RESPONSE
Reg(59 h) = E908h - VIN_UV_FAULT_LIMIT
Reg(5A h) = 3Ah - VIN_UV_FAULT_RESPONSE
Reg(5B h) = D1E0h - IIN_OC_FAULT_LIMIT
Reg(5C h) = FCh - IIN_OC_FAULT_RESPONSE
Reg(5E h) = 0000h - POWER_GOOD_ON
Reg(5F h) = 0000h - POWER_GOOD_OFF
```

```
Reg(60 h) = 0000h - TON_DELAY
Reg(61 h) = 0028h - TON_RISE
Reg(62 h) = 0032h - TON_MAX_FAULT_LIMIT
Reg(63 h) = 38h - TON_MAX_FAULT_RESPONSE
Reg(64 h) = 0000h - TOFF_DELAY
Reg(65 h) = 000Ah - TOFF_FALL
Reg(66 h) = 0032h - TOFF_MAX_WARN_LIMIT
Reg(68 h) = 012Ch - POUT_OP_FAULT_LIMIT
Reg(69 h) = 81h - POUT_OP_FAULT_RESPONSE
Reg(D0 h) = 4Bh - SLV_ADDR_SELECT
Reg(F4 h) = 003E000000FF0000FFFF60007F70FB01FF00037FDE639FFF03E8079F0A65000E20h - CMD_MASK
Reg(F5 h) = FFFFFFFFFF000000FFFFFFFFFFFFFFFFFFFFFFFF15h - EXTCMD_MASK
Reg(FE01 h) = 10h - NM_DIGFILT_LF_GAIN_SETTING
Reg(FE02 h) = E1h - NM_DIGFILT_ZERO_SETTING
Reg(FE03 h) = A4h - NM_DIGFILT_POLE_SETTING
Reg(FE04 h) = 16h - NM_DIGFILT_HF_GAIN_SETTING
Reg(FE05 h) = 31h - LLM_DIGFILT_LF_GAIN_SETTING
Reg(FE06 h) = F2h - LLM_DIGFILT_ZERO_SETTING
Reg(FE07 h) = E3h - LLM_DIGFILT_POLE_SETTING
Reg(FE08 h) = 3Ah - LLM_DIGFILT_HF_GAIN_SETTING
Reg(FE09 h) = 0Ch - SS_DIGFILT_LF_GAIN_SETTING
Reg(FE0A h) = AEh - SS_DIGFILT_ZERO_SETTING
Reg(FE0B h) = 00h - SS_DIGFILT_POLE_SETTING
Reg(FE0C h) = 1Eh - SS_DIGFILT_HF_GAIN_SETTING
Reg(FE0D h) = 33A1h - OUTA_REDGE_SETTING
Reg(FE0E h) = 33B8h - OUTA_FEDGE_SETTING
Reg(FE0F h) = 0210h - OUTB_REDGE_SETTING
Reg(FE10 h) = 0228h - OUTB_FEDGE_SETTING
Reg(FE11 h) = 0210h - OUTC_REDGE_SETTING
Reg(FE12 h) = 0228h - OUTC_FEDGE_SETTING
Reg(FE13 h) = 33A1h - OUTD_REDGE_SETTING
Reg(FE14 h) = 33B8h - OUTD_FEDGE_SETTING
Reg(FE15 h) = 0348h - SR1_REDGE_SETTING
Reg(FE16 h) = 00A0h - SR1_FEDGE_SETTING
Reg(FE17 h) = 34D8h - SR2_REDGE_SETTING
Reg(FE18 h) = 3230h - SR2_FEDGE_SETTING
Reg(FE19 h) = 33A0h - SR1_REDGE_LLM_SETTING
Reg(FE1A h) = 33B8h - SR1_FEDGE_LLM_SETTING
Reg(FE1B h) = 0210h - SR2_REDGE_LLM_SETTING
Reg(FE1C h) = 0228h - SR2_FEDGE_LLM_SETTING
Reg(FE1D h) = 00h - ADT_CONFIG
Reg(FE1E h) = 00h - ADT_THRESHOLD
Reg(FE1F h) = 88h - OUTA_DEAD_TIME
Reg(FE20 h) = 88h - OUTB_DEAD_TIME
Reg(FE21 h) = 88h - OUTC_DEAD_TIME
Reg(FE22 h) = 88h - OUTD_DEAD_TIME
Reg(FE23 h) = 88h - SR1_DEAD_TIME
```

```
Reg(FE24 h) = 88h - SR2_DEAD_TIME
Reg(FE25 h) = C0h - VSBAL_SETTING
Reg(FE26 h) = 23h - VSBAL_OUTA_B
Reg(FE27 h) = 32h - VSBAL_OUTC_D
Reg(FE28 h) = C8h - VSBAL_SR1_2
Reg(FE29 h) = 04h - FFWD_SETTING
Reg(FE2A h) = 12h - ISHARE_SETTING
Reg(FE2B h) = 00h - ISHARE_BANDWIDTH
Reg(FE2C h) = 01h - IIN_OC_FAST_SETTING
Reg(FE2D h) = FFh - IOUT_OC_FAST_SETTING
Reg(FE2E h) = 02h - IOUT_UC_FAST_SETTING
Reg(FE2F h) = A9h - VOUT_OV_FAST_SETTING
Reg(FE30 h) = 69B5h - DEBOUNCE_SETTING_1
Reg(FE31 h) = 020Fh - DEBOUNCE_SETTING_2
Reg(FE32 h) = 0A05h - DEBOUNCE_SETTING_3
Reg(FE33 h) = 0000h - DEBOUNCE_SETTING_4
Reg(FE34 h) = 84h - VOUT_OV_FAST_FAULT_RESPONSE
Reg(FE35 h) = 80h - IOUT_OC_FAST_FAULT_RESPONSE
Reg(FE36 h) = B8h - IOUT_UC_FAST_FAULT_RESPONSE
Reg(FE37 h) = FCh - IIN_OC_FAST_FAULT_RESPONSE
Reg(FE38 h) = B8h - ISHARE_FAULT_RESPONSE
Reg(FE39 h) = 3Fh - GPIO1_FAULT_RESPONSE
Reg(FE3A h) = 38h - GPIO2_FAULT_RESPONSE
Reg(FE3B h) = 3Fh - GPIO3_FAULT_RESPONSE
Reg(FE3C h) = 38h - GPIO4_FAULT_RESPONSE
Reg(FE3D h) = C0h - PWM_FAULT_MASK
Reg(FE3E h) = 55h - DELAY_TIME_UNIT
Reg(FE3F h) = 00h - WDT_SETTING
Reg(FE40 h) = 35h - GPIO_SETTING
Reg(FE41 h) = 5Ch - GPIO1_2_KARNAUGH_MAP
Reg(FE42 h) = 06h - GPIO3_4_KARNAUGH_MAP
Reg(FE43 h) = 00h - PGOOD_FAULT_DEB
Reg(FE44 h) = 0009h - PGOOD1_FAULT_SELECT
Reg(FE45 h) = 0080h - PGOOD2_FAULT_SELECT
Reg(FE46 h) = 0000h - SOFT_START_BLANKING
Reg(FE47 h) = 0000h - SOFT_STOP_BLANKING
Reg(FE48 h) = 00h - BLACKBOX_SETTING
Reg(FE49 h) = 00h - PWM_DISABLE_SETTING
Reg(FE4A h) = 88h - FILTER_TRANSITION
Reg(FE4B h) = 39h - DEEP_LLM_SETTING
Reg(FE4C h) = 87h - DEEP_LLM_DISABLE_SETTING
Reg(FE4D h) = 44h - OVP_FAULT_CONFIG
Reg(FE4E h) = 21h - CS1_SETTING
Reg(FE4F h) = E5h - CS2_SETTING
Reg(FE50 h) = DEh - PULSE_SKIP_AND_SHUTDOWN
Reg(FE51 h) = 03h - SOFT_START_SETTING
Reg(FE52 h) = 00h - SR_DELAY
```

```
Reg(FE53 h) = DBh - MODULATION_LIMIT
Reg(FE54 h) = 00h - Reserved
Reg(FE55 h) = 42h - SYNC
Reg(FE56 h) = 69h - DUTY_BAL_EDGESEL
Reg(FE57 h) = F1h - DOUBLE_UPD_RATE
Reg(FE58 h) = 83B8h - VIN_SCALE_MONITOR
Reg(FE59 h) = 9B33h - IIN_CAL_GAIN
Reg(FE5A h) = 64h - TSNS_SETTING
Reg(FE5B h) = 07h - AUTO_GO_CMD
Reg(FE5C h) = 01h - DIODE_EMULATION
Reg(FE5D h) = 02h - CS2_CONST_CUR_MODE
Reg(FE5E h) = 00h - NL_ERR_GAIN_FACTOR
Reg(FE5F h) = 24h - SR_SETTING
Reg(FE60 h) = 00h - NOMINAL_TEMP_POLE
Reg(FE61 h) = 00h - LOW_TEMP_POLE
Reg(FE62 h) = 01h - LOW_TEMP_SETTING
Reg(FE63 h) = 13h - GPIO3_4_SNUBBER_ON_TIME
Reg(FE64 h) = 4Ah - GPIO3_4_SNUBBER_DELAY
Reg(FE65 h) = 80h - VOUT_DROOP_SETTING
Reg(FE66 h) = 00h - NL_BURST_MODE
Reg(FE67 h) = F0h - HF_ADC_CONFIG
Board Settings
Input Voltage = 48 V
N1 = 5
N2 = 2
R Normal (CS2) = 0.6 mOhm
I (load) = 20 A
R1 = 11 KOhm
R2 = 1 KOhm
C3 = 1 uF
C4 = 1 uF
N1 (CS1) = 1
N2 (CS1) = 100
R (CS1) = 10 Ohm
ESR (L1) = 1.44 mOhm
L1 = 2.42 uH
C1 = 150 uF
ESR (C1) = 1 mOhm
ESR (L2) = 0 mOhm
L2 = 0 uH
C2 = 820 uF
ESR (C2) = 20 mOhm
R (Normal-Mode) (Load) = 0.6 Ohm
R (Light-Load-Mode) (Load) = 12 Ohm
Cap Across R1 & R2 = 0 "(1 = Yes: 0 = No)"
Switches / Diodes = 1 (0 = Switches: 1 = Diodes)
Second LC Stage = 1 (1 = Yes: 0 = No)
```

R3 = 0 KOhm

R4 = 0 KOhm

C5 = 0 µF

C6 = 0 µF

R6 = 25 KOhm

R7 = 1 KOhm

Topology = 0 (0 = Full Bridge: 1 = Half Bridge: 2 = Two Switch Forward: 3 = Interleaved Two Switch Forward: 4 = Active Clamp Forward)

Restricted_1 = 0

Restricted_2 = 0

Restricted_3 = 1

= 3

SCHEMATICS AND ARTWORK

ADP1055-EVALZ SCHEMATIC

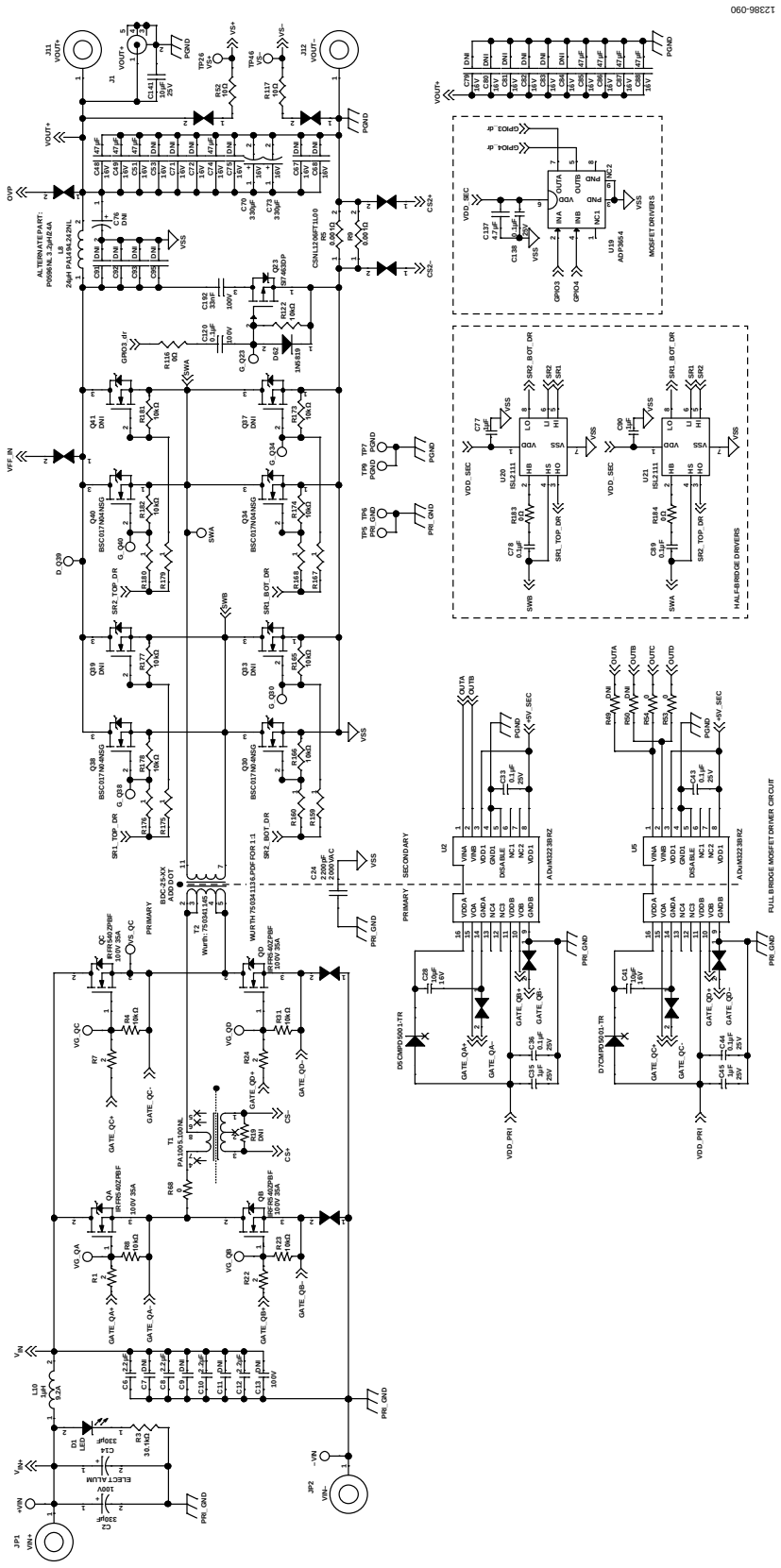

Figure 91. ADP1055 Evaluation Board Schematic—Part 1

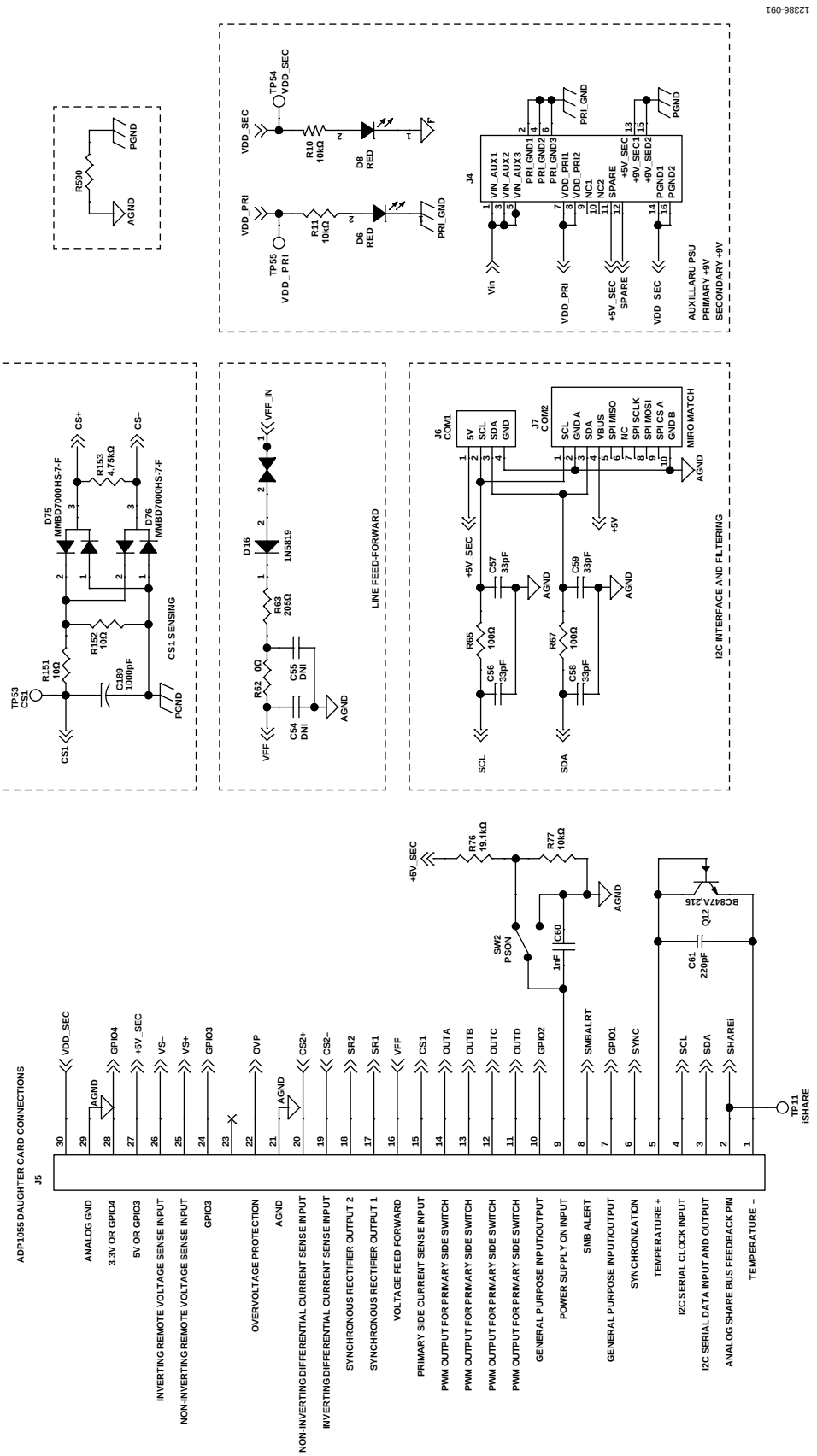

Figure 92. ADP1055 Evaluation Board Schematic—Part 2

ADP1055-EVALZ LAYOUT

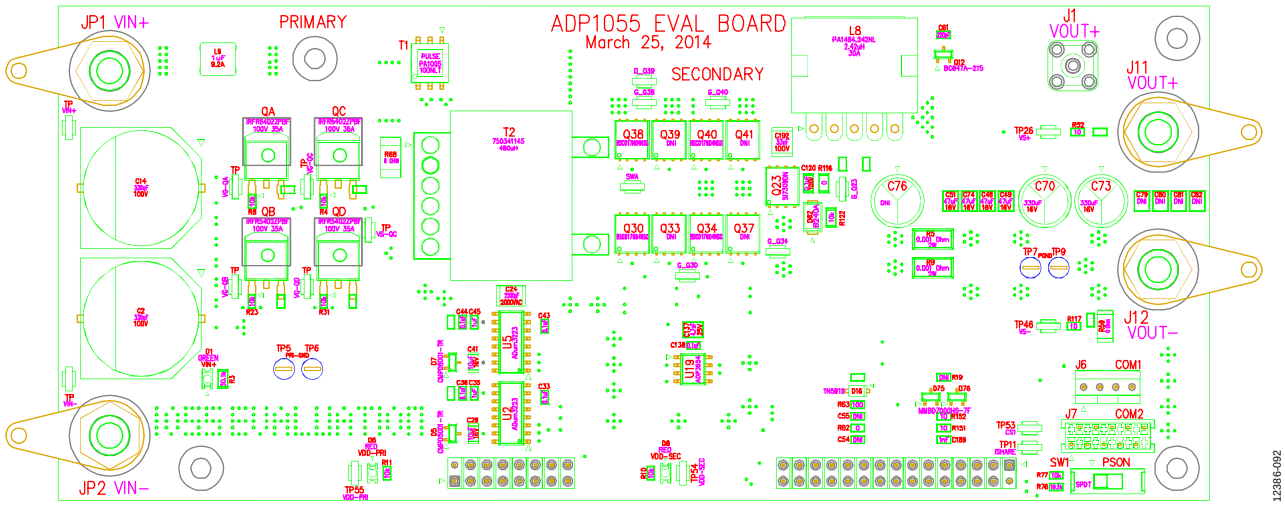

Figure 93. PCB Assembly Top

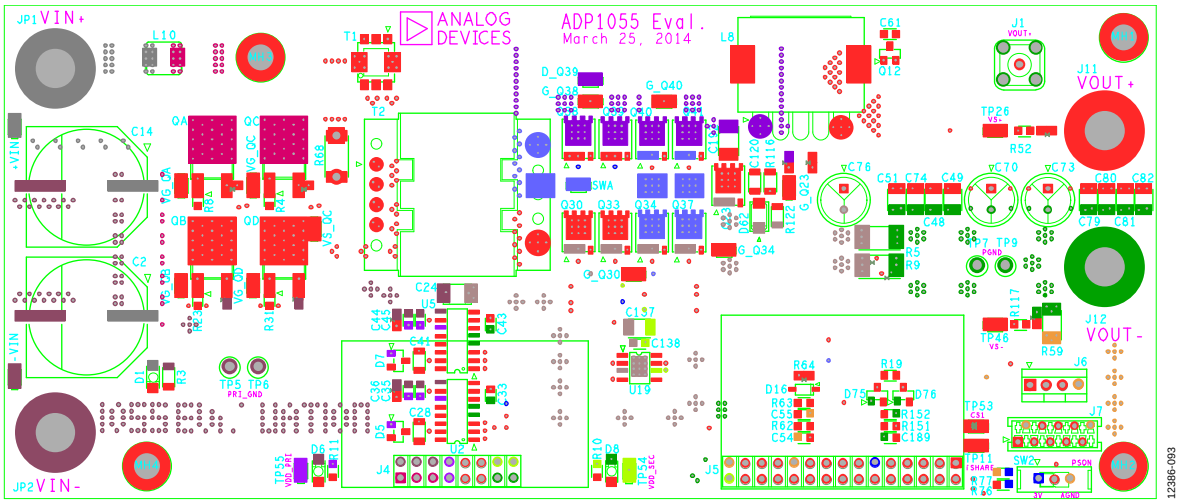

Figure 94. PCB Layout, Silkscreen Layer

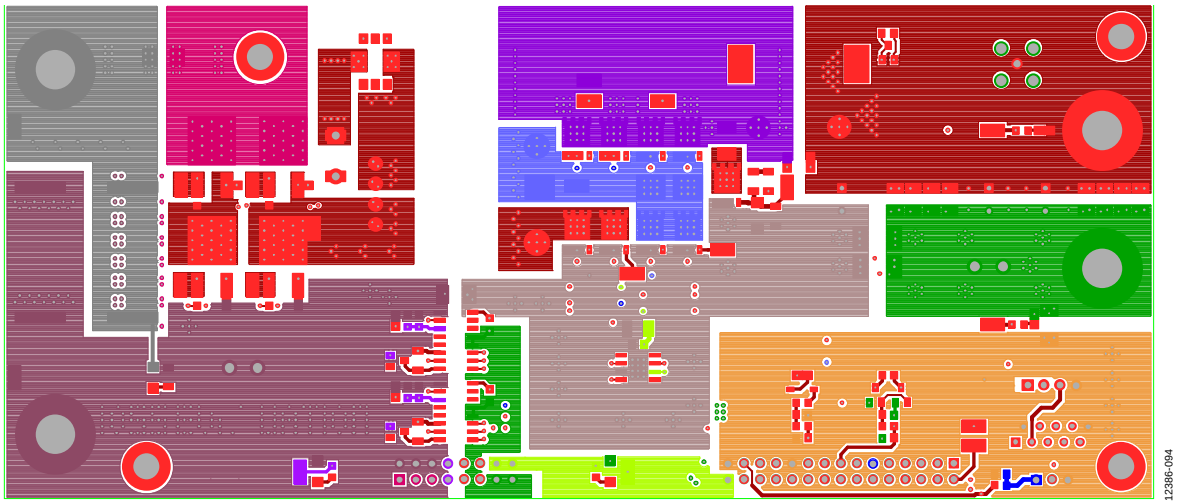

Figure 95. PCB Layout, Top Layer

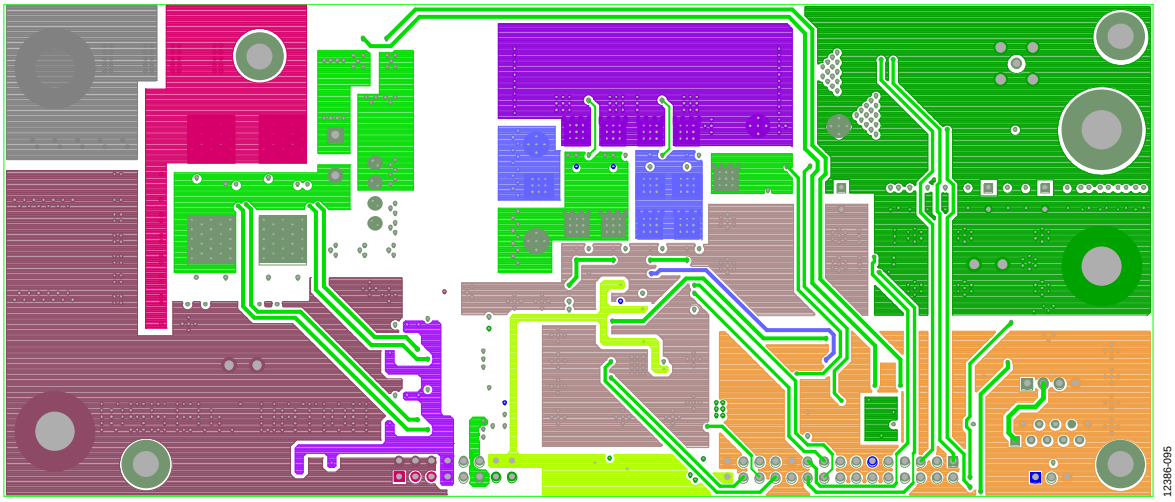

Figure 96. PCB Layout, Layer 2

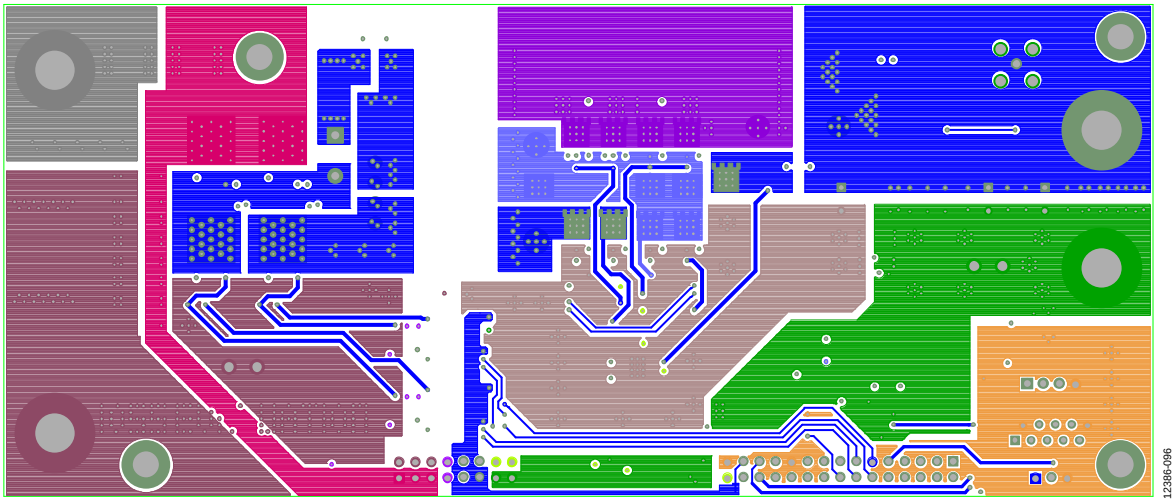

Figure 97. PCB Layout, Layer 3

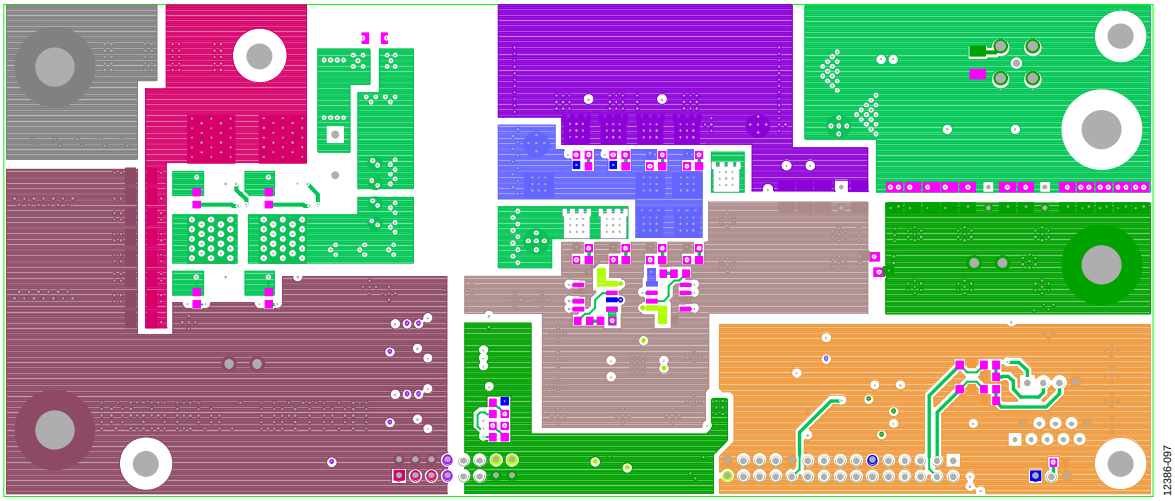

Figure 98. PCB Layout, Layer 4

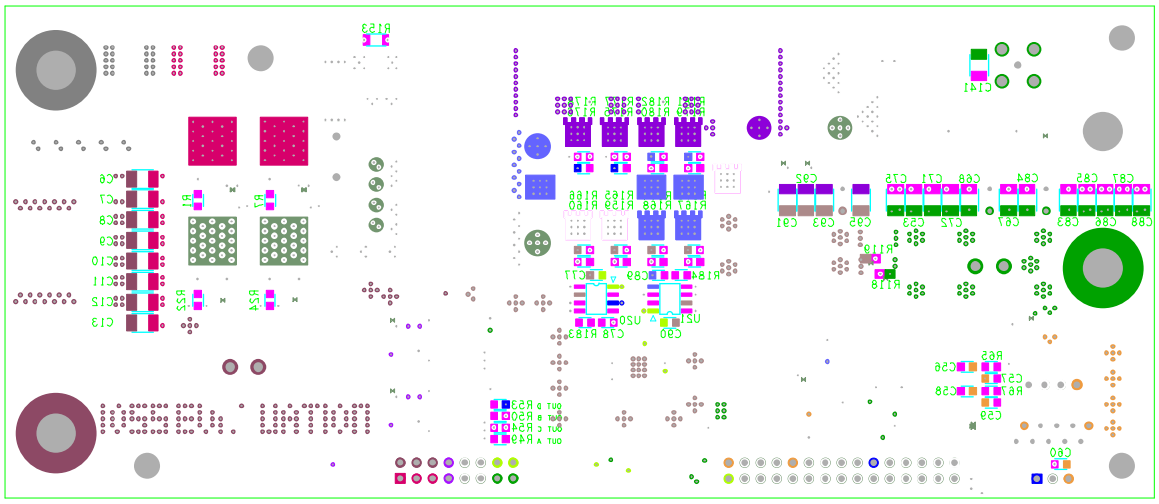

Figure 99. PCB Layout, Bottom Layout

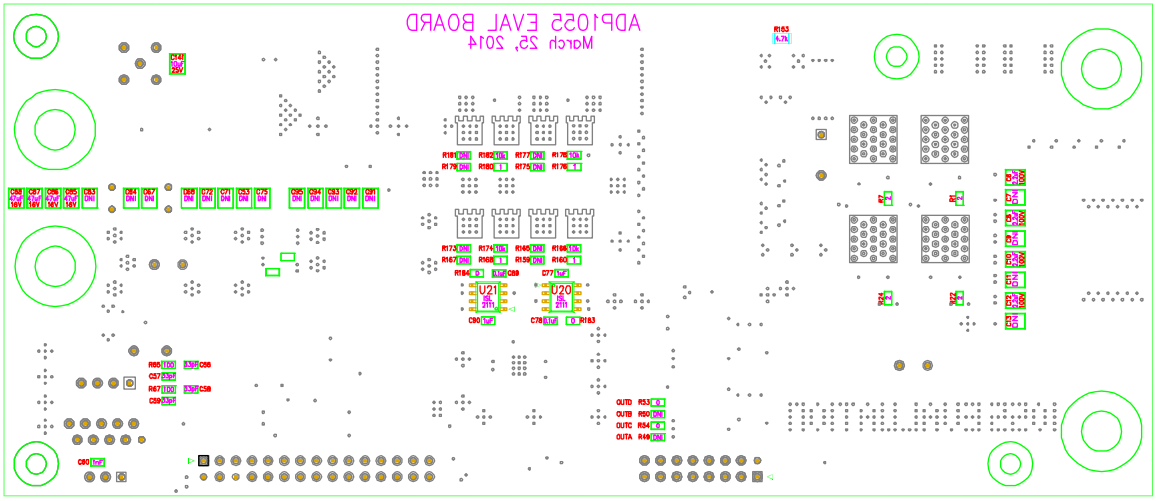

Figure 100. PCB Assembly Bottom

ADP1055DC1-EVALZ SCHEMATIC

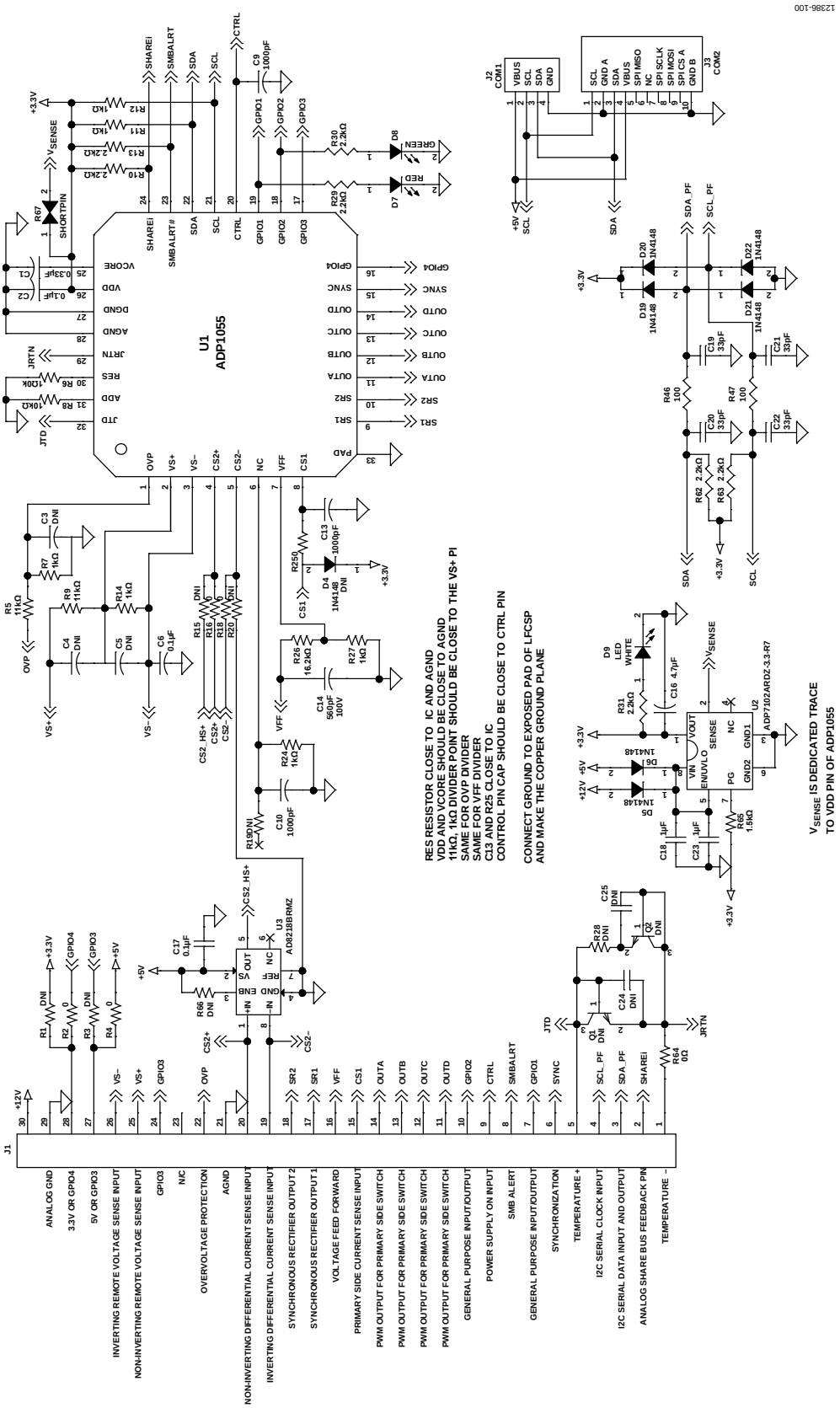

Figure 101. ADP1055 Daughter Card Schematic

ADP1055DC1-EVALZ LAYOUT

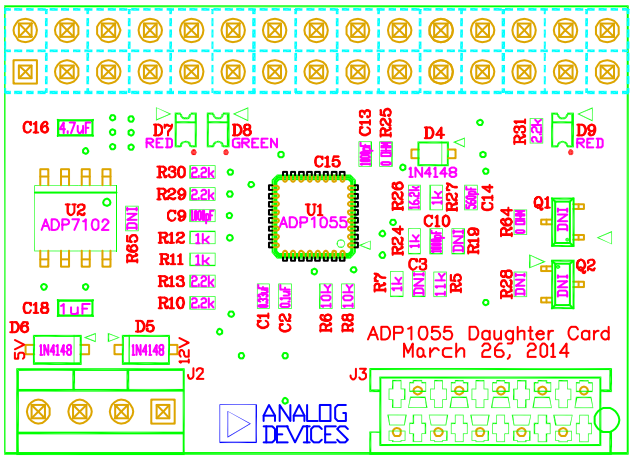

Figure 102. PCB Assembly, Top

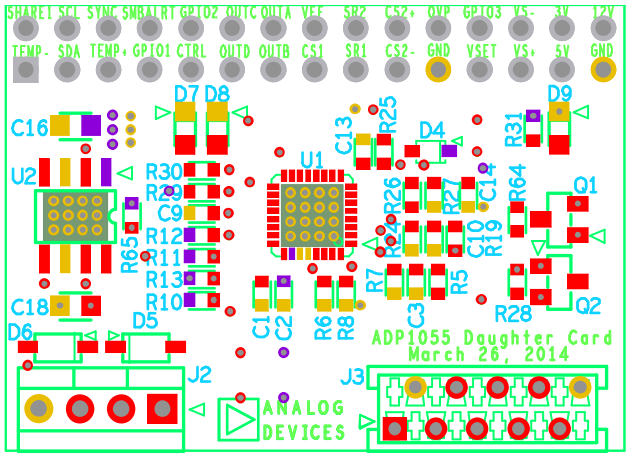

Figure 103. PCB Layout, Silkscreen Layer Top

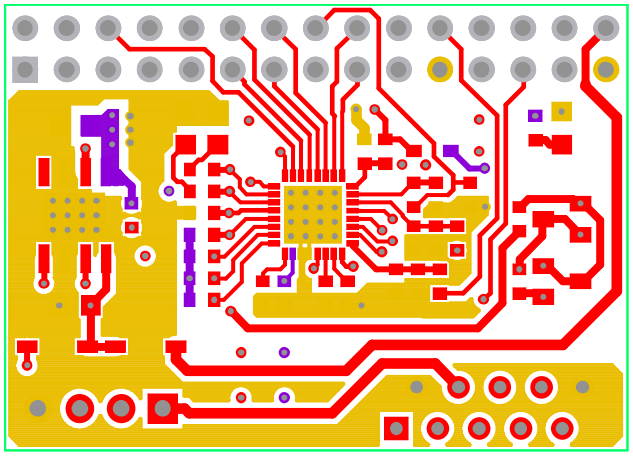

Figure 104. PCB Layout, Top Layer

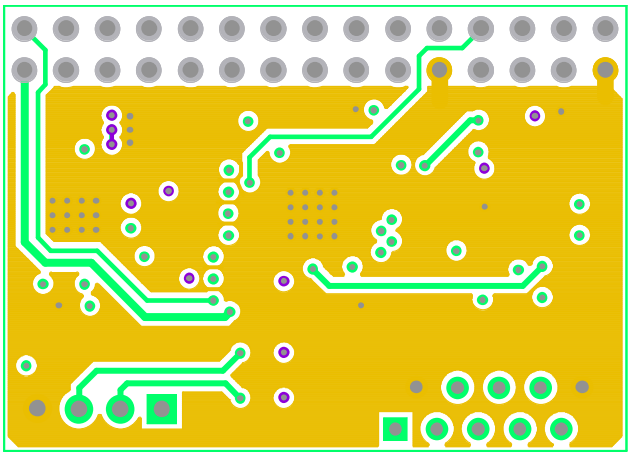

Figure 105. PCB Layout, Layer 2

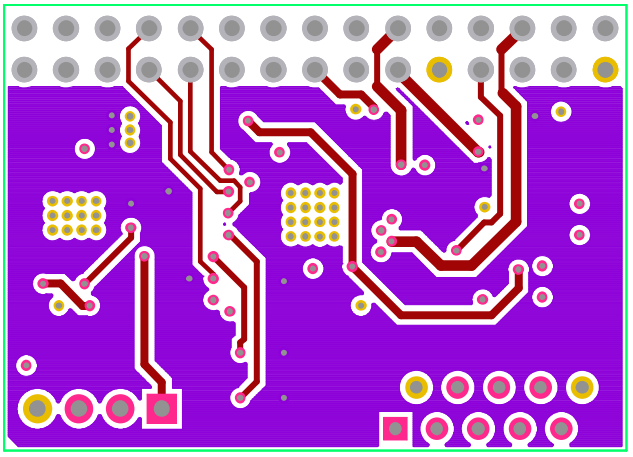

Figure 106. PCB Layout, Layer 3

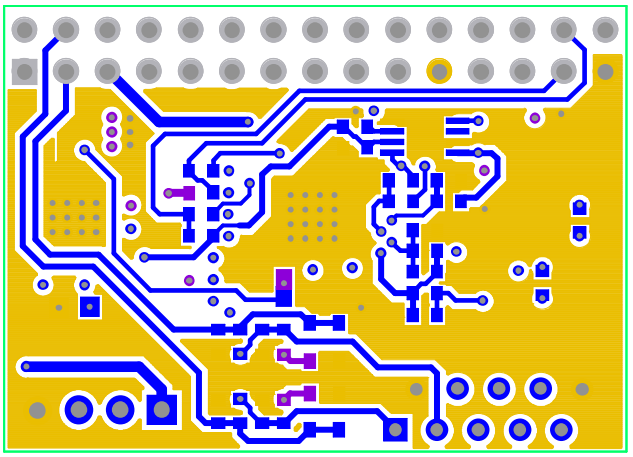

Figure 107. PCB Layout, Bottom Layer

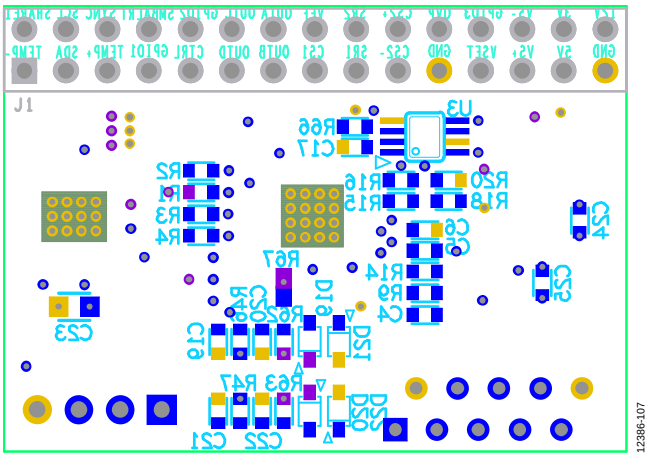

Figure 108. PCB Layout, Silkscreen Bottom

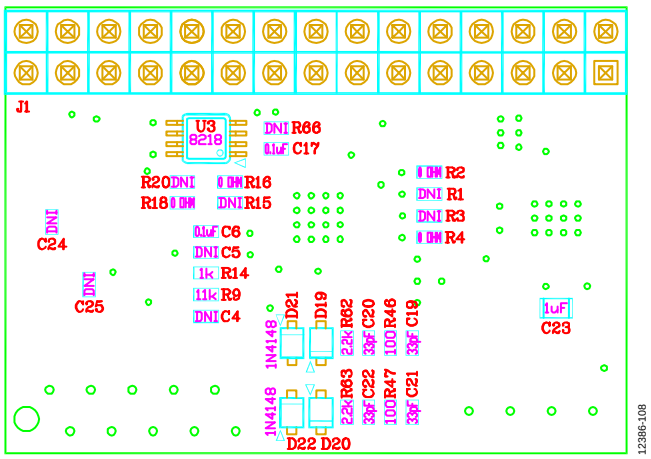

Figure 109. PCB Assembly, Bottom

BILL OF MATERIALS

The section provides the components list for the evaluation board followed by the components list for the daughter card.

Table 5. ADP1055 Evaluation Board Components List

Qty.	Reference	Value	Description	Manufacturer	Part Number
1			PC TEST POINT MINI SMD	Keystone	5019
1			PC TEST POINT MINI SMD	Keystone	5019
1	C2	330 µF	CAP 330 µF 100 V ±20% ELECTROLYTIC ALUM	Digi-Key	EEV-FK2A331M
1	C6	2.2 µF	SMD CAP CER 2.2 µF 100 V X7R	Murata	GCM32DR72A225KA64L
1	C8	2.2 µF	SMD CAP CER 2.2 µF 100 V X7R	Murata	GCM32DR72A225KA64L
1	C10	2.2 µF	SMD CAP CER 2.2 µF 100 V X7R	Murata	GCM32DR72A225KA64L
1	C12	2.2 µF	SMD CAP CER 2.2 µF 100 V X7R	Murata	GCM32DR72A225KA64L
1	C14	330 µF	CAP 330 µF 100 V ±20% ELECTROLYTIC ALUM	Digi-Key	EEV-FK2A331M
1	C24	2200 pF	CAP CER 2200 pF 2 kV 10% X7S SMD	TDK	C4532X7S3D222K160KA
1	C28	10 µF	CAP CER 10 µF 16 V 20% X7R	TDK	C3216X7R1C106M
1	C33	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C35	1 µF	CAP CER 1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C36	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1C104M
1	C41	10 µF	CAP CER 10 µF 16 V 20% X7R	TDK	C3216X7R1C106M
1	C43	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C44	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1C104M
1	C45	1 µF	CAP CER 1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C48	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C49	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C51	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C55	DNI	CAP CER 1000 pF 50 V 10% X7R SMD	AVX	08055C102KAT2A
1	C56	33 pF	CAP CER 33 pF 50 V ±5% NPO SMD	AVX	08055A330JAT2A
1	C57	33 pF	CAP CER 33 pF 50 V ±5% NPO SMD	AVX	08055A330JAT2A
1	C58	33 pF	CAP CER 33 pF 50 V ±5% NPO SMD	AVX	08055A330JAT2A
1	C59	33 pF	CAP CER 33 pF 50 V ±5% NPO SMD	AVX	08055A330JAT2A
1	C60	1 nF	CAP CER 1000 pF 50 V 10% X7R SMD	AVX	08055C102KAT2A
1	C61	220 pF	SMD CAP CER 2200 pF 100 V 10% X7R	AVX	C2012C0G2A221J
1	C70	330 µF	CAP ALUM 300 µF 16 V 20% RADIAL	United	EKZE160ELL331MHB5D
1	C73	330 µF	CAP ALUM 330 µF 16 V 20% RADIAL	United	EKZE160ELL331MHB5D
1	C74	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C77	1 µF	CAP CER 1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C78	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C85	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C86	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C87	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C88	47 µF	CAP CER 47 µF 16 V 10% X5R	Murata	GRM32ER61C476KE15K
1	C89	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C90	1 µF	CAP CER 1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C120	0.1 µF	CAP CERAMIC 0.1 µF 100 V 10% X7R SMD	AVX	12061C104KAT2A

Qty.	Reference	Value	Description	Manufacturer	Part Number
1	C137	4.7 µF	CAP CER 4.7 µF 50 V 10% X7R SMD	Kemet	C1210C475K5RACTU
1	C138	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	C1608X7R1E105K
1	C141	10 µF	CAP CER 10 µF 25 V 10% X7R	TDK	C3216X7R1E106K160AB
1	C189	1000 pF	CAP 1000 pF 50 V 10% X7R SMD	AVX	08055C102KAT2A
1	C192	33 nF	CAP CERAMIC 0.033 µF 100 V 5% NPO SMD	Kemet	C1812C333J1GACTU
1	D_Q39		PC TEST POINT MINI SMD	Keystone	5019
1	D1		LED SUPER RED CLEAR 75 MA 1.7 V SMD	Digi-Key	CMD15-21SRC/TR8
1	D5		DIODES POWER SWITCHING 120 V 400 mA	Central Semiconductor	CMPD5001-TR
1	D6	LED Green	LED HI EFF RED CLEAR SMD	Visual	CMD15-21VRC/TR8
1	D7		DIODES POWER SWITCHING 120 V 400 mA	Central Semiconductor	CMPD5001-TR
1	D8	LED Green	LED HI EFF RED CLEAR SMD	Visual	CMD15-21VRC/TR8
1	D16		DIODE SCHOTTKY 40 V 1A SMD	Diodes	1N5819HW-7-F
1	D62		DIODE SCHOTTKY 40 V 1A SMD	Diodes	1N5819HW-7-F
1	D75		DIODE ARRAY 100 V 300 mA	Diodes	MMBD7000HS-7-F
1	D76		DIODE ARRAY 100 V 300 mA	Diodes	MMBD7000HS-7-F
1	G_Q23		PC TEST POINT MINI SMD	Keystone	5019
1	G_Q30		PC TEST POINT MINI SMD	Keystone	5019
1	G_Q34		PC TEST POINT MINI SMD	Keystone	5019
1	G_Q38		PC TEST POINT MINI SMD	Keystone	5019
1	G_Q40		PC TEST POINT MINI SMD	Keystone	5019
1	JP1	VIN+	CONN JACK BANANA UNINS PANEL MOU	Emerson	108-0740-001
1	JP2	VIN−	CONN JACK BANANA UNINS PANEL MOU	Emerson	108-0740-001
1	J1	BNC/R	CONN JACK VERTICAL PCMNT GOLD	Emerson	131-3701-261
1	J4	CON16	CONN HEADER BRKWAY 0.100 16 POS STR	TE	4-102973-0-08
1	J5	CON30	CONN HEADER BRKWAY 0.100 30 POS STR	TE	4-102973-0-15
1	J6	HDR1X4	CONN HEADER 4 POS SGL PCB 30 GOLD	FCI	69167-104HLF
1	J7	HDR1X4	CONN FMALE ON BRD 10 POS VERT T/H	TE Conn	8-215079-0
1	J11	VOUT+	CONN JACK BANANA UNINS PANEL MOU	Emerson	108-0740-001
1	J12	VOUT−	CONN JACK BANANA UNINS PANEL MOU	Emerson	108-0740-001
1	L8		INDUCTOR PWR 2.42 µH SMD	Pulse	PA1494.242NL
1	L10	1 µH	INDUCTOR POWER 1.0 µH 9.2 A SMD	Vishay Dale	IHLP2020CZER1R0M01
1	QA		MOSFET N-CH 100 V 35 A	International	IRFR540ZPBF
1	QB		MOSFET N-CH 100 V 35 A	International	IRFR540ZPBF
1	QC		MOSFET N-CH 100 V 35 A	International	IRFR540ZPBF
1	QD		MOSFET N-CH 100 V 35 A	International	IRFR540ZPBF
1	Q12		TRANSISTOR NPN 45 V 100 MA SMD	NXP	BC847C,215
1	Q23		MOSFET P-CH 60 V 8 A	Vishay	SI7463DP
1	Q30		MOSFET N-CH 40 V 100 A	Infineon	BSC017N04NS G
1	Q34		MOSFET N-CH 40 V 100 A	Infineon	BSC017N04NS G
1	Q38		MOSFET N-CH 40 V 100 A	Infineon	BSC017N04NS G
1	Q40		MOSFET N-CH 40 V 100 A	Infineon	BSC017N04NS G
1	R1	2	RES 2.00 Ω 1/8 W 1% SMD	Yageo	RC0805FR-072RL
1	R3	30.1k	RES 24.9 kΩ 1/3 W 1% SMD	Digi-Key	CRCW121024K9FKEA

Qty.	Reference	Value	Description	Manufacturer	Part Number
1	R4	10K	RES 10 kΩ 1/ 4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R5	0.001	RES 0.001 Ω 21% SMD	Bourns Inc	CRF2512-FV-R001ELF
1	R7	2	RES 2.00 Ω 1/8 W 1% SMD	Yageo	RC0805FR-072RL
1	R8	10K	RES 10 kΩ ¼ W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R9	0.001	RES 0.001 Ω 2 W 1% SMD	Bourns, Inc	CRF2512-FV-R001ELF
1	R10	10k	RES 10.0 kΩ 1/8 W 1% SMD	Yageo	RC0805FR-0710KL
1	R11	10K	RES 10.0 kΩ 1/8 W 1% SMD	Yageo	311-10.0KCRCT-ND
1	R22	2	RES 2.00 Ω 1/8 W 1% SMD	Yageo	RC0805FR-072RL
1	R23	10K	RES 10 kΩ ¼ W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R24	2	RES 2.00 Ω 1/8 W 1% SMD	Yageo	RC0805FR-072RL
1	R31	10K	RES 10 kΩ ¼ W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R52	10	SMD RES 10 Ω ¼ W 5%	Stackpole	RNCP0805FTD10R0
1	R53	0	RES 0.0 Ω 1/8 W JUMP SMD	Yageo	RC0805FR-070RL
1	R54	0	RES 0.0 Ω 1/8 W JUMP SMD	Yageo	RC0805FR-070RL
1	R58		SHORTPIN		
1	R59		SMD RES 0 Ω 3/4 W 5%	Vishay/Dale	311-1.00CRCT-ND
1	R60		SHORTPIN		
1	R61		SHORTPIN		
1	R62	0	RES 0.0 Ω 1/8 W JUMPER SMD	Yageo	RC0805JR-070RL
1	R63	205	RES 205 Ω 1/8 W 5% SMD	Yageo	RC0805JR-07100RL
1	R64		SHORTPIN		
1	R65	100	RES 100 Ω 1/8 W 1% SMD	Yageo	311-100CRCT-ND
1	R66		SHORTPIN		
1	R67	100	RES 100 Ω 1/8 W 1% SMD	Yageo	311-100CRCT-ND
1	R68	0	RES 0.0 Ω 3/4 W 1% SMD	Vishay	CRCW20100000Z0EF
1	R69		SHORTPIN		
1	R70		SHORTPIN		
1	R76	19.1k	RES 19.1 kΩ 1/8 W 1% SMD	Yageo	311-100CRCT-ND
1	R77	10k	RES 10 kΩ 1/8 W 1% SMD	Yageo	311-100CRCT-ND
1	R116	0	SMD RES 0 Ω 3/4 W 5%	Stackpole	311-1.00CRCT-ND
1	R117	10	SMD RES 10 Ω 1/4 W 5%	Stackpole	RNCP0805FTD10R0
1	R118		SHORTPIN		
1	R119		SHORTPIN		
1	R122	10k	RES 10.0 KΩ 1/2 W 1% SMD	Stackpole	RNCP1206FTD10K0
1	R123		SHORTPIN		
1	R124		SHORTPIN		
1	R125		SHORTPIN		
1	R126		SHORTPIN		
1	R151	10	RES 0.0 Ω 1/8 W 5% SMD	Yageo	RC0805JR-070RL
1	R152	10	RES 10 Ω 1/8 W 1% SMD	Yageo	RC0805FR-077K15L
1	R153	4.75K	RES 4.75 kΩ 1/4 W 1% SMD	Vishay/Dale	CRCW12064K75FKEA
1	R159	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R160	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00

Qty.	Reference	Value	Description	Manufacturer	Part Number
1	R165	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R166	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R167	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R168	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R173	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R174	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R175	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R176	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R177	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R178	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R179	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R180	1	RES 1.0 Ω 1/4 W 1% SMD	Stackpole	CSR0805FK1R00
1	R181	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R182	10k	RES 10.0 kΩ 1/4 W 1% SMD	Stackpole	RNCP0805FTD10K0
1	R183	0	RES 0.0 Ω 1/8 W JUMP SMD	Yageo	RC0805JR-070RL
1	R184	0	RES 0.0 Ω 1/8 W JUMP SMD	Yageo	RC0805JR-070RL
1	SWA		PC TEST POINT MINI SMD	Keystone	5019
1	SW2	PSON	SW SLIDE SPDT 30 V 0.2 A PC MOUNT	E Switch	EG1218
1	TP5		TEST POINT HAND MADE CRAFTS	Analog Devices	
1	TP6		TEST POINT HAND MADE CRAFTS	Analog Devices	
1	TP7		TEST POINT HAND MADE CRAFTS	Analog Devices	
1	TP9		TEST POINT HAND MADE CRAFTS	Analog Devices	
1	TP11		PC TEST POINT MINI SMD	Keystone	5019
1	TP26		PC TEST POINT MINI SMD	Keystone	5019
1	TP46		PC TEST POINT MINI SMD	Keystone	5019
1	TP53		PC TEST POINT MINI SMD	Keystone	5019
1	TP54		PC TEST POINT MINI SMD	Keystone	5019
1	TP55		PC TEST POINT MINI SMD	Keystone	5019
1	T1		XFRMR CURR SENSE 2.0MH 1:10 SMD	Pulse	PA1005.100NLT
1	T2		TRANSFORMER PLANAR 480 µH SMD	Wurth	750341145
1	U2		IC DGTL ISO 2CH LOGIC	Analog Devices	ADuM3223
1	U5		IC DGTL ISO 2CH LOGIC	Analog Devices	ADuM3223
1	U19		IC MOSFET DRV 4 A DUAL HS	Analog Devices	ADP3654ARDZ
1	U20		IC MSFT HALF-BRG 100 V	Intersil	ISL2111ABZ
1	U21		IC MSFT HALF-BRG 100 V	Intersil	ISL2111ABZ
1	VG_QA		PC TEST POINT MINI SMD	Keystone	5019
1	VG_QB		PC TEST POINT MINI SMD	Keystone	5019
1	VG_QC		PC TEST POINT MINI SMD	Keystone	5019
1	VG_QD		PC TEST POINT MINI SMD	Keystone	5019
1	VS_QC		PC TEST POINT MINI SMD	Keystone	5019

Table 6. ADP1055 Daughter Card Components Listing

Qty.	Reference	Value	Description	Manufacturer	Part Number
	C1	0.33 µF	CAP CER 0.33 µF 10% 50 V X5R SMD	TDK	C1608X5R1H334K080AB
1	C2	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R	Murata	GRM188R71E104KA01D
1	C6	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R	Murata	GRM188R71E104KA01D
1	C9	1000 pF	CAP CER 1000 pF 50 V 20% X7R SMD	Murata	GRM188R71H102MA01D
1	C10	1000 pF	CAP CER 1000 pF 50 V 20% X7R SMD	Murata	GRM188R71H102MA01D
1	C13	1000 pF	CAP CER 1000 pF 50 V 20% X7R SMD	Murata	GRM188R71H102MA01D
1	C14	560 pF	SMD CAP CER 560 pF 100 V 10% X7R	Murata	GRM188R72A561KA01D
1	C16	4.7 µF	CAP CER 4.7 µF 10 V 10% X7R SMD	Taiyo Yuden	LMK212B7475KG-T
1	C17	0.1 µF	CAP CER 0.1 µF 25 V 10% X7R SMD	Murata	GRM188R71E104KA01D
1	C18	1 µF	CAP CER 1 µF 25 V 10% X7R SMD	Murata	GCM21BR71E105KA56L
1	C19	33 pF	CAP CER 33 pF 50 V 5% NPO SMD	Panasonic	ECJ-1VC1H330J
1	C20	33 pF	CAP CER 33 pF 50 V 5% NPO SMD	Panasonic	ECJ-1VC1H330J
1	C21	33 pF	CAP CER 33 pF 50 V 5% NPO SMD	Panasonic	ECJ-1VC1H330J
1	C22	33 pF	CAP CER 33 pF 50 V 5% NPO SMD	Panasonic	ECJ-1VC1H330J
1	C23	1 µF	CAP CER 1 µF 25 V 10% X7R SMD	Murata	GCM21BR71E105KA56L
1	D4	1N4148	DIODE SW 150MA 75 V	Micro Commercial	1N4448WX-TP
1	D5	1N4148	DIODE SW 100 V 200 MA	ON Semi	MMSD4148T3G
1	D6	1N4148	DIODE SW 100 V 200 MA	ON Semi	MMSD4148T3G
1	D7	LED Green	LED THIN 660 NM SUPRED SMD	Lumex Opto	SML-LXT0805SRW-TR

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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