ANALOG DEVICES

AN-1141
APPLICATION NOTE

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Powering a Dual Supply Precision ADC with Switching Regulators

by Rui Du

INTRODUCTION

Compared with an LDO device, a switching regulator always dissipates much less heat and provides higher efficiency. Therefore, a switching regulator is suitable for powering different kinds of portable devices or the nodes in a wireless sensor network to lengthen battery time. Unfortunately, a switching regulator intrinsically generates ripple and noise at both the output rail and the ground. At the same time, a switching regulator brings electromagnetic radiation. These interferences are almost inevitable due to the continuously on-off operation of the power switch. With the parasitic parameters involved, the noise will be present at unexpected frequency points besides the integer multiple of the switching frequency.

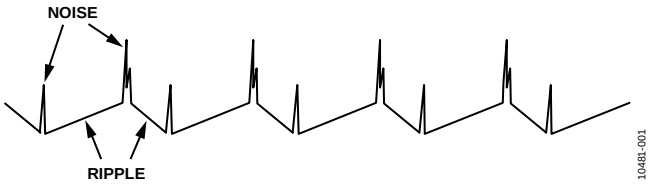

Figure 1. Typical Ripple and Noise at the Output of a Switching Regulator

Although damaged from the noise issues, if the interference of the switching regulator can be effectively controlled while the circuit is powered by a switching regulator, which has a strong anti-interference capacity, then the degrading of the system performance will be slight.

For a typical application, when a data converter is powered by a switching mode power supply (SMPS), keep the total noise over the band of interest lower than the noise floor to prevent it from being seen by the converter. Although the in-band noise from the switching regulator is normally greater than the noise floor, because of the power rejection ratio of the ADC, the noise will be sharply attenuated before entering the signal path; as a result, the switching noise will not degrade the performance of the ADC.

There are two options to power the ADC with switching regulators:

A. Select a low noise switching regulator and then use carefully designed filtering and shielding methods to remove as much of the noise as possible.
B. Estimate the noise suppressing capability of the data converter, and then select the product, which has good noise-immunity performance.

In practice, both options can be used at the same time so that the power solution of using a switching regulator can be acceptable in most cases. The switching regulator solution includes the benefits of high efficiency and low temperature.

In CN-0137, a dual-output synchronous buck switching regulator, ADP2114, is used to power the 16-bit, 125 MSPS analog-to-digital converter, AD9268. The outputs of ADP2114 are filters using an extra stage of an LC filter (ferrite bead).

Compared with the linear supplies solution, the testing result shows that using a dc-to-dc supply has nearly no influences on the performance of the ADC (see Table 1).

Table 1. Experiment Results Reported in CN-0137

	Linear Supplies		DC-to-DC Supply	
Analog Input Frequency (MHz)	**SNR (dBFS)**	**SFDR (dBc)**	**SNR (dBFS)**	**SFDR (dBc)**
10.3	79.2	92.2	79.2	92.3
70.0	78.5	91.0	78.4	90.8
100.3	77.8	85.8	77.7	85.6
140.3	76.9	85.0	76.9	84.8
170.3	76.2	84.3	75.9	84.6
200.3	75.0	76.9	75.0	77.0

The noise performance of the ADP2114 is guaranteed by multiple technologies implemented in the design. The typical voltage ripple is less than 1 mV. Using additional filtering, its noise performance can even align with linear supplies.

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REVISION HISTORY

2/12—Revision 0: Initial Version

EXPERIMENT RESULTS

In this application note, a switching regulator is used to power the ADC without any additional filtering or shielding measures, only the necessary external components kept for normal operation of the dc-to-dc power supply. According to the second option mentioned previously, two power-insensitive ADCs, the AD7610 and AD7612 are used for testing. This application note aims at finding out how much harm is brought by the SMPS to the ADC and whether it is acceptable.

The AD7610 and AD7612 are 16-bit charge redistribution successive approximation register (SAR) analog-to-digital converters. They feature true bipolar analog input range. The analog input signal should never exceed the supply rails by more than 0.3 V. For ±10 V input, a typical power supply is ±12 V. See the AD7610 and AD7612 data sheets available from www.analog.com.

More importantly, the AD7610 and AD7612 provide excellent power rejection ratio. They are very insensitive to power supply variations on AVDD over a wide frequency range (see Figure 2).

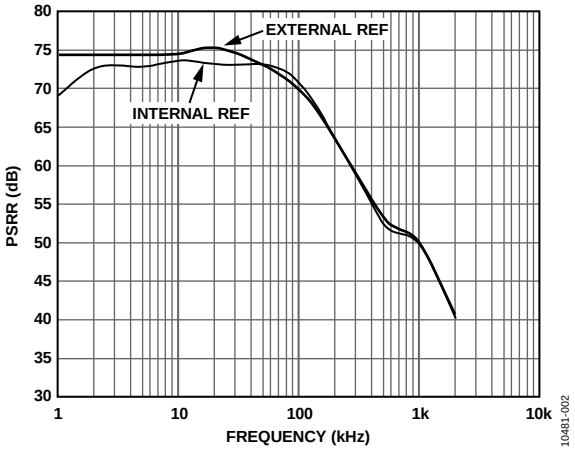


Figure 2. AVDD PSRR vs. Frequency of AD7610 or AD7612

Figure 3 shows an equivalent circuit for the input structure of the AD7610 and AD7612. The analog input is first handled by the high voltage branches (powered by VCC and VEE) and scaled down to 0 V to 5 V.

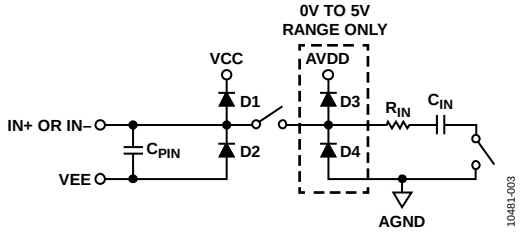


Figure 3. Simplified Analog Input Structure of AD7610 or AD7612

This analog input structure allows the sampling of the differential signal between IN+ and IN−. By using this differential input, small signals common to both inputs are rejected as shown in Figure 4, which represents the typical CMRR over frequency.

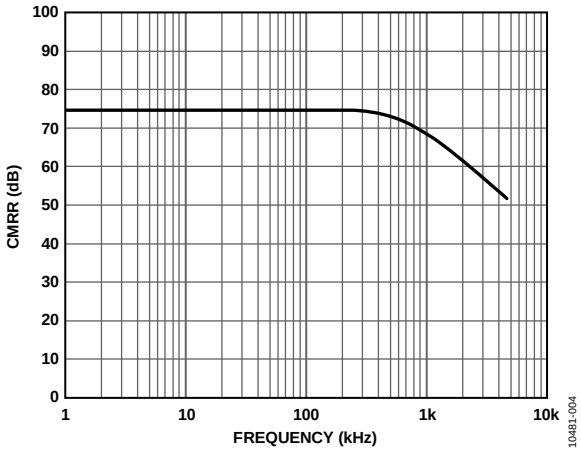


Figure 4. Analog Input CMRR vs. Frequency of AD7610 or AD7612

For powering the AD7610 and AD7612, a 5 V to ±12 V power module using the ADP1613 (the boost dc-to-dc converts 5 V to 12 V) and ADP2301 (the inverting dc-to-dc converts +5 V to −12 V) was designed. For more information about the inverting converter application of ADP2301, refer to the AN-1083 Application Note.

The power solution is made to help those customers, who only have 5 V on-board to generate ±12 V with high-current ability and high-efficiency (see Figure 5).

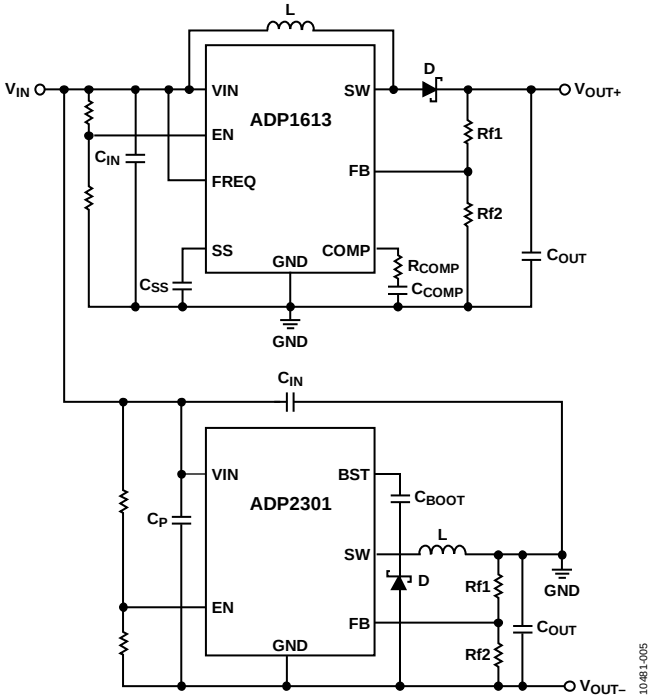


Figure 5. Schematic of the 5 V to ±12 V Power Module Using ADP1613 or ADP2301

For a SMPS, the output-voltage ripple can be suppressed by using a big inductor and output capacitor in the topology. To deal with the switching noise, an extra filter at the output can be used. By doing this, the PCB area will be sacrificed.

The basic configuration of the 5 V to ±12 V power modules is shown in Table 2.

Table 2. Basic Configuration for the ±12 V Power Modules

	Output	
Configuration	**+12 V**	**−12 V**
Switching Frequency	1.3 MHz	1.4 MHz
Output Inductor	10 µH	8.2 µH
Input Capacitor	10 µF	10 µF
Output Capacitor	10 µF	44 µF
Maximum Load	400 mA	200 mA

Note the following about the ripple and noise performance under the typical loading (50% of full load):

- For the +12 V rail of the power module:
  - the ripple ≈ 20 mV p-p
  - the noise ≈ 140 mV p-p (oscilloscope in 1 MΩ mode)
- For the −12 V rail of the power module:
  - the ripple ≈ 10 mV p-p
  - the noise ≈ 50 mV p-p (oscilloscope in 1 MΩ mode)

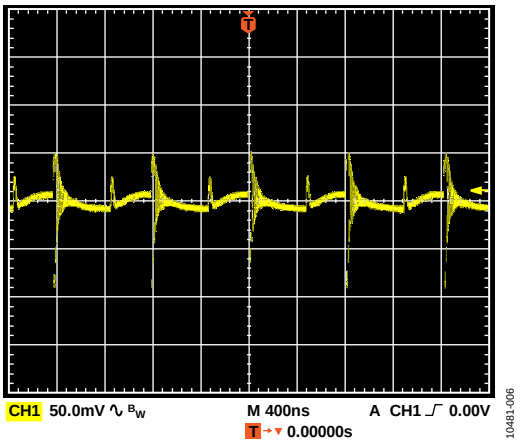


Figure 6. AC-Coupled Output Voltage of the +12 V Rail

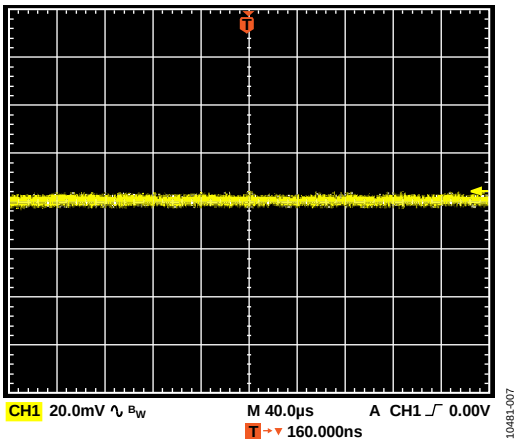


Figure 7. Filtered Output Voltage of the +12 V Rail (AC-Coupled)

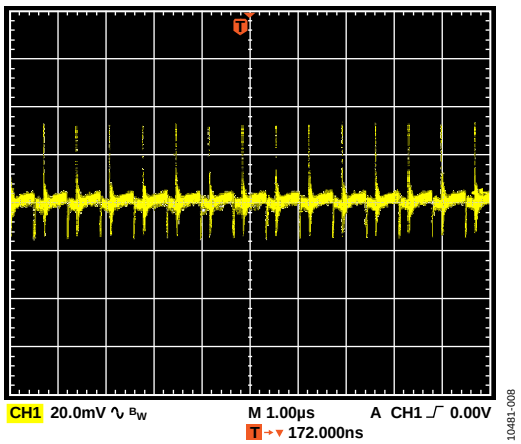


Figure 8. AC-Coupled Output Voltage of the −12 V Rail

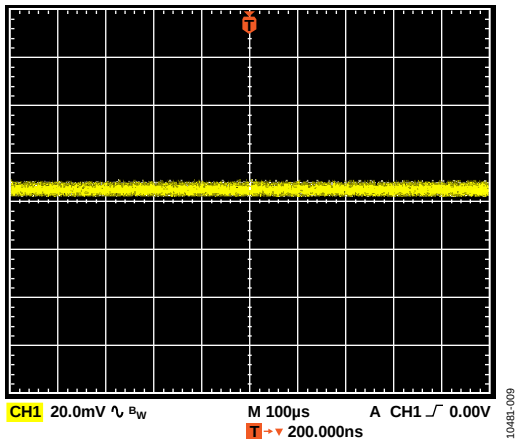


Figure 9. Filtered Output Voltage of the −12 V Rail (AC-Coupled)

When 2-stage filters are added to the output (the first stage is the LC filter, and the second stage is the bead + decoupling capacitor), most of the ripple and noise can be removed. However, in all the experiments mentioned in this application note, the original output, no extra filters, was used.

EXPERIMENT 1

The first experiment was performed based on AD7612-EVAL and ADuC7026-EVAL. The ADuC7026-EVAL was used to read the conversion results.

The input range of AD7612 is configured as ±5 V.

The analog inputs of AD7612 (IN+ and IN−) are both directly grounded, the input buffers on the evaluation board are bypassed (see Figure 10).

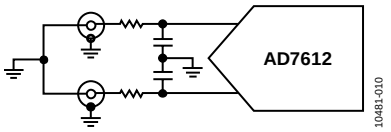


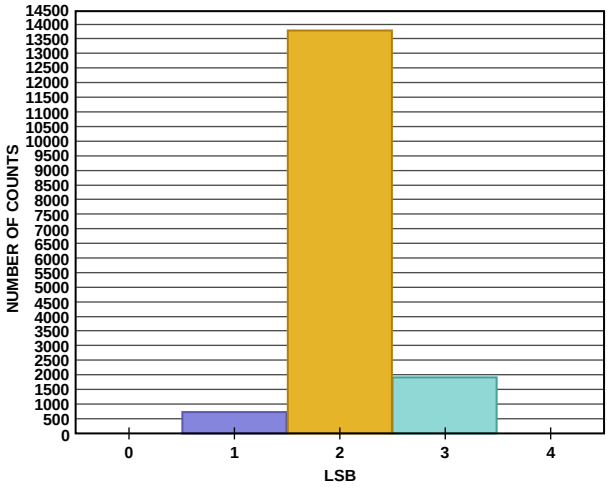
Figure 10. Simplified Schematic for Experiment 1. The 3 dB Bandwidth of the Input Anti-Aliasing Filter is about 4 MHz.

Two power supply configurations were used in the experiment:

- Configuration A: VCC and VEE of the AD7612 are powered by the ±12 V power module based on ADP1613 and ADP2301. The +5 V AVDD and DVDD are powered by high quality linear dc power.
- Configuration B: For comparison, VCC, VEE, AVDD, and DVDD are all provided by the high quality linear dc power.

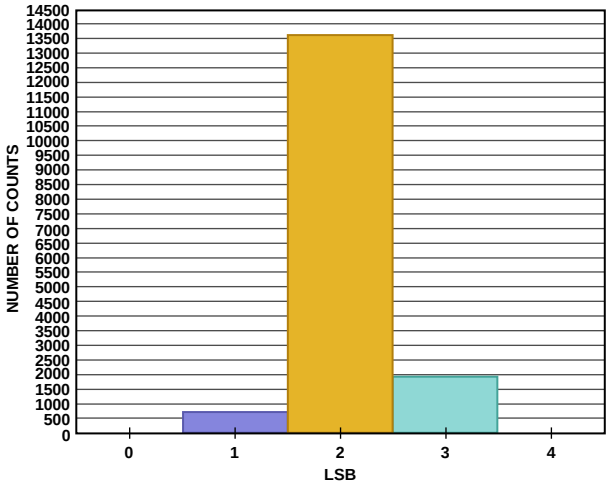
During the test, 16,384 conversions were performed.

The testing results for Configuration A and Configuration B are shown in Figure 11 and Figure 12.



LSB	NUMBER OF COUNTS
0x0000	0
0x0001	664
0x0002	13862
0x0003	1857
0x0004	1
μ	2.0729
δ	0.3857

Figure 11. Testing Results—Histogram for Power Supply Configuration A



LSB	NUMBER OF COUNTS
0x0000	0
0x0001	717
0x0002	13769
0x0003	1898
0x0004	0
μ	2.0721
δ	0.393

Figure 12. Testing Results—Histogram for Power Supply Configuration B

Following are the calculations for mean and variance:

For Configuration A,
mu (μ) = 2.0729 LSB
sigma (δ) = 0.3857 LSB

The peak-to-peak noise ≈ 2.5456 LSB

peak-to-peak resolution ≈

$$\log_2\left(\frac{2^{16}}{2.5456}\right) \approx \log_2 10 \times 4.411 \approx 14.65 \text{ bits}$$

For an interval estimation,
The 95% confidence interval of μ is [2.0670, 2.0788]
The 95% confidence interval of δ is [0.3816, 0.3900]

For Configuration B,
mu (μ) = 2.0721 LSB
sigma (δ) = 0.3930 LSB

The peak-to-peak noise ≈ 2.5938 LSB

peak-to-peak resolution ≈

$$\log_2\left(\frac{2^{16}}{2.5938}\right) \approx \log_2 10 \times 4.403 \approx 14.63 \text{ bits}$$

For an interval estimation,
The 95% confidence interval of μ is [2.0661, 2.0781]
The 95% confidence interval of δ is [0.3888, 0.3973]

The change of peak-to-peak resolution is within 0.03 bit, using SNR = 6.02 N + 1.76. The change of the SNR is within 0.2 dB.

EXPERIMENT 2

The second experiment was performed based on the AD7610-EVAL. The FIFO board (EVAL-Control BRDXZ) and the evaluation software were used to analyze the conversion results.

The input range of AD7610 is configured as ±5 V.

The input buffers are enabled (AD8021). The inputs of AD8021s are both grounded. The AD8021 is dual-supply operation, using the same ±12 V rails as AD7610 (see Figure 13).

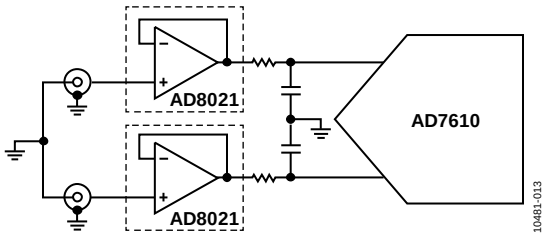


Figure 13. Simplified Schematic for Experiment 2. The 3 dB Bandwidth of the Input Anti-Aliasing Filter is about 4 MHz.

Two power supply configurations were used in the experiment:

- Configuration A: Using high quality linear dc power to provide +12 V VCC, −12 V VEE, +5 V AVDD, and +5 V DVDD (and power the input buffer).
- Configuration B: Using high quality linear dc power to provide +5 V AVDD, +5 V DVDD; using ±12 V SMPS to provide +12 V VCC, −12 V VEE (and to power the input buffer).

The testing results for Configuration A and Configuration B are shown in Figure 14 to Figure 19.

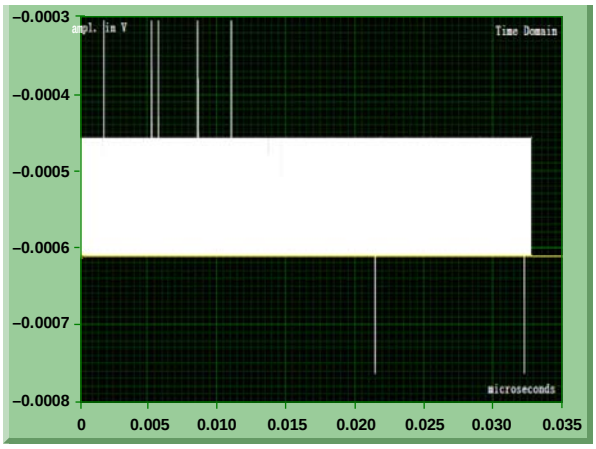


Figure 14. Time Domain Waveform for Power Supply, Configuration A

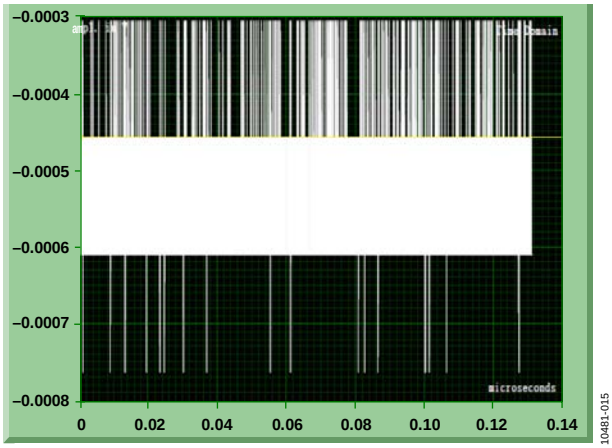


Figure 15. Time Domain Waveform for Power Supply, Configuration B

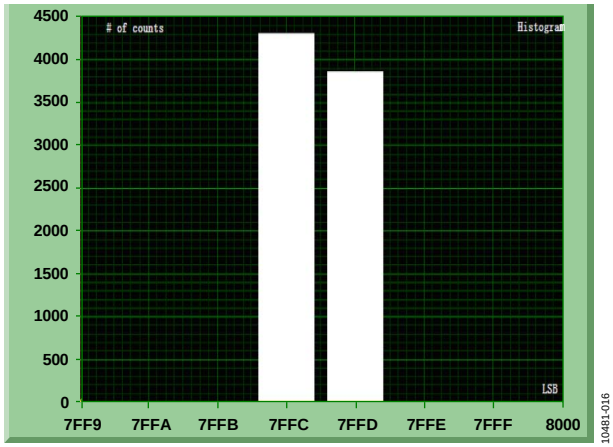


Figure 16. Histogram for Power Supply, Configuration A

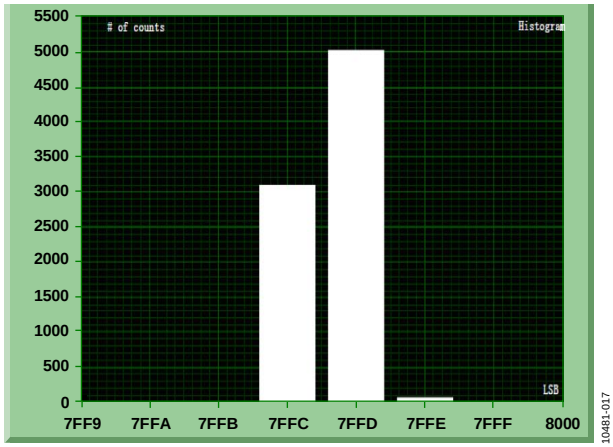


Figure 17. Histogram for Power Supply, Configuration B

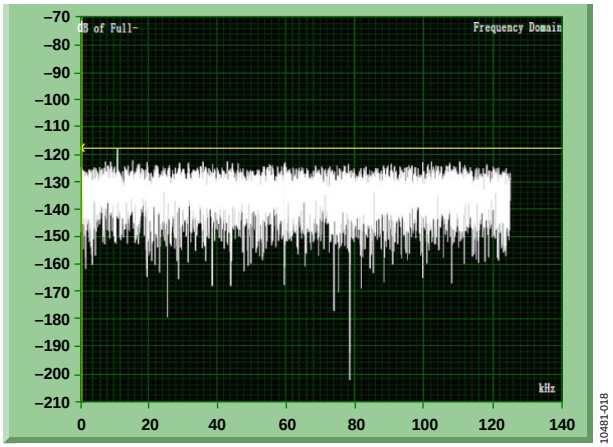


Figure 18. Spectrum for Power Supply, Configuration A

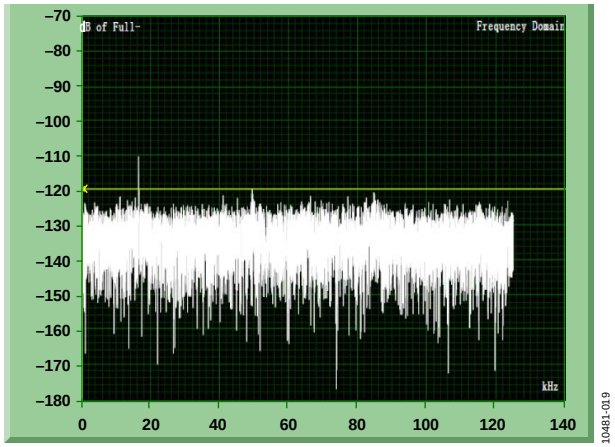


Figure 19. Spectrum for Power Supply, Configuration B

For Configuration A,
SNR = 93.40 dB
SINAD = 93.39 dB

For Configuration B,
SNR = 93.20 dB
SINAD = 93.18 dB

The impact on the noise performance of the AD7610 and AD7612 caused by the SMPS is very limited. The SNR has only about 0.1 dB to 0.2 dB variation and there is almost no change in ENOB. If an extra filter is added for the SMPS, the results should be even better.

In the AD7610 and AD7612 data sheets, the frequency response of PSRR for AVDD is specified. From the experiment results, it seems that VCC and VEE also have impressive PSRR specifications.

FILTERING CONSIDERATIONS

As a second-order filter, the LC filter provides a sharp roll-off above its resonant frequency and is widely used at the output of the dc-to-dc power supply. However, normally the performance of the switching regulator is only specified for the resistive load. If a LC filter is inserted between the dc-to-dc power supply and the resistive load, the dc-to-dc power supply sees a new complex load present at the output:

$$Z_L = \frac{R + sL + s^2LCR}{1 + sCR}$$

where s is the complex variable in Laplace transform.

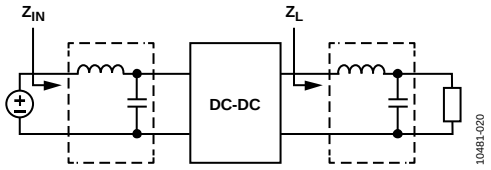


Figure 20. DC-to-DC with Input/Output LC Filters

From this point of view, as a closed-loop system, the load condition affects the dc-to-dc's loop transfer function. The bandwidth and the phase margin of the closed-loop system are altered, which may even cause stability issues. The influence of the additional filter on the dc-to-dc is complicated. As an approximation, within an appropriate range, the transient behavior of the dc-to-dc power supply with an extra LC filter is similar to the step response of a series RLC tank.

Following are some semi-experiential guidelines for choosing the LC filter, which may help to improve the stability of the design.

- Normally it's safe to set the resonant frequency of the LC filter to be higher than the original loop bandwidth of the dc-to-dc.
- If the resonant frequency had to be made lower, try to use smaller inductance and bigger capacitance (lower *Q*).

Figure 21 and Figure 22 shows the simulation results for the frequency response and the transient response of different LC filters. A group of inductance and capacitance is used, while the resonant frequency of the LC tank remains unchanged. Figure 21 and Figure 22 show the waveform of the output voltage during load-transient courses: the excessive waveform is measured before the additional LC filter; the lagging waveform is measured after the additional LC filter. With the increasing of inductance, ringing is present during the load-transient.

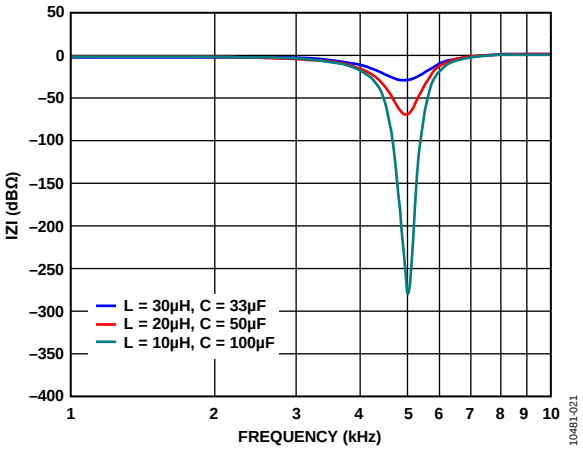


Figure 21. Frequency Response of Different LC Filters (with a Fixed Resistive Load)

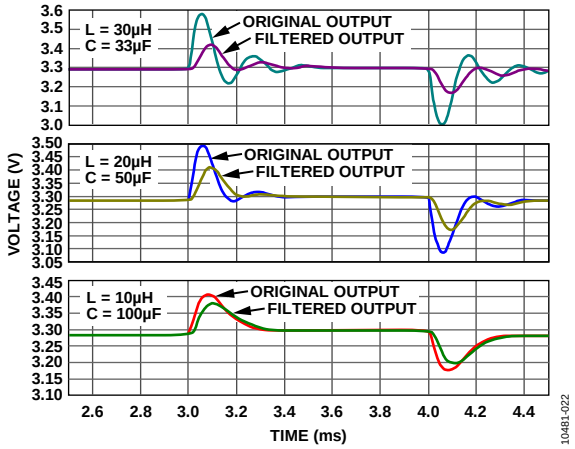


Figure 22. Transient Response of the DC-DC with Different Output LC Filters Inserted

A measured result for ADP1613 (12 V output) is shown in Figure 23. With an extra LC filter added to the output (L = 4.7 µH, C = 10 µF), the noise is greatly reduced, while the transient response doesn't change a lot, and the system is stable.

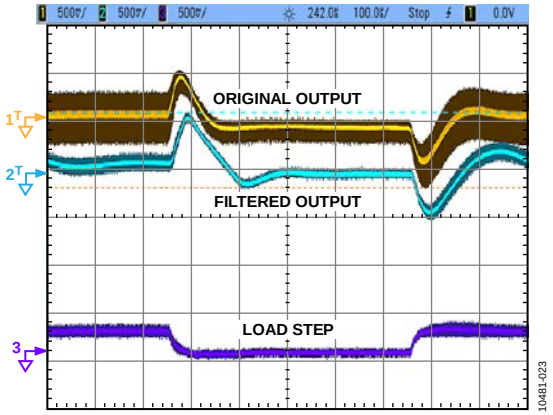


Figure 23. Transient Response of ADP1613 (12 V Output) with the Output LC Filter Inserted

CONCLUSION

The AD7610 and AD7612 have excellent power rejection performance. Their differential inputs ensure the common-mode rejection capability within a certain frequency range. When the power supply is designed for these kinds of ADCs, a switching regulator can be considered. With the help of external filtering and shielding units, the noise characters of the SMPS will be improved further. For energy-constrained applications, if the system to be powered has good noise rejection ability, coupled with the filtering and the shielding measures, use of SMPS will improve the energy efficiency but not degrade the performance of the system.

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AD7612 Data Sheet. Analog Devices, Inc. 2006.

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Kessler, Matthew C. AN-1083 Application Note. *Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 Switching Regulators*. Analog Devices, Inc.

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