Mini Tutorial
MT-230

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Noise Considerations in High Speed Converter Signal Chains

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IN THIS MINI TUTORIAL

The most common outside noise sources and how they influence the total dynamic system performance of a high speed signal chain are described as well as some analog and digital tricks that can be employed to further increase the signal-to-noise ratio (SNR) in your next design.

INTRODUCTION

Designing in high speed analog signal chains can be challenging with so many noise sources to consider. Whether the frequencies are high speed (>10 MHz) or low speed, the converter should be viewed as a high speed mixer such that all input pins, regardless of their makeup (such as analog, clock, or power), can allow noise to convolve onto the output spectrum.

Converters have a specified noise floor, which is process limited depending on what node or bias it resides in. In most cases, high speed analog-to-digital converters (ADCs) are being designed in 0.18 µCMOS, which means that the analog supply (AVDD) is +1.8 V. This trend continues to push the boundaries on the other surrounding/ support devices that drive the analog inputs and clock, and bias the converter.

Because this headroom of the converter is continuously being constrained, maintaining a very low noise spectral density of −150 dBFS/Hz and lower is challenging with each new design. This is why it is paramount that the designer recognize the importance of the surrounding noise contributions within the entire signal chain solution.

Admittedly, there are many noise principles. This tutorial addresses two of these principles: noise bandwidth and the addition of noise sources.

NOISE BANDWIDTH

Noise bandwidth is not the same as the typical −3 dB bandwidth of an amplifier or filter cutoff point. The shape for noise takes on a different form (rectangular) which specifies the total integration of the bandwidth. This means making a slight adjustment in the noise calculation when considering the noise bandwidth contribution.

For a first-order system, for example a first-order low-pass filter, the noise bandwidth is 57% larger. For a second-order system, it is 22% larger and for a third-order system, it is 15.5% larger, and so on. Use Table 1 as a quick reference when including noise bandwidth in calculations.

Table 1. Noise Bandwidth vs. System Order

System Order	Noise Bandwidth
1	1.57
2	1.22
3	1.15
4	1.13
5	1.11

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REVISION HISTORY

4/15—Rev. 0 to Rev. A

Updated Format ..... Universal
Changes to Jitter Section 6
Changes to Factoring Noise into the Signal Chain Design Section, Equation 7

3/14—Revision 0: Initial Version

NOISE SOURCES

Sources of noise come in all forms; when adding noise sources, they are uncorrelated and they resolve into a smaller unit rather than a straight summation. Therefore, a benefit to this is that the current boundaries that were once limited by a single device can now be pushed. The advantage, if it makes sense for the application, is that the sum drivers/amplifiers, converters, or both can be summed to improve the SNR dynamic range of the system.

For example, summing the outputs of four ADCs improves the SNR by 6 dB, or 1 bit. The input to each ADC consists of a signal term (V_S) and a noise term (V_N). Summing four noisy voltage sources results in a total voltage, V_T, which is the linear sum of the four signal voltages plus the RSS of the four noise voltages (see Equation 1, the total noise equation).

$$V_T = V_{S1} + V_{S2} + V_{S3} + V_{S4} + \sqrt{V_{N1}{}^2 + V_{N2}{}^2 + V_{N3}{}^2 + V_{N4}{}^2} \quad (1)$$

Because $V_{S1} = V_{S2} = V_{S3} = V_{S4}$, the signal has effectively been multiplied by four, whereas the converter noise—with equal rms values—has been multiplied by only two, thereby increasing the signal-to-noise ratio by a factor of two, or 6.02 dB. Thus, the 6.02 dB increase (delta SNR) that results from summing four like signals gives rise to one additional bit of effective resolution because SNR(dB) = 6.02 N + 1.76, where N is the number of bits. See Equation 2 for an effective resolution equation for multichannel systems.

$$N + \Delta N = \left[\frac{SNR(\text{dB})}{6.02} - \frac{1.76}{6.02}\right] + \frac{6.02\ \text{dB}}{6.02} = N + 1 \quad (2)$$

Table 2 shows the increased SNR that results from summing the outputs of multiple devices. From the standpoint of simplicity, summing four devices is an obvious choice based on area, power, and packaging. Larger numbers may also be of interest in critical cases, but that depends on other system specifications (including cost), the amount of board space available, and, of course, power consumption.

Table 2. Number of ADCs vs. SNR Increase

Number of ADCs	Increase in SNR (dB)
2	3
4	6
8	9
16	12
32	15

The ideal SNR for a 14-bit ADC is (6.02 × 14) + 1.76 = 86.04 dB. A typical 14-bit ADC data sheet specifies an SNR of 74 dB, thus, yielding an ENOB of 12 bits as shown in Equation 3.

$$ENOB = \frac{(74 - 1.76)}{6.02} = 12\ \text{bits} \quad (3)$$

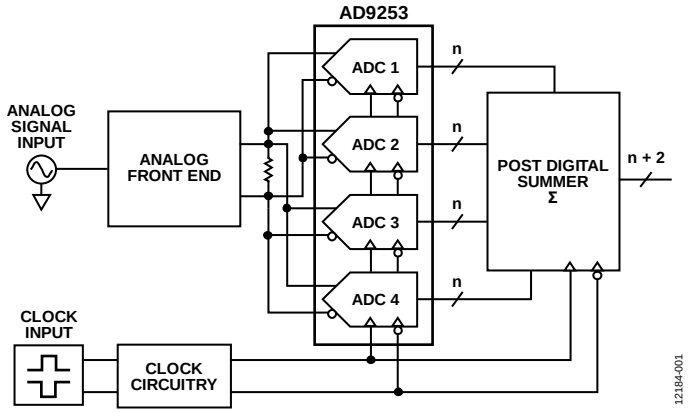

Figure 1. Basic Block Diagram of Summing Four ADCs in Parallel

Newer designs today continue to push down the core power of the ADCs thereby making both quad and octal ADCs readily available in the marketplace, such as the AD9253, 14-bit, 125 MSPS quad ADC. For multiple ADC systems, this means easier implementation and more space savings. Thus, by summing the outputs of four, 14-bit converters together, the designer can recoup one extra bit, pushing the system-level ENOB to 13 bits or 80 dB.

The same techniques can be employed for dual and quad amplifiers as well, which decreases the additive noise seen by the converter.

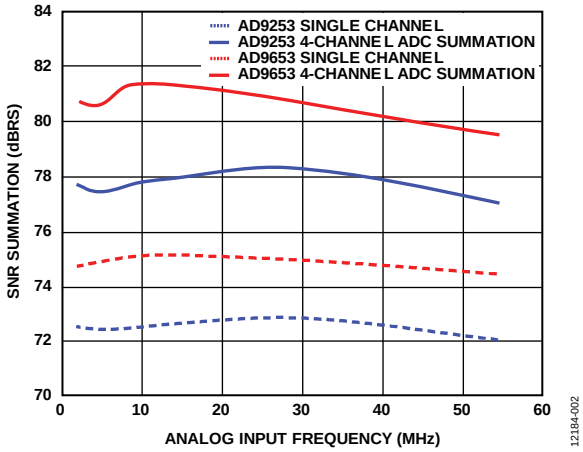

Figure 2. Summation SNR Performance vs. Frequency

NOISE CONTRIBUTIONS

Nearly every circuit component has some inherent finite amount of noise, especially if it is an active device. Resistors are little noisy heaters generating some finite amount of thermal noise. Their contribution is small, yet if the designer uses high value resistors wrapped around an amplifier to drive the converter, its noise contribution can become significant relative to the desired performance. Surround that resistor with a little gain results in even more noise.

It is important to define the resistive noise generator. This error, E_t, is represented as

$$\sqrt{(4kTR\Delta f)}$$

where:
$k = 1.38 \times 10^{-23}$ W/s/K = Boltzmann's constant.
T = 290 Kelvin.
R = resistance in ohms.
f = noise bandwidth of the system in Hertz.

For example, a 1 kΩ resistor is equal to 4 nV rms/Hz in a 1 Hz bandwidth. Use this unit of measure to quickly obtain a brief idea on scaling all the resistive noise sources in a circuit.

For example, an amplifier noise model using the AD8138 amplifier is shown in Figure 3. This shows how to sum all the resistor noise, including gain, to obtain the total output referred noise.

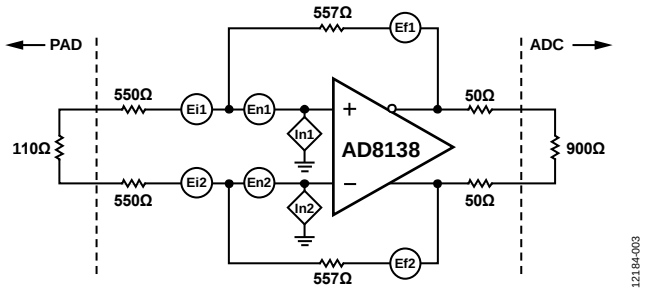

Figure 3. Amplifier Noise Model

Notice that the amplifier specifically has some voltage noise sources (En1 and En2) and some current noise sources (In1 and In2). These noise sources can be found in the amplifier data sheet specifications. Each of the resistor noise sources are also defined.

Through simple calculations, the following equations can be defined, and the total output referred (RTO) noise of the amplifier circuit shown in Figure 3 can be found.

Resistor Noise = 4 nV/√(Hz) per 1 kΩ

En, In, and noise bandwidth (NBW) are found in the AD8138 data sheet, where:

NBW = 1.57 × 3 dB BW or 320 MHz × 1.57 = 502.4 MHz

En = 5 nV/√(Hz)

In = 2 pA/√(Hz)

Ei = (550/1000) × 4 nV = 2.2nV/√(Hz)

Ef = (557/1000) × 4 nV = 2.23 nV/√(Hz)

R_{INPUT} *Voltage Noise* = *Ei* × (1 + 557/605) = 4.23 nV/√(Hz)

AD8138 Voltage Noise = *En* × (1 + 557/605) = 9.6 nV/√(Hz)

AD8138 Current Noise = (*In* × 557 || 605) × (1 + 557/605) = 1.11 nV/√(Hz)

Front-End Noise = √((*R_{INPUT} Voltage Noise*)² + (*AD8138 Voltage Noise*)² + (*AD8138 Current Noise*)² + (*Ef*)²) = √((4.23 nV² + 9.6 nV² + 1.11 nV² + 2.23 nV²)) = 10.8 nV/√(Hz)

Total Noise = √(*NBW*) × *Front-End Noise* = 241.7 µV rms

Note that amplifiers are different from op amps, simply because they include resistive elements inside them. Thus, the noise calculation is included in the overall noise contribution given in the data sheet.

This is usually referred to in the data sheet as "referred to input" (RTI) noise. By choosing the gain in the amplifier circuit, the RTI number can be used and scaled such that

RTI = 1.3 nV/√(Hz)

Gain = 16 dB

thus, RTO = $1.3 \times 10^{(16/20)}$ = 8.2 nV/√(Hz)

It is much easier to use an amplifier with integrated resistors for noise analysis.

JITTER

Clock noise or jitter affects the performance of the converter. With a basic understanding on how to factor in this noise, assuming it is broadband, then it is easy to get a sense of the degradation due to this metric.

Simply use the broadband jitter noise in seconds (preferably femtoseconds(fs) or below) and the analog input frequency or IF frequency of interest. The maximum error occurs when the clock amplitude is at its highest and assuming a sinewave input. A simple equation can be derived to get the rms voltage error. For example, a 30 MHz analog input IF and a clock jitter of 100 fs yields a broadband voltage noise of 18.8 μV or $2 \times \pi$ 30 MHz × 100 fs.

POWER SUPPLY NOISE

Exploring power supply noise requires the noise of the LDO itself and its measured band. Again, this can usually be found in the regulator data sheet. For example, a regulator can have a 225 μV of noise over a 100 kHz bandwidth. If this is known and the noise is treated as white, then this can be used to get an estimate of how this might contribute to the ADC noise performance (SNR). However, you need to know the ADC power supply rejection (PSR).

In most cases, it is −40 dB to −60 dB over the first Nyquist in the analog supply domain (AVDD). Therefore, in this case use −40 dB as the assumption for simplicity. This gives an effective noise contribution of 7.12 nV or 225 μV/√(100 kHz) × $10^{(-40/20)}$. Keep in mind this is only for one supply domain as noted. All the supply domains need to be evaluated in the same manner and each domain may have different PSR values within the ADC, amplifier, and so on.

FACTORING NOISE INTO THE SIGNAL CHAIN DESIGN

The following example helps to make the principles explored in this mini tutorial solid and further illustrates the overall dynamic performance of the entire signal chain. This example looks at the ADL5566 amplifier driving the AD9643 ADC and separate power supplies, ADP1708 and ADP1706, biasing the amplifier and converter, respectively, as shown in Figure 4.

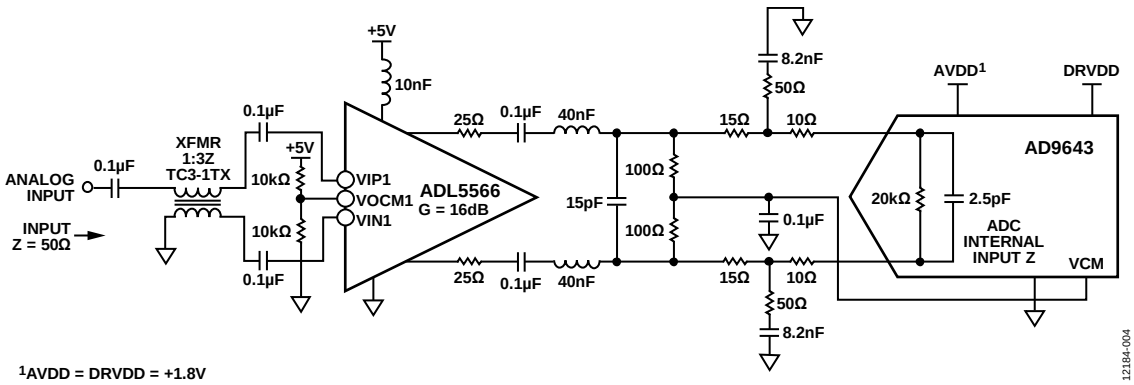

Figure 4. Example Signal Chain Block Diagram

Because a lot of the upfront work was completed in the previous sections, the next item to calculate is the ADC thermal noise.

On the AD9643, the analog input full scale is 1.75 V p-p differential, which has a data sheet SNR of 71.7 dBFS. By back-calculating the SNR equation, the following thermal noise can be found:

$$SNR = 20 \times log(Full\ Scale\ (V\ rms)/Thermal\ Noise\ (V\ rms))$$

or

$$71.7 = 20 \times log((1.75/2/\sqrt{(2)})/Thermal\ Noise\ (V\ rms))$$

or

$$Thermal\ Noise = 161\ \mu V\ rms$$

Next, determine the noise contribution of the power supplies. The example calculation shows the AVDD contribution for the ADC analog supply is 7.12 nV rms.

Do the same for the DRVDD supply of the converter and the AVDD supply of the amplifier. In these calculations, the PSRR of the DRVDD is −80 dB and the PSRR of the AVDD of the amplifier is −60 dB. Over the same band, this gives 71.2 pV rms and 1.42 nV rms noise contributions, respectively.

$$Amp\ AVDD = 450\ \mu V/\sqrt{(100\ k)} \times 10^{(-60/20)} = 1.42\ nV$$

$$ADC\ AVDD = 225\ \mu V/\sqrt{(100\ k)} \times 10^{(-40/20)} = 7.12\ nV$$

$$ADC\ DRVDD = 225\ \mu V/\sqrt{(100\ k)} \times 10^{(-80/20)} = 71.2\ pV$$

To find the total noise contribution of the supplies, simply RSS these three noise sources, which gives a total of 7.26 nV rms or $\sqrt{(7.12\ nV^2 + 71.2\ pV^2 + 1.42\ nV^2)}$.

From this amplifier example, the ADL5566 RTO noise is 8.2 nV/√(Hz) with a maximum gain of 16 dB. Next, define the amount of bandwidth. Typically, an antialiasing filter is used between the output of the amplifier and the input of the converter. Otherwise, all the broadband noise of the amplifier folds back in-band. By limiting this noise, it is assumed that the bandwidth of the filter is 150 MHz, (−3 dB point). This number is used because the AD9643 is a 250 MSPS ADC and has a Nyquist band of $f_S/2$ or 125 MHz. Typically, to capture the entire Nyquist band of interest, the AAF is designed to be somewhat larger. As shown in Figure 7, a second-order system or two-pole LC filter was used for the AAF implementation; this yields a noise bandwidth of 150 MHz × 1.22 = 183 MHz. Therefore, calculate the noise contribution of the amplifier to be 111 μV rms or 8.2 nV/√(183 MHz).

Now, simply RSS all the noise sources derived in the example using the following standard SNR equation:

$$SNR = 20 \times log(((1.75/2)/\sqrt{(2)})/\sqrt{(161\ \mu Vrms^2 + 111\ \mu Vrms^2 + 7.26\ nVrms^2 + 18.8\ \mu Vrms^2)}) = 69.96\ dB$$

This identifies the total signal dynamic range in terms of SNR. Reviewing these contributions in more detail, it can be easily understood what part of the signal chain is donating the highest contribution. Understanding these noise sources gives insight to tradeoffs in order to achieve the best performance overall given the associated devices chosen.

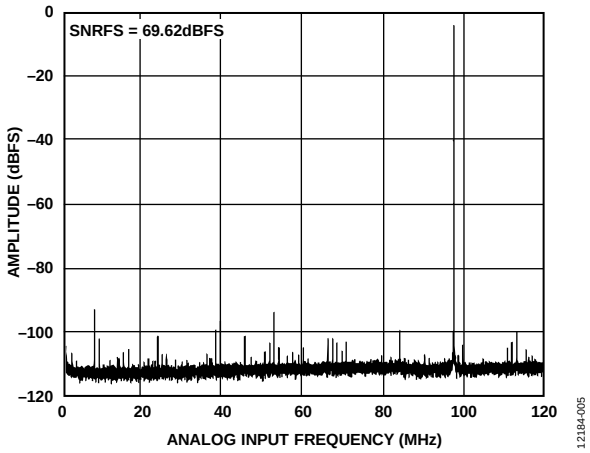

Figure 5. Measured FFT/Noise Floor Performance of the ADL5566 and AD9643

SIGNAL CHAIN DESIGN PERFORMANCE

Understanding noise tradeoffs and root causes of noise within a signal chain can lead to an easier design up front. This mini tutorial has shown how all the devices, active and passive, interact within a signal chain to closely predict the SNR dynamic range performance outcome of the entire signal chain. Keep these principles in mind when doing a signal chain design.

Acknowledgements

Thank you to David Brown and William Nguyen for their help in the lab with measurement collection.

Spreadsheet analysis is provided in Figure 6 and Figure 7 to refer to when designing. If you have further questions, connect with the applications engineering group at the EngineerZone, an online technical support community.

INPUT	
RESULT	
AMP	ADL5566
ADC	AD9643

SNR

ADC		AMP	
Number of Bits (Bits)	14	Amp Gain (Av)	6.3
ADC FullScale (Diff Vpp)	1.75	AMP BW (Hz)	4.50E+09
ADC BW (Hz)	1.00E+09	RTI (nV/√Hz)	1.3
AIN Freq (Hz)	9.00E+07	Gain (dB)	16
Sig BW (–3dB)	1.50E+08	RTO (nV/√Hz)	8.20
Noise BW (–3dB) - 1st Order	2.36E+08		
Noise BW (–3dB) - 2nd Order	1.83E+08	Ro (Ω) =	50
Noise BW (–3dB) - 3rd Order	1.73E+08	Rt1 (Ω) =	200
		Rs1 (Ω) =	30
		Rs2 (Ω) =	20
Sample Clock (Hz)	2.50E+08	Rt2 (Ω) =	100
Clock Jitter (Sec)	1.00E-13	Radc (Ω) =	2.00E+04
		Rtotal (Ω) =	1.29E+02
Ideal N-bit SNR (dBFS)	86.04		
		Total Resistor Noise (nV/√Hz)	1.43E+00
Actual ADC N-bit SNR (dBFS)	71.7		
ADC Noise Floor (V/√Hz)	1.44E-08		
ADC Noise Density (dBFS/Hz)	–152.67		
1LSB or Bit (Vrms)	3.77636E-05		
		Summary of Verrors	
		Noise - Resistor (V)	1.94E-05
		Noise - Power Supply (V)	7.26E-09
		Noise - Jitter (V)	5.65E-05
		Noise - ADC Thermal (V)	1.61E-04
		Noise - Amp (V)	1.11E-04
		SNR (dBFS)	*69.62*

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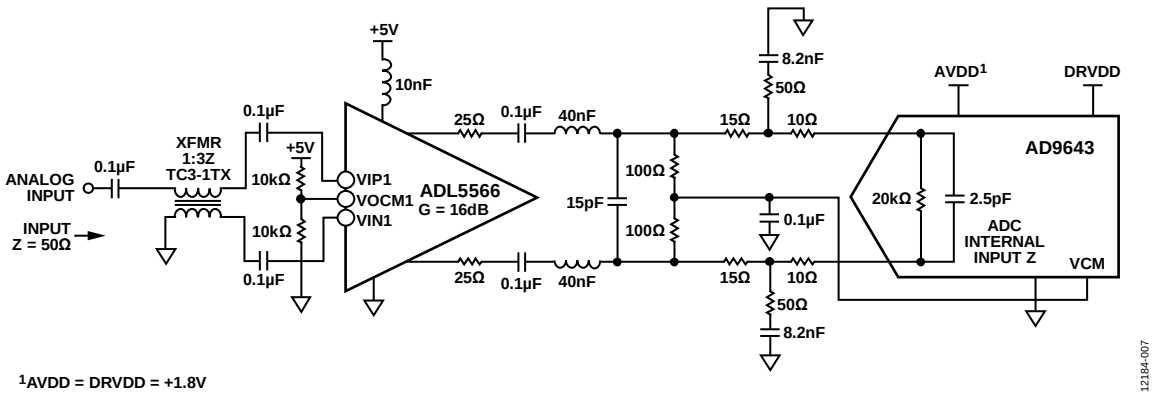
Figure 6. SNR Equations/Results

INPUT			
RESULT			
AMP-AVDD	ADC-AVDD	ADC-DRVDD	
ADP1708	ADP1706	ADP1706	

SFDR

	AMP	ADC
Freq (MHz)	100	90
SFDR, typ (dBc)	–94.7	–88
SFDR (dBc)	*–87.16*	

POWER	AMP AVDD	ADC AVDD	ADC DRVDD
AMP/ADC PSRR (dB)	–60	–40	–80
LDO Noise (nV)	4.50E-04	2.25E-04	2.25E-04
LDO Noise BW (Hz)	1.00E+05	1.00E+05	1.00E+05
Total Noise (nV/√Hz)	1.42E-06	7.12E-07	7.12E-07
Effecitve Noise (nV/√Hz)	1.42E-09	7.12E-09	7.12E-11



[1]AVDD = DRVDD = +1.8V

Figure 7. SFDR/Power Equations/Results with Signal Chain Figure

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