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XStream™ ADI-BERT: An 11.3 Gbps Bit Error Rate Tester Solution Based on ADN2915, a Continuous-Tuning Wideband Clock and Data Recovery IC

FEATURES

- Serial data input: 25.0 Mbps to 11.3 Gbps
- Designed-in reference clock
- PRBS generator—based on an ADN2915
  - Exceeds all jitter specifications required by SONET/SDH, including jitter transfer, jitter generation, and jitter tolerance
  - Frequency multiplier option (ADN2915 in lock to reference mode): allows producing up to 11.3 Gbps PRBS patterns from clocks lower than 25 MHz
- Error detector—based on a second ADN2915
  - Detects PRBS7, PRBS15, and PRBS31 patterns
  - No external components needed
- USB-to-I²C circuit allows I²C communication from a PC
- 12 V dc input, converted to ~5 V by a dc-to-dc converter, is used by five ADP1706 regulators to power all of the chips

ADI-BERT KIT CONTENTS

- ADI-BERT evaluation platform with enclosure
- CD with PRBS generator GUI, Rev. 3.1 or higher
- AC power adapter with power cord
- USB cable

ADDITIONAL EQUIPMENT NEEDED

- PC running Windows XP or higher

ONLINE RESOURCES

- Documents Needed
  - ADN2915 data sheet
  - AD9577 data sheet
  - ADI-BERT user guide
- Design and Integration Files
  - Schematics, layout files, bill of materials
- FAQs and Troubleshooting

TYPICAL SETUP

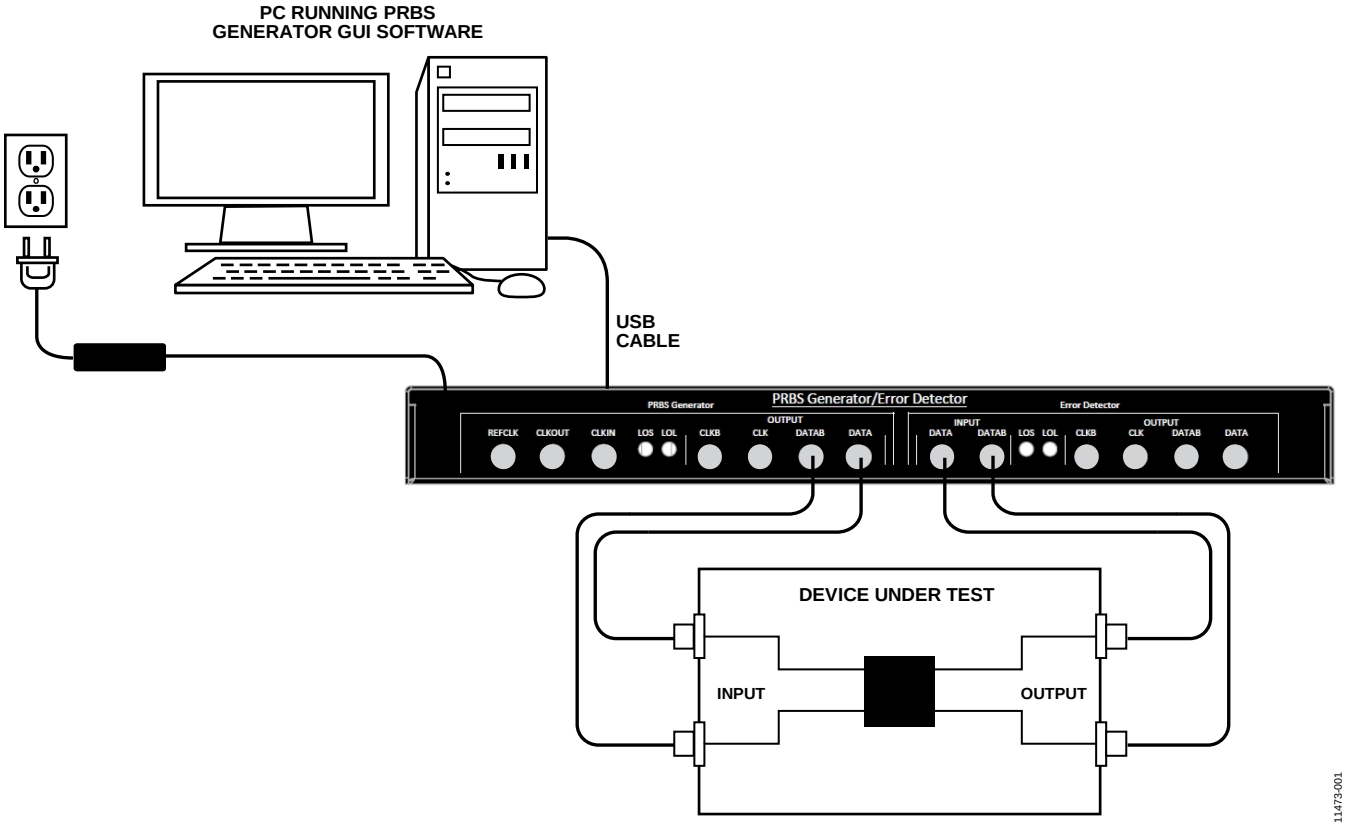

Figure 1.

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REVISION HISTORY

1/14—Rev. 0 to Rev. A

Removed Reference Circuit Terminology; Changed to ADI-BERT (Throughout) 1
Changes to Related Links 30

11/13—Revision 0: Initial Version

GENERAL DESCRIPTION

Test pattern generation and error detection are critical functions needed for design, development, and debug of systems with high speed serial interfaces. The ADI-BERT is a flexible, continuous rate pattern generator and error detector of up to 11.3 Gbps that enables test pattern generation for a wide range of industry protocols and data rates. By using this ADI-BERT, you can quickly implement a standalone system or integrate this function into an existing system with minimal hardware and software development time. The PRBS generator GUI software provides an easy to use graphical user interface.

The ADI-BERT is preferable to alternative approaches, such as implementing this function in a high end FPGA or using external lab equipment, because it provides more flexibility, is easy to use, and is cost effective. The alternative approach of implementing the function in a high end FPGA is generally constrained to a narrow range of data rates and is not particularly flexible or easy to use, and the approach of using external lab equipment is often prohibitively expensive.

The ADN2915 clock and data recovery (CDR) IC runs any rate from 10 Mbps to 11.3 Gbps. It also exceeds all jitter specifications required by SONET/SDH, including jitter transfer, jitter generation, and jitter tolerance.

For full details on the ADN2915, see the ADN2915 data sheet, which should be consulted in conjunction with this user guide when using this ADI-BERT.

Figure 2. Photograph of ADI-BERT

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

1. Copy the **prbs_gen_rcv_gui.zip** file from the included CD to a PC.
2. Unzip the **prbs_gen_rcv_gui.zip** file.
3. Navigate to the **cvidistkit.PRBSgen/Volume** directory.
4. Run the **setup.exe** file and follow the instructions to install the software.

Additional steps may be required before using certain modes and auxiliary functions. See the Modes of Operation section and the Auxiliary Buttons section for more information.

ADI-BERT SETUP PROCEDURES

Verifying the I²C Communication

When the GUI starts, an I²C communication check is performed. If the I²C communication is working properly, the application appears as in Figure 3. All of the controls are active, and the instrument is set up in its default state (see the Modes of Operation section for more information).

I²C Communication Error

If the I²C communication is not working properly, the application appears as in Figure 4. All of the controls are unavailable and are not functional except for the **Check Status** control. If this is the case,

1. Verify that the instrument is connected to power, that the USB connector is connected, and that the power switch is turned on.
2. Click **Check Status** to recheck the I²C communication.

The GUI should now appear as in Figure 3.

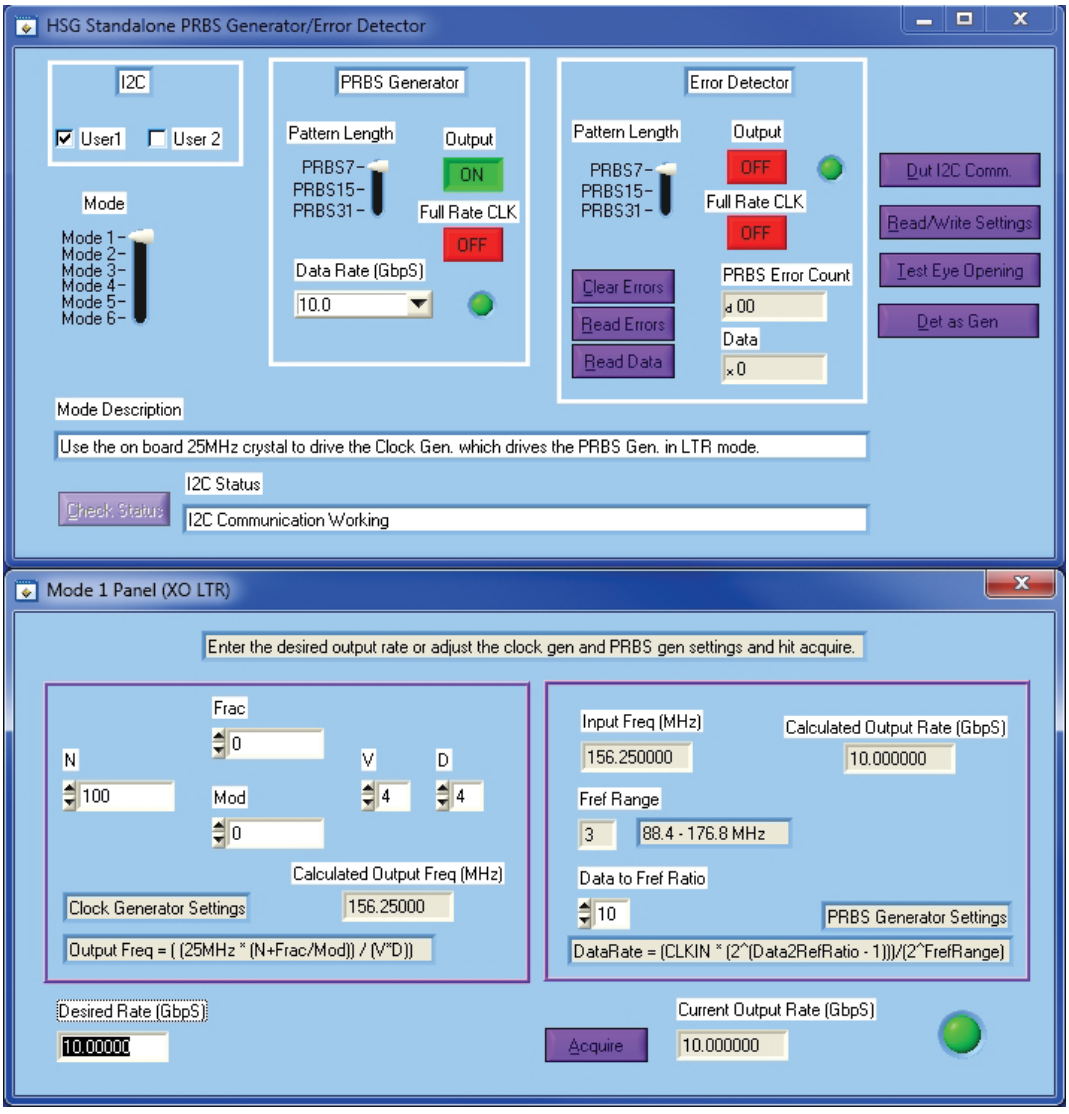


Figure 3. GUI Startup—I²C Communication Verified

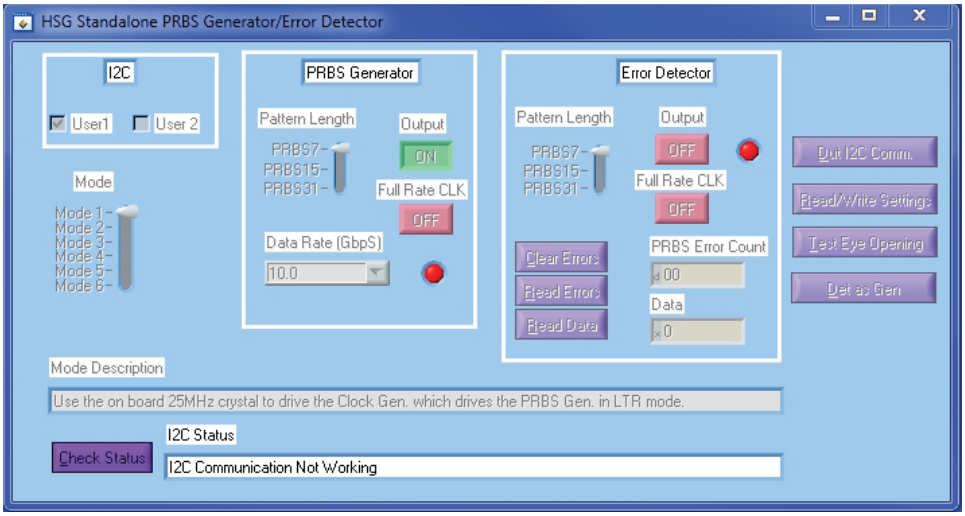


Figure 4. GUI Startup—I²C Communication Error

ADI_BERT HARDWARE

POWER SUPPLIES

The ADI-BERT comes with an ac power adapter. The power adapter converts the ac voltage of the wall outlet to 12 V dc. All of the on-board supplies are generated from this dc voltage.

ADDITIONAL FUNCTIONALITY

Auxiliary Voltage Supplies

On the back side of the PRBS generator, there are three auxiliary output voltages that can be used to power up a device under test (DUT) board. All three of the supplies are referenced to the same ground, which is connected to the black banana connection. There is a slide switch for each supply that allows setting the supply to 1.2 V, 1.8 V, 2.5 V, 3.3 V, or 5.0 V. Each of these supplies is capable of supplying 1.0 A.

I²C Communication

There are two 5-pin user I²C connections located on the back side of the PRBS generator. These connections are used to communicate with a DUT board. The connections for each 5-pin I²C connector are SDA, AGND, NC, DVCC, and SCK as you move farther away from the power switch. The pull-ups for the SDA and SCK pins are on the PRBS generator PCB and are pulled up to DVCC from the I²C connector. Each I²C connection has its own DVCC; therefore, each bus can be pulled up to a different voltage. In the case where DVCC does not come from the DUT board, there are jumpers—P5 for USER 1 and P15 for USER 2—on the PRBS generator PCB that when populated allow the corresponding bus to be pulled up to 3.3 V.

ADI-BERT CIRCUITRY

THEORY OF OPERATION

This section describes how the PRBS generator and error detector operate and briefly discusses the hardware. The ADI-BERT takes advantage of the built-in PRBS generator and error detector capabilities of the ADN2915. The ADN2915 can operate in lock to reference (LTR) or lock to data (LTD) mode.

For example, in LTD mode, a 2.5 GHz input clock is interpreted as a 5 Gbps maximum data pattern, and the CDR locks to 5.0 Gbps. The internal CDR clock subsequently clocks the PRBS generator, producing a 5.0 Gbps pattern. To produce PRBS patterns at different rates, apply a clock frequency that is half the desired output rate.

One limitation of operating in LTD mode is that you need to apply a high frequency clock to produce a high rate PRBS pattern. When operating in LTR mode, the CDR is used as a frequency multiplier, allowing high rate PRBS patterns to be produced with low frequency clocks.

In Mode 1 through Mode 4, ADI-BERT uses the AD9577 to supply the clocks needed for PRBS generation. In Mode 3 and Mode 4, an external reference clock is required. In Mode 5 and Mode 6, an external clock source is used to drive the ADN2915.

AD9577 CLOCK GENERATOR

The output of the AD9577 clock generator is at a low voltage positive emitter coupled logic (LVPECL) level. The frequency of the clock output is calculated as in Equation 1.

$$Output\ Freq = (25\ \text{MHz} \times (N + (Frac/Mod)))/(V \times D) \quad (1)$$

The AD9577 has four output clocks (OUT0 to OUT3, each of which has a positive and negative pin), but only the OUT2 output clock is used to drive the ADN2915. Because only a single-ended clock is needed, the negative pin (OUT2N) of OUT2 is available for use at the CLKOUT SMA connection on the front side of the PRBS generator. The clock output frequency is programmable and can be used in an integer-N or a fractional-N mode. With the AD9577 in integer-N mode, Frac/Mod in Equation 1 is equal to 0.

The AD9577 can be driven by a crystal oscillator (using the 25 MHz crystal oscillator on the PRBS generator PCB) or by a reference clock (using the REFCLK input on the front side of the PRBS generator). Mode 1 and Mode 2 of the PRBS generator operate with the crystal oscillator driving the AD9577, whereas Mode 3 and Mode 4 operate with the REFCLK input driving the AD9577. The frequency of the reference clock should be in the range from 19.44 MHz to 27 MHz. The accompanying GUI that drives the PRBS generator controls all of the on-board I²C settings and hardware controls.

ADN2915 PRBS GENERATOR

The ADN2915 has a built-in PRBS generator. It can be used in LTR or LTD mode. Mode 1, Mode 3, and Mode 5 of this PRBS generator operate in LTR mode; Mode 2, Mode 4, and Mode 6 operate in LTD mode.

In LTD mode, the output data rate is calculated as in Equation 2.

$$f_{DATARATE} = 2 \times CLKIN \quad (2)$$

where *CLKIN* is the frequency of the clock signal driving the ADN2915 PIN and NIN pins. This clock can come from the AD9577 or the CLKIN input on the front side of the PRBS generator.

In LTR mode, the output data rate is calculated as in Equation 3.

$$f_{DATARATE} = (CLKIN \times (2^{(Data2RefRatio - 1)}))/(2^{FrefRange}) \quad (3)$$

where *CLKIN* is the frequency of the clock signal driving the ADN2915 PIN/NIN and REFCLKP/REFCLKN pins. This clock can come from the AD9577 or the CLKIN input at the front of the PRBS generator. The frequency of CLKIN should be in the range from 11.05 MHz to 178.6 MHz.

In the case of the PRBS generator, only the PIN and REFCLKP pins are driven. The NIN and REFCLKN pins are terminated to 50 Ω. There is a high bandwidth relay that is used to switch between the CLKIN input and the AD9577. There is also a surface-mount power splitter that is used to take the single-ended output of the relay and split it to the PIN and REFCLKP pins of the ADN2915.

ADN2915 PRBS ERROR DETECTOR

The ADN2915 also has a built-in PRBS error detector. The error detector is used in LTD mode. No additional circuitry is required for its operation. All commands to operate the error detector are handled by the software.

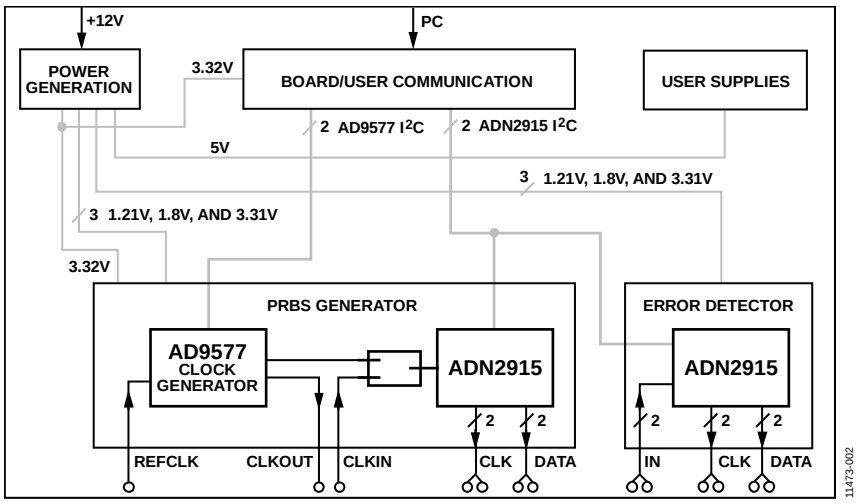


Figure 5. PRBS Generator/Error Detector Block Diagram

MODES OF OPERATION

DEFAULT SETUP

The ADI-BERT defaults to Mode 1. In this mode,

- The instrument generates a 10.0 Gbps PRBS7 pattern at the PRBS generator data outputs.
- The PRBS generator clock outputs run at 5 GHz.
- The error detector outputs are off.

QUICK REFERENCE

Table 1 and Table 2 provide a quick reference of the following for each mode of operation:

- Table 1 provides an overview of the setup.
- Table 2 shows the data rates and REFCLK input.

Mode 1 is the default power-up mode and requires no external equipment for its use. This mode allows data rates from 25 Mbps to 11.3 Gbps. Mode 2 also requires no external equipment and allows data rates from 22.4 Mbps to 1.275 Gbps. In Mode 2, the ADI-BERT output data rate is limited by the maximum output clock of the AD9577. The maximum output clock of the AD9577 is 637.5 MHz.

Mode 3 and Mode 4 are identical to Mode 1 and Mode 2, respectively, except that an external source is needed to drive the REFCLK input. The REFCLK input can be run from 19.44 MHz to 27 MHz.

Mode 5 and Mode 6 both require an external source to drive the ADN2915 inputs. The source should be connected to the CLKIN connection on the front side of the PRBS generator. Mode 5 and Mode 6 allow data rates from 25 Mbps to 11.3 Gbps. Mode 5 should be used only when a low speed clock generator is available.

Table 1. Setup for Each Mode of Operation

Mode	AD9577 Clock Input	ADN2915 Mode	ADN2915 Clock Input
1 (Default)	On-board 25 MHz crystal	Lock to reference	On-board AD9577
2	On-board 25 MHz crystal	Lock to data	On-board AD9577
3	User supplied REFCLK	Lock to reference	On-board AD9577
4	User supplied REFCLK	Lock to data	On-board AD9577
5[1]	N/A	Lock to reference	User supplied clock
6	N/A	Lock to data	User supplied clock

[1] Mode 5 should be used only when a low speed clock generator is available.

Table 2. Data Rates and REFCLK Input for Each Mode of Operation

	Data Rates		REFCLK Input (MHz)	
Mode	Min	Max	Min	Max
1 (Default)	25 Mbps	11.3 Gbps	N/A[1]	N/A[1]
2	22.4 Mbps	1.275 Gbps	N/A[1]	N/A[1]
3	25 Mbps	11.3 Gbps	19.44	27
4	22.4 Mbps	1.275 Gbps	19.44	27
5	25 Mbps	11.3 Gbps	N/A[2]	N/A[2]
6	25 Mbps	11.3 Gbps	N/A[2]	N/A[2]

[1] On-Board 25 MHz crystal oscillator is in use.
[2] No reference clock is in use.

MODE 1 OPERATION

Mode 1 involves using the on-board AD9577 clock generator to drive the ADN2915 PRBS generator in LTR mode (see Figure 6). The AD9577 is driven by the on-board crystal oscillator. The data rate being generated from the ADN2915 is calculated as in Equation 4.

$$f_{DATARATE} = (CLKIN \times (2^{(Data2RefRatio-1)}))/(2^{FrefRange}) \quad (4)$$

where *CLKIN* is the output clock from the AD9577.

The clock generator output frequency is calculated as in Equation 5.

$$Output\ Freq = (25\ \text{MHz} \times (N + (Frac/Mod)))/(V \times D) \quad (5)$$

where 25 MHz is the frequency of the crystal oscillator.

Getting Started

To use this mode,

- Select Mode 1 using the selector switch in the GUI.

Overview of Available GUI Controls

Figure 7 shows the **Mode 1 Panel (XO LTR)** window. There are controls to set **N**, **Frac**, **Mod**, **V**, and **D** of the AD9577 clock generator. There are also controls to set the **Fref Range** and **Data to Fref Ratio** of the ADN2915 PRBS generator. As these values are changed, the values of the **Calculated Output Rate (GbpS)** and **Desired Rate (GbpS)** boxes are updated. It is important to note, however, that when changing these values, the output rate does not change until **Acquire** is clicked. The data rate being generated is displayed in the **Current Output Rate (GbpS)** box.

Another way to change the data rate is to type the rate in the **Desired Rate (GbpS)** box and then press ENTER. Because only one side of the differential clock being generated by the AD9577 is used by the PRBS generator, the other side of the differential clock is available for use at the CLKOUT connection on the front side of the PRBS generator.

In the **Mode 1 Panel (XO LTR)** window, there is also an LED indicator located in the lower right corner of the window that is green when the output is available and red when the internal settings are being set.

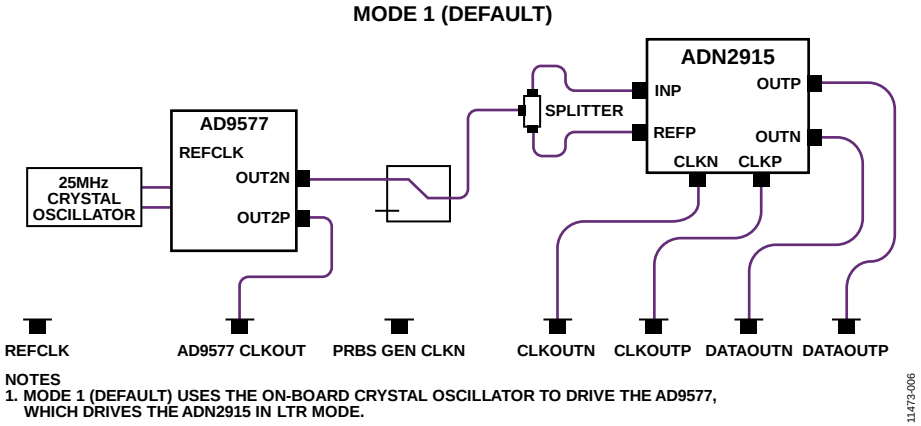


Figure 6. Mode 1 Block Diagram

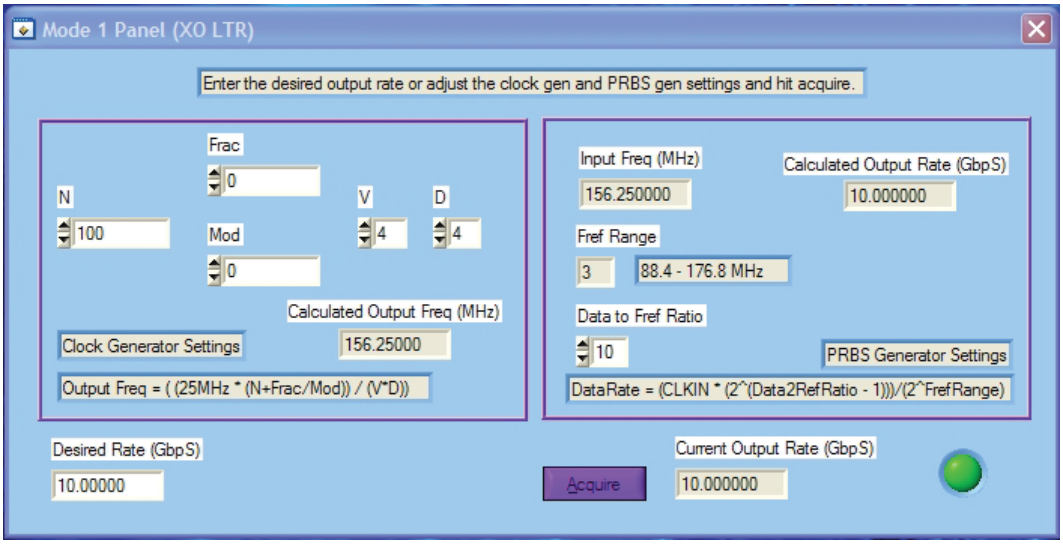


Figure 7. Mode 1 Panel (XO LTR) Window

MODE 2 OPERATION

Mode 2 involves using the on-board AD9577 clock generator to drive the ADN2915 PRBS generator in LTD mode (see Figure 8). The AD9577 is driven by the on-board crystal oscillator. The data rate being generated from the ADN2915 is calculated as in Equation 6.

$$f_{DATARATE} = 2 \times ((25\ \text{MHz} \times (N + (Frac/Mod))/(V \times D)) \quad (6)$$

where 25 MHz is the frequency of the crystal oscillator.

Getting Started

To use this mode,

- Select Mode 2 using the selector switch in the GUI.

Overview of Available GUI Controls

Figure 9 shows the **Mode 2 Panel (XO LTD)** window. There are controls to set **N**, **Frac**, **Mod**, **V**, and **D** of the AD9577 clock generator. As these values are changed, the values of the **Calculated Output Rate (GbpS)** and **Desired Rate (GbpS)** boxes are updated. It is important to note, however, that when changing these values, the output rate does not change until **Acquire** is clicked. The data rate being generated is displayed in the **Current Output Rate (GbpS)** box.

Another way to change the data rate is to type the rate in the **Desired Rate (GbpS)** box and then press ENTER. Because only one side of the differential clock being generated by the AD9577 is used by the PRBS generator, the other side of the differential clock is available for use at the CLKOUT connection on the front side of the PRBS generator.

In the **Mode 2 Panel (XO LTD)** window, there is also an LED indicator located in the lower right corner of the window that is green when the output is available and red when the internal settings are being set.

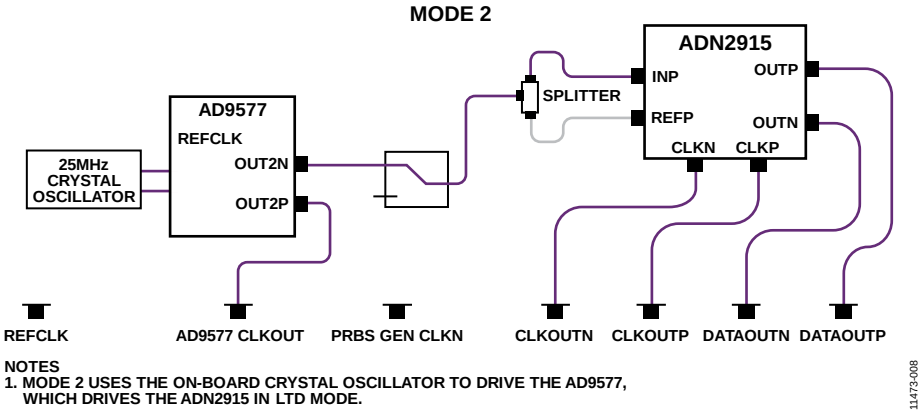


Figure 8. Mode 2 Block Diagram

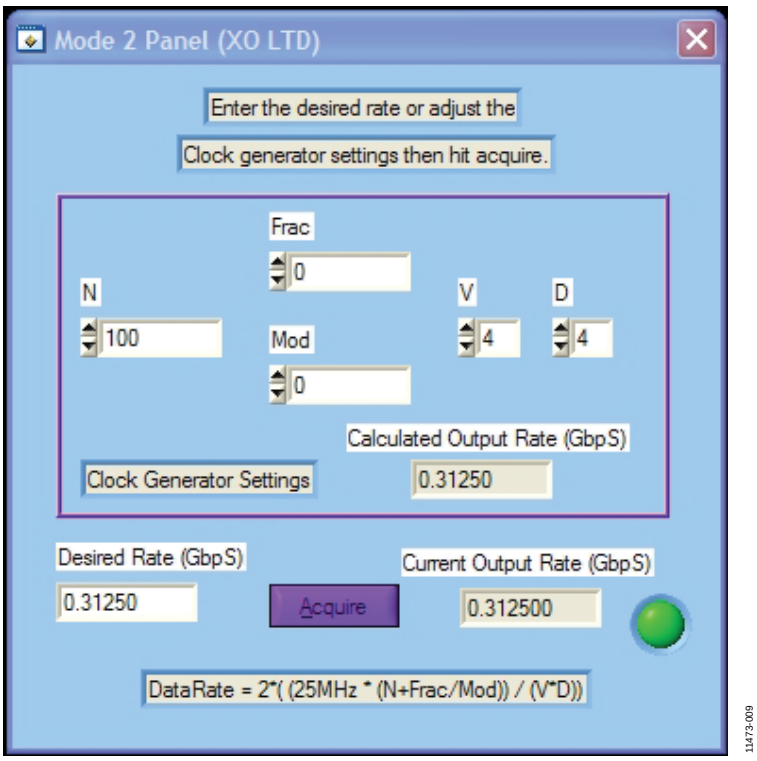


Figure 9. Mode 2 Panel (XO LTD) Window

MODE 3 OPERATION

Mode 3 involves using the on-board AD9577 clock generator to drive the ADN2915 PRBS generator in LTR mode (see Figure 10). The AD9577 is driven by the REFCLK signal from the REFCLK input on the front side of the PRBS generator. It is recommended to use a 200 mV p-p input signal. The data rate being generated from the ADN2915 is calculated as in Equation 4, where CLKIN is the output clock from the AD9577.

The clock generator output frequency is calculated as in Equation 7.

$$Output\ Freq = (REFCLK \times (N + (Frac/Mod)))/(V \times D) \quad (7)$$

where *REFCLK* is the frequency of the input signal at the REFCLK connection on the front side of the PRBS generator.

Getting Started

To use this mode,

- Select Mode 3 using the selector switch in the GUI.
- A user supplied reference clock must be applied to the AD9577 input.
- The frequency of the user supplied reference clock must be entered in the **REFCLK Freq (MHz)** box.

Overview of Available GUI Controls

Figure 11 shows the **Mode 3 Panel (REFCLK LTR)** window. There are controls to set **N**, **Frac**, **Mod**, **V**, and **D** of the AD9577 clock generator. There are also controls to set the **Fref Range** and **Data to Fref Ratio** of the ADN2915 PRBS generator. As these values are changed, the values of the **Calculated Output Rate (GbpS)** and **Desired Rate (GbpS)** boxes are updated. It is important to note, however, that when changing these values, the output rate does not change until **Acquire** is clicked. The data rate being generated is displayed in the **Current Output Rate (GbpS)** box. Note that to attain accurate calculations, you must enter the frequency of the user supplied reference clock in the **REFCLK Freq (MHz)** box.

Another way to change the data rate is to type the rate in the **Desired Rate (GbpS)** box and then press ENTER. When any of the settings are changed, the **Current Output Rate (GbpS)** box vanishes until **Acquire** is clicked again. Because only one side of the differential clock being generated by the AD9577 is used by the PRBS generator, the other side of the differential clock is available for use at the CLKOUT connection on the front side of the PRBS generator.

In the **Mode 3 Panel (REFCLK LTR)** window, there is also an LED indicator located in the lower right corner of the window that is green when the output is available and red when the internal settings are being set.

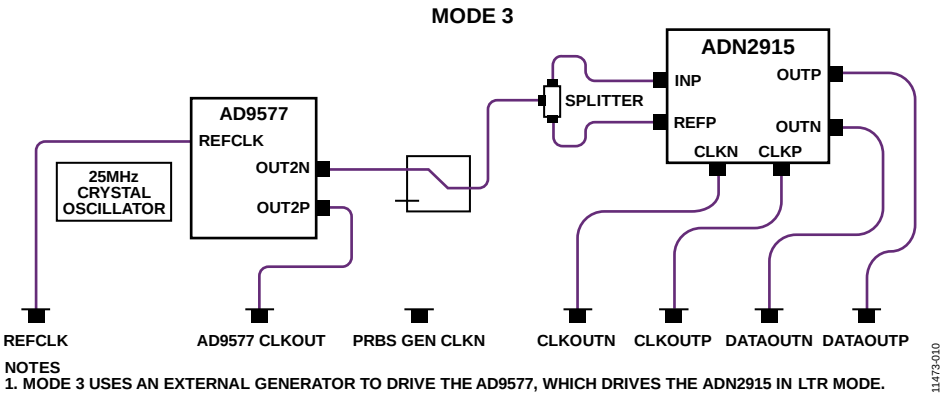


Figure 10. Mode 3 Block Diagram

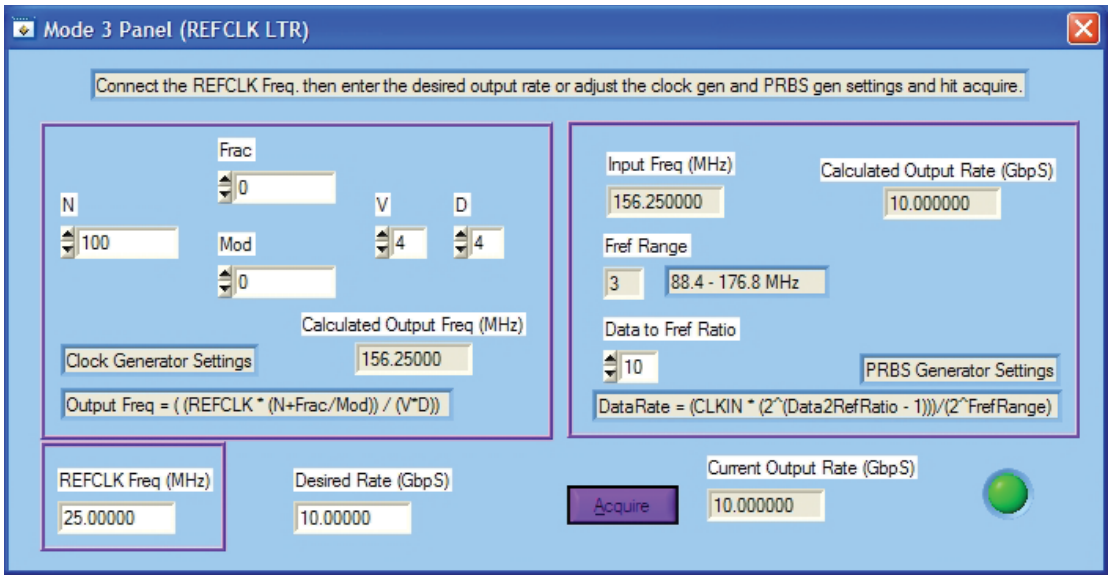


Figure 11. Mode 3 Panel (REFCLK LTR) Window

MODE 4 OPERATION

Mode 4 involves using the on-board AD9577 clock generator to drive the ADN2915 PRBS generator in LTD mode (see Figure 12). The AD9577 is driven by the REFCLK signal from the REFCLK input on the front side of the PRBS generator. It is recommended to use a 200 mV p-p input signal. The data rate being generated from the ADN2915 is calculated as in Equation 8.

$$f_{DATARATE} = 2 \times ((REFCLK \times (N + (Frac/Mod))/(V \times D)) \quad (8)$$

where *REFCLK* is the frequency of the input signal at the REFCLK connection on the front side of the PRBS generator.

Getting Started

To use this mode,

- Select Mode 4 using the selector switch in the GUI.
- A user supplied reference clock must be applied to the AD9577 input.
- The frequency of the user supplied reference clock must be entered in the **REFCLK Freq (MHz)** box.

Overview of Available GUI Controls

Figure 13 shows the **Mode 4 Panel (REFCLK LTD)** window. There are controls to set **N**, **Frac**, **Mod**, **V**, and **D** of the AD9577 clock generator. As these values are changed, the value of the **Calculated Output Rate (GbpS)** box is updated. It is important to note, however, that when changing these values, the output rate does not change until **Acquire** is clicked. The data rate being generated is displayed in the **Current Output Rate (GbpS)** box. Note that to attain accurate calculations, you must enter the frequency of the user supplied reference clock in the **REFCLK Freq (MHz)** box.

When any of the settings are changed, the **Current Output Rate (GbpS)** box vanishes until **Acquire** is clicked again. Because only one side of the differential clock being generated by the AD9577 is used by the PRBS generator, the other side of the differential clock is available for use at the CLKOUT connection on the front side of the PRBS generator.

In the **Mode 4 Panel (REFCLK LTD)** window, there is also an LED indicator located in the lower right corner of the window that is green when the output is available and red when the internal settings are being set.

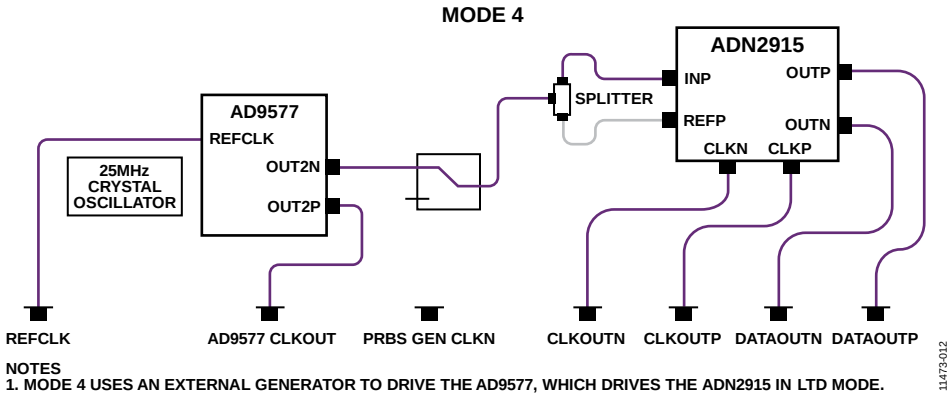


Figure 12. Mode 4 Block Diagram

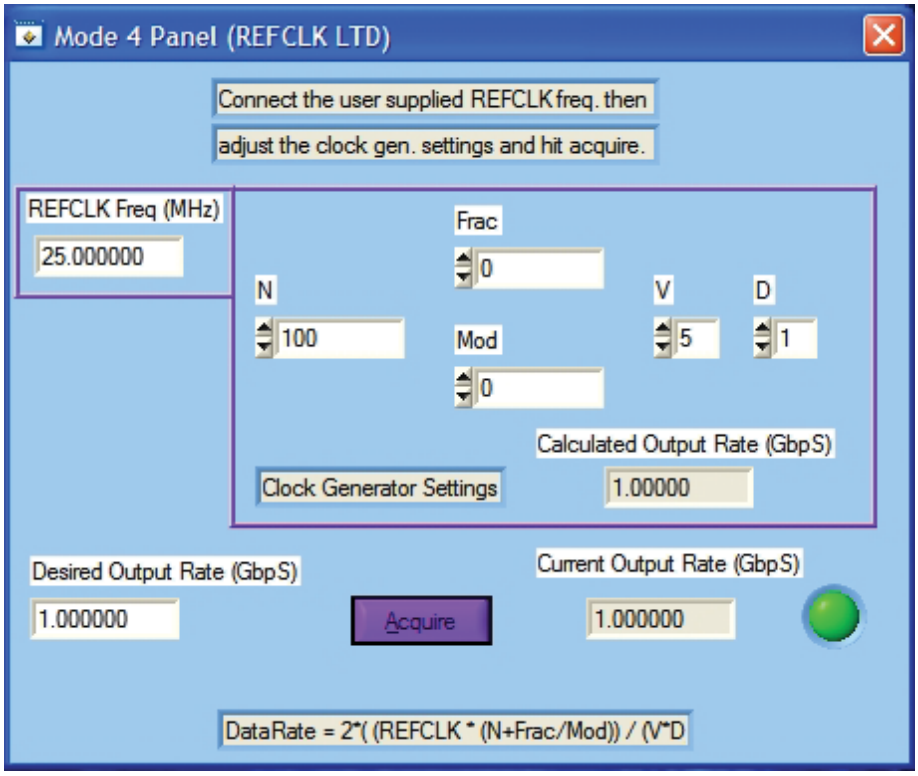


Figure 13. Mode 4 Panel (REFCLK LTD) Window

MODE 5 OPERATION

Mode 5 involves using an external generator to drive the ADN2915 PRBS generator in LTR mode (see Figure 14). The input to the ADN2915 has a limiting amplifier stage and a sensitivity of 10 mV p-p. There is a relay and a power splitter in the path to the ADN2915 input; therefore, it is recommended to use a signal in the 50 mV p-p to 300 mV p-p range. The data rate being generated from the ADN2915 is calculated as in Equation 9.

$$f_{DATARATE} = (CLKIN \times (2^{(Data2RefRatio-1)}))/(2^{FrefRange}) \quad (9)$$

where *CLKIN* is the frequency of the input signal at the CLKIN connection on the front side of the PRBS generator.

Getting Started

This mode should be used only when a low speed clock generator is available. To use this mode,

- Select Mode 5 using the selector switch in the GUI.
- A user supplied clock must be applied to the ADN2915 input.
- The frequency of the user supplied clock must be entered in the **User Supplied Freq (MHz)** box.

Overview of Available GUI Controls

Figure 15 shows the **Mode 5 Panel (CLKIN LTR)** window. There are controls to set the **Fref Range** and **Data to Fref Ratio** of the ADN2915 PRBS generator. As these values are changed, the value of the **Desired Output Rate (GbpS)** box is updated. It is important to note, however, that when changing these values, the output rate does not change until **Acquire** is clicked. The data rate being generated is displayed in the **Current Output Rate (GbpS)** box. Note that to attain accurate calculations, you must enter the frequency of the user supplied input clock in the **User Supplied Freq (MHz)** box.

In the **Mode 5 Panel (CLKIN LTR)** window, there is also an LED indicator located in the lower right corner of the window that is green when the output is available and red when the internal settings are being set.

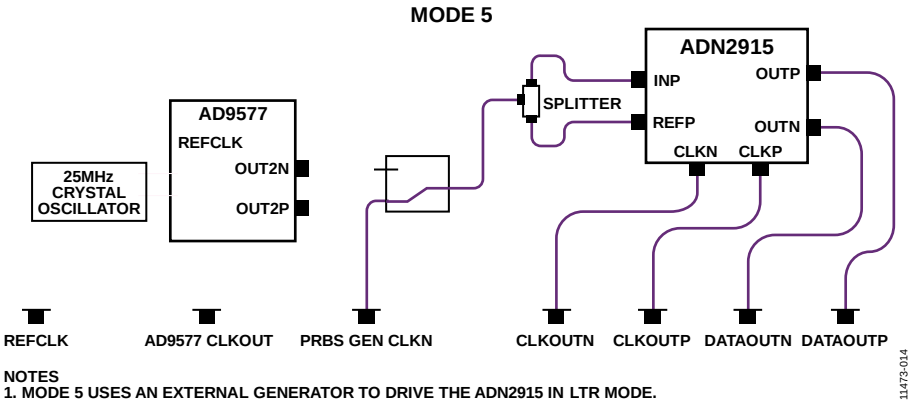


Figure 14. Mode 5 Block Diagram

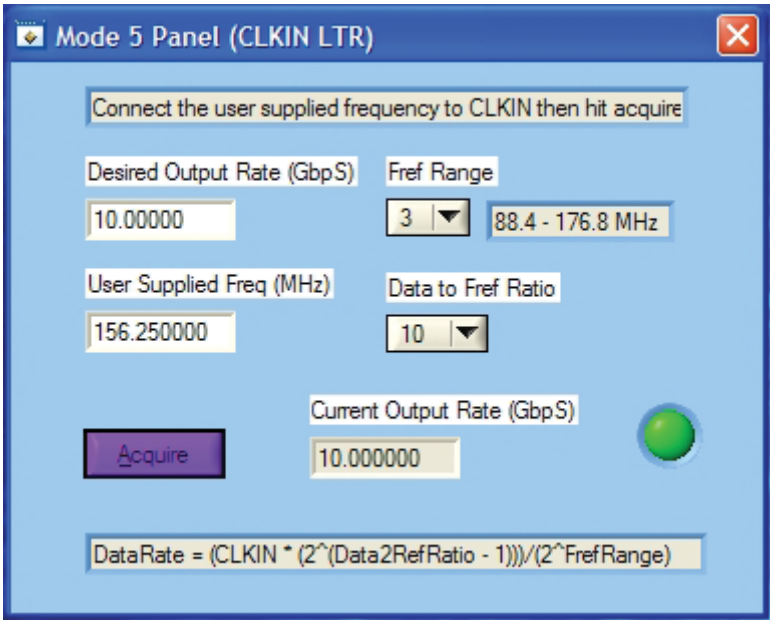


Figure 15. Mode 5 Panel (CLKIN LTR) Window

MODE 6 OPERATION

Mode 6 involves using an external generator to drive the ADN2915 PRBS generator in LTD mode (see Figure 16). As in Mode 5, in Mode 6 the input to the ADN2915 has a limiting amplifier stage and a sensitivity of 10 mV p-p. There is a relay and a power splitter in the path to the ADN2915 input; therefore, it is recommended to use a signal in the 50 mV p-p to 300 mV p-p range. The data rate being generated from the ADN2915 is calculated as in Equation 10.

$$f_{DATARATE} = 2 \times CLKIN \quad (10)$$

where *CLKIN* is the frequency of the input signal at the CLKIN connection on the front side of the PRBS generator.

Getting Started

To use this mode,

- Select Mode 6 using the selector switch in the GUI.
- A user supplied clock must be applied to the ADN2915 input.
- The needed data rate must be entered in the **Desired Output Rate (GbpS)** box, and then the required signal must be connected to the CLKIN input on the front side of the PRBS generator.

Overview of Available GUI Controls

Figure 17 shows the **Mode 6 Panel (CLKIN LTD)** window. Clicking **Acquire** causes the ADN2915 to initiate a new acquisition. After **Acquire** is clicked, the data rate changes as the frequency of the applied clock is changed.

In the **Mode 6 Panel (CLKIN LTD)** window, there is also an LED indicator located toward the right of the window that is green when the output is available and red when an acquisition is being performed.

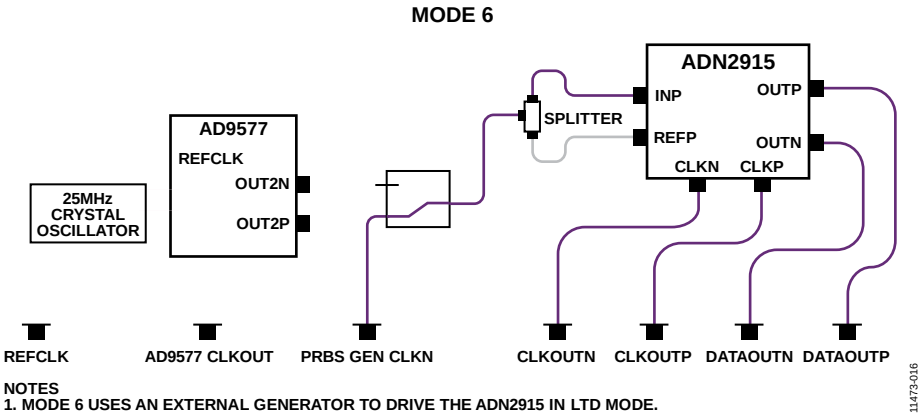


Figure 16. Mode 6 Block Diagram

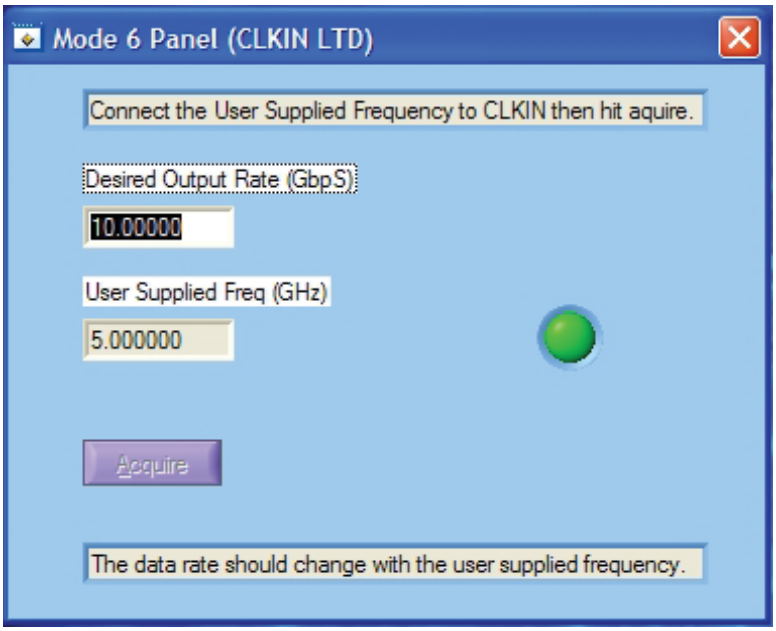


Figure 17. Mode 6 Panel (CLKIN LTD) Window

HOW TO USE THE SOFTWARE

STARTING THE SOFTWARE

After the PRBS generator GUI software is installed on a PC, a shortcut is created on the desktop. Double-click the shortcut to start the ADI-BERT graphical user interface (see Figure 18).

OVERVIEW OF THE MAIN WINDOW

The main window of the software is shown in Figure 18 and has the features described in this section.

User I²C

There are two 5-pin user I²C connections on the back side of the PRBS generator. The connections are labeled USER 1 and USER 2. One or both of these I²C buses can be used by selecting the appropriate check box in the main window (see Figure 18). These buses can be used to connect to an external DUT or evaluation board.

Mode Switch

The PRBS generator can be used in six modes. The mode can be selected by using the **Mode** slider in the main window.

PRBS Generator

The pattern length of the signal being generated is selected by using the **Pattern Length** slider in the main window. You can select a PRBS7, PRBS15, or PRBS31 pattern using this slider. There is also a push-button control, labeled **Output**, to turn the PRBS generator outputs on or off in the **PRBS Generator** section of the main window. A second push-button control, labeled **Full Rate CLK**, in the **PRBS Generator** section of the main window controls whether the output clock is full or half rate. However, when the data rate is greater than ~5.5 Gbps, the output clock is always half rate, even if **Full Rate CLK** is in the on position. There is a list of 21 predefined data rates that can be selected from the **Data Rate (GbpS)** pull-down menu. These rates are listed in Table 3 and are only available when ADI-BERT is in Mode 1. There is also an LED indicator in the **PRBS Generator** section of the main window that is green when the output is available and red when the internal settings are being set.

Table 3. Available Predefined Rates (Mode 1 Only)

Data Rate (Gbps)	Protocol
11.3	10xFC FEC
11.1	CEI 11G
11.095	10G Base-KR FEC
10.709	OTU2
10.52	10xFC
10.3125	10G Base-KR
10.0	Infiniband QDR
9.95328	OC-192/STM-64
9.953	CEI 11G
9.1	8xFC FEC
8.5	PCIe Gen 3
6.25	RXAUI
5.0	Infiniband DDR
4.25	4xFC
3.125	XAUI
2.5	PCIe Gen 1/Infiniband SDR
2.48832	OC-48/STM-16
2.125	2xFC
1.25	Gigabit Ethernet
1.0625	1xFC
0.62208	OC-12/STM-4

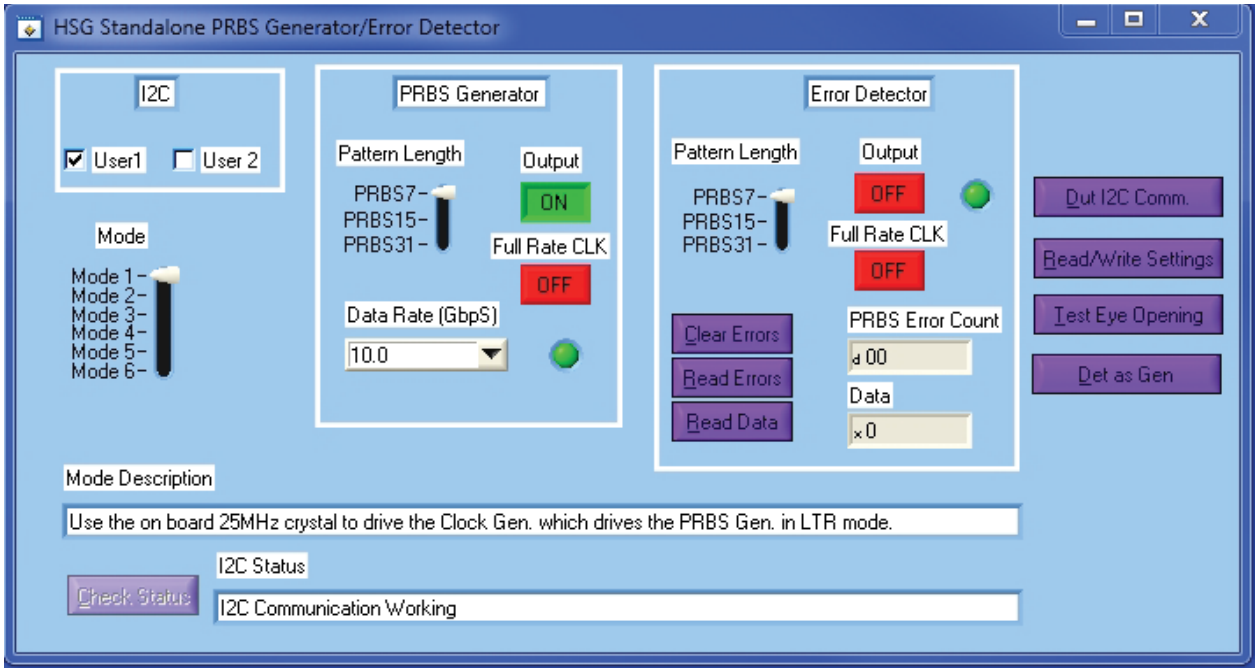


Figure 18. Main Window

Error Detector

The pattern length of the data input signal is selected by using the **Pattern Length** slider in the main window. You can select a PRBS7, PRBS15, or PRBS31 pattern using this slider. There is also a push-button control, labeled **Output**, to turn the error detector outputs on or off in the **Error Detector** section of the main window. A second push-button control, labeled **Full Rate CLK**, in the **Error Detector** section of the main window controls whether the error detector output clock is full or half rate. However, when the data rate is greater than ~5.5 Gbps, the output clock is always half rate, even if **Full Rate CLK** is in the on position.

There are three additional push-button controls in the **Error Detector** section: **Clear Errors**, **Read Errors**, and **Read Data**. Clicking **Clear Errors** resets the internal error count to 0. Clicking **Read Errors** reads the internal error count and displays the number of errors in the **PRBS Error Count** box. Because the error count register of the ADN2915 is only an 8-bit register, the maximum error count is 255. Click **Read Data** to read the last 32 data bits and display the resulting data in the **Data** box. There is also an LED indicator in the **Error Detector** section of the main window that is green when the error detector is available. Because the ADN2915 acts as a CDR when in error detection mode, three outputs—CLK, DATAB, and DATA—are available on the front side of the error detector that allow boosting a signal using the limiting amplifier capability of the ADN2915.

Auxiliary Buttons

There are four auxiliary function buttons: **Dut I2C Comm.**, **Read/Write Settings**, **Test Eye Opening**, and **Det as Gen**.

DUT I²C Communication

Figure 19 shows the **Dut I2C Communication** window. This window works in conjunction with the **User 1** and **User 2** check boxes in the **I2C** section of the main window in Figure 18. When the **Dut I2C Communication** window is first opened, the **Reading File** indicator and **I2C Communication Failed!!!!** warning are not visible. For this window to function properly, the DUT board must be connected to one of the user I²C connections (USER 1 or USER 2) located on the back side of the PRBS generator and the correct DUT address must be entered in the **Dut Address** box. The DUT address should be the 7-bit address shifted to the left by one bit. This allows for the LSB to be set for a read or write operation. When **Write** is clicked, the **Dut Address**, **Reg. Address**, and **Write Data boxes** are read by the software and then written to the DUT. When **Read** is clicked, the **Dut Address** and **Reg. Address** boxes are read by the software, and then an I²C read is performed on the DUT. The result of the read operation is displayed in the **Read Data** box. If an error occurs while performing a read or write, the **I2C Communication Failed!!!!** warning is displayed (see Figure 19).

Click **Import DUT Settings** to read a file of predetermined settings and then write it to the DUT. The file format is a list of register addresses and data separated by commas as in the following example:

```
RegAddr1,Data1
RegAddr2,Data2
RegAddr3,Data3
...
RegAddrN,DataN
```

The values should be in hexadecimal format without the leading 0x. The file should contain no more than 256 RegAddr,Data pairs. To use this feature, create a directory named **PRBSGEN_Files** on the C: drive to store the files. The **Reading File** indicator is displayed while the file is being read.

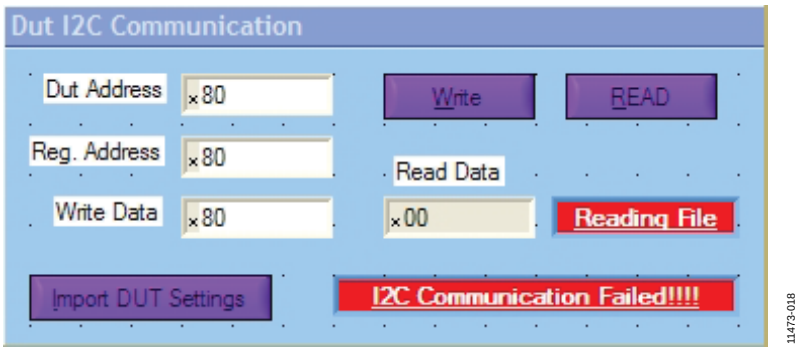


Figure 19. Dut I2C Communication Window

Read/Write Settings

When **Read/Write Settings** is clicked, the **File I/O** window is displayed (see Figure 20). This window can be used to create and recall setup files. This window can be used only in Mode 1. When the settings in this window are changed, there is no change to the current PRBS generator settings. When the desired output rate is found, the settings can be saved by clicking **Export Settings**. The settings can be read back to set up the PRBS generator by clicking **Import Settings** and browsing for the correct setup file. To use this function, create a directory called **PRBSGEN_Files** on the C: drive.

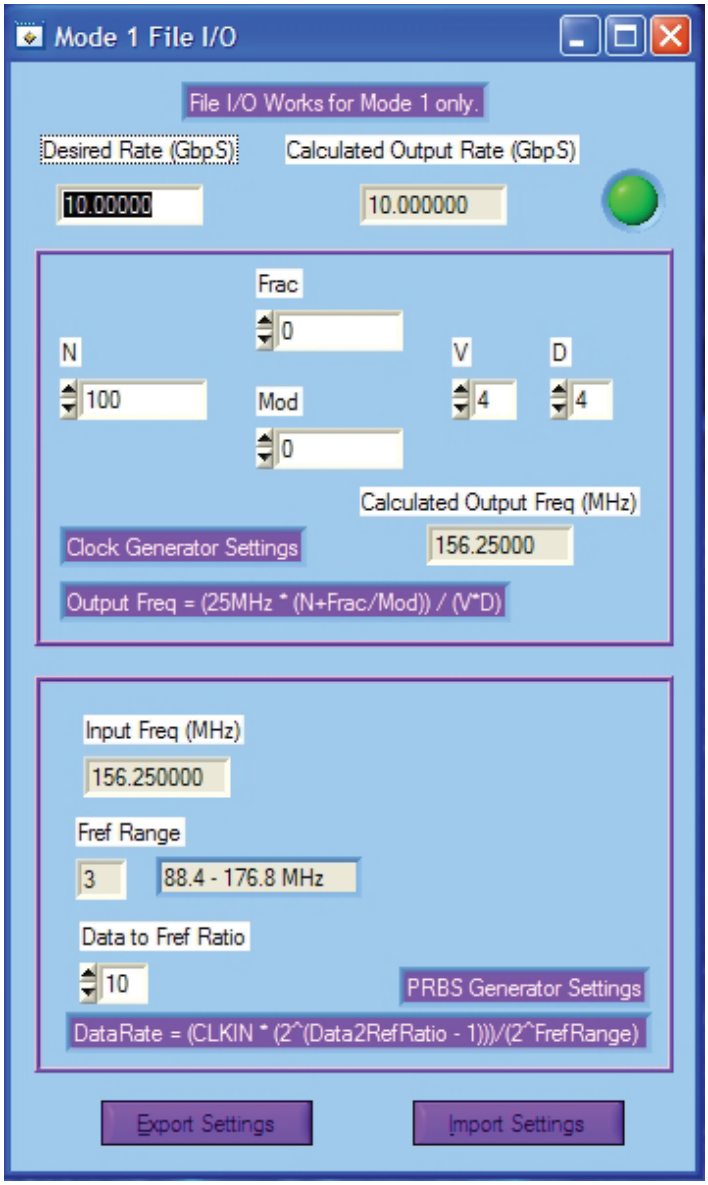


Figure 20. Mode 1 File I/O Window

Eye Opening Test

Clicking **Test Eye Opening** opens the **Sample Phase Adjust** window. The purpose of this window is to check how open the data eye is, and this is accomplished by adjusting the phase of the sampling instant. As the sampling phase is moved farther from the center of the eye, the error detector might start to detect errors. It is possible, however, to adjust the sampling phase to its extremes and still not detect any errors. In this case, the input data has plenty of margin. The phase of the sampling instant can be adjusted on the error detector from −0.25 UI to +0.22 UI in 1/32th unit interval steps.

To perform an eye opening test,

1. Enter the duration of the bit error count in the **Bit Error Count Delay** box.
2. Click **Run**.

A canned routine then goes through all of the sample phase settings and measures the bit error count for each. When the routine is finished, a chart is displayed showing the error count for each setting. Ideally, the bit error count should be low toward the center of the chart and increase to the end points.

The eye opening test function works only when the error detector is locked and the input rate is ≥5.65 Gbps. A **NOT LOCKED** message is shown on the window if **Run** is clicked and the error detector is not locked (see Figure 21).

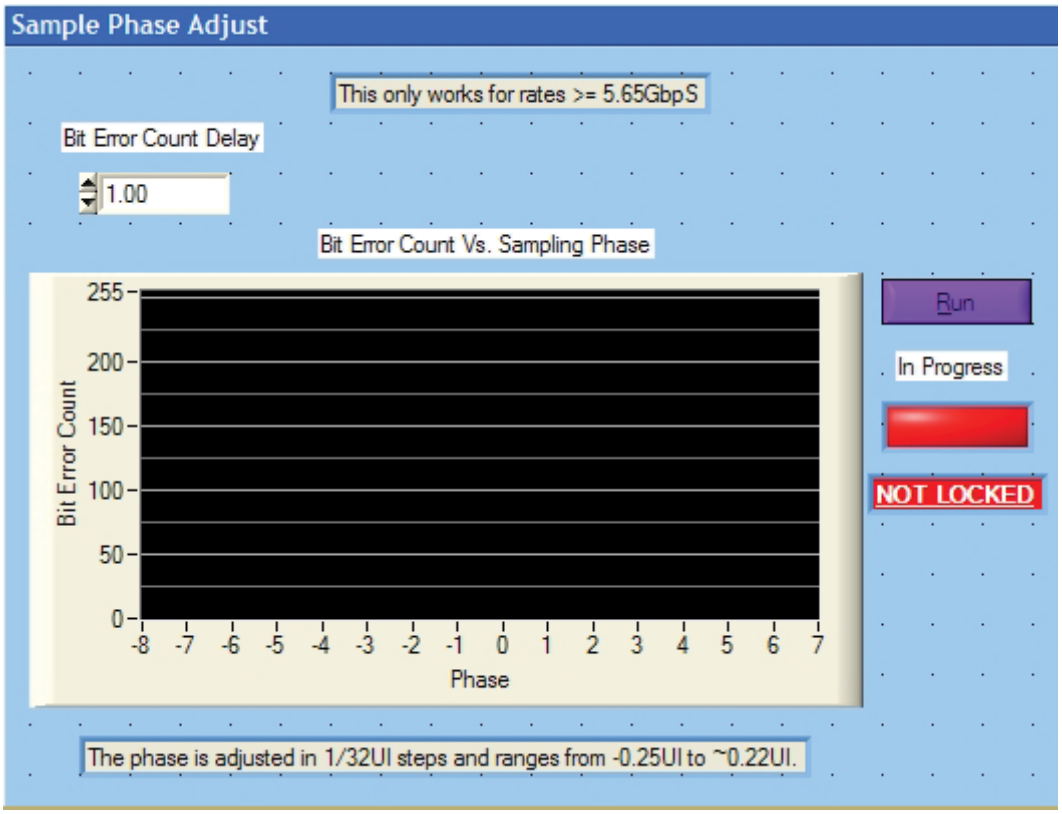


Figure 21. Sample Phase Adjust Window (for Eye Opening Test)

Det as Gen

When **Det as Gen** is clicked, the window in Figure 22 is displayed and the error detector controls in the main window become unavailable (see Figure 23).

When using this function, the software sets up the ADN2915 used for the error detector into the LTD mode so that the second ADN2915 also functions as a PRBS generator, similar to Mode 6 of the PRBS generator. The data rate being generated from the ADN2915 is calculated as in Equation 10, where CLKIN is the frequency of the input signal at the CLKIN connection on the front side of the PRBS generator. A signal is generated only if the input clock is applied. The data rate changes as the frequency of the applied clock is changed. When exiting the **Detector as Generator** window, the error detector is reset to its default state.

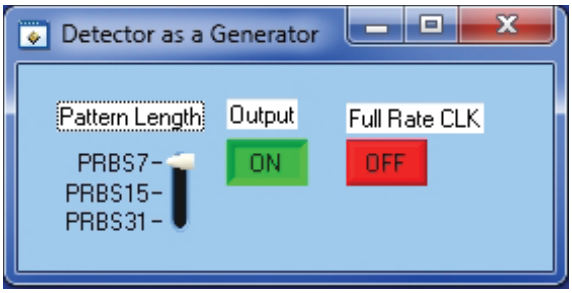


Figure 22. Detector as Generator Window

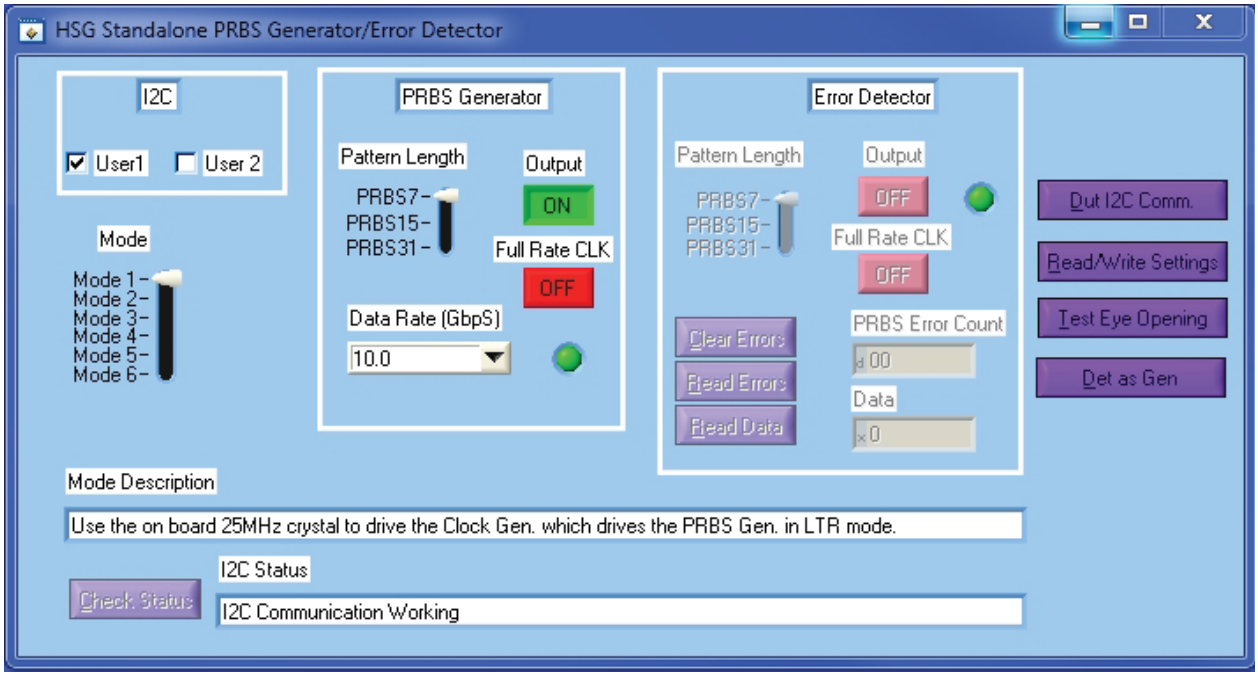


Figure 23. Main Window After Clicking Det as Gen (Error Detector Unavailable)

EVALUATION AND TEST

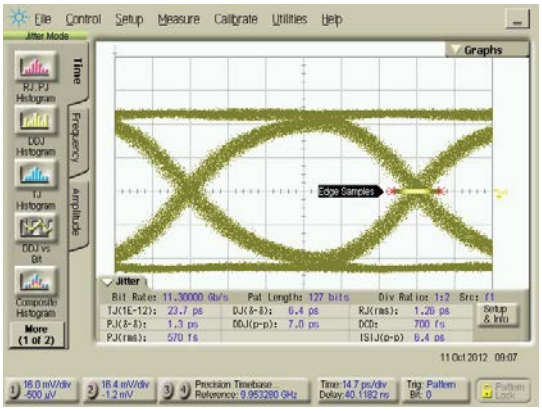
EQUIPMENT LIST

- ADI-BERT
- PC running the PRBS generator GUI
- Two SMA cables of matched length with >18 GHz bandwidth
- AC power adapter
- USB cable

TEST PROCEDURES

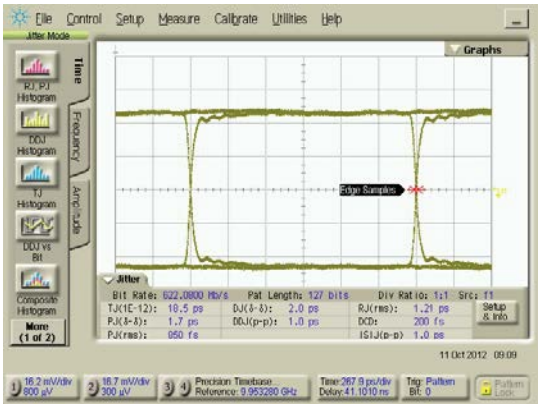
1. Plug the ac power adapter into the wall.
2. Plug the dc output of the power adapter into the ADI-BERT.
3. Connect the USB cable from a PC to the ADI-BERT.
4. Connect the first SMA cable from the PRBS generator DATA output to the error detector DATA input.
5. Connect the second SMA cable from the PRBS generator DATAB output to the error detector DATAB input.
6. Start the PRBS generator GUI by double-clicking the desktop shortcut.
7. Verify that the PCB I^2C communication is working properly.
8. Click **Clear Errors** in the main GUI window.
9. Click **Read Errors** in the main GUI window.
10. The **PRBS Error Count** box in the main GUI window should display 0 errors.

TYPICAL PERFORMANCE



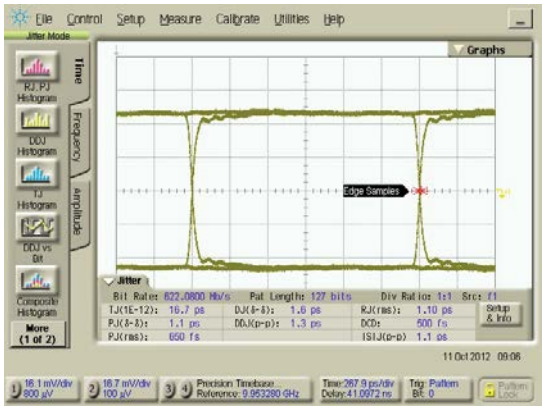
11473-023

Figure 24. Mode 1 Eye Diagram at 11.3 Gbps



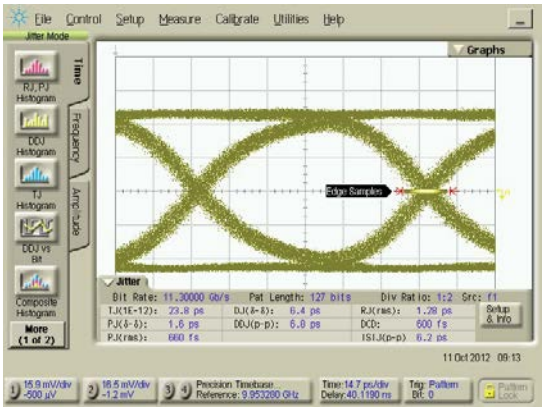
11473-026

Figure 27. Mode 2 Eye Diagram at 622.06 Mbps



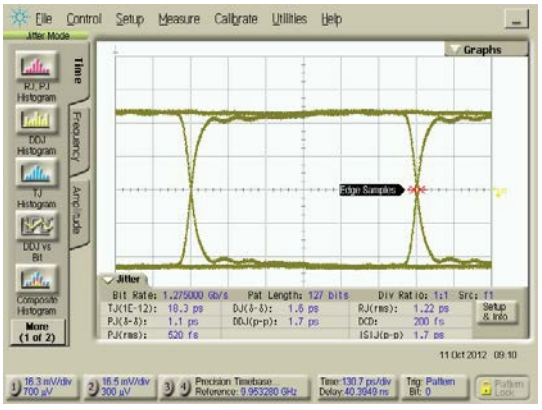
11473-024

Figure 25. Mode 1 Eye Diagram at 622.08 Mbps



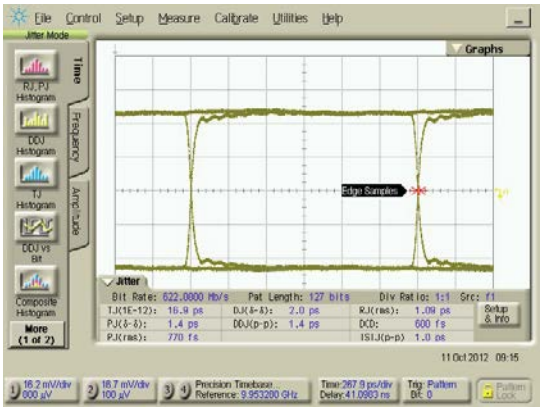
11473-027

Figure 28. Mode 3 Eye Diagram at 11.3 Gbps



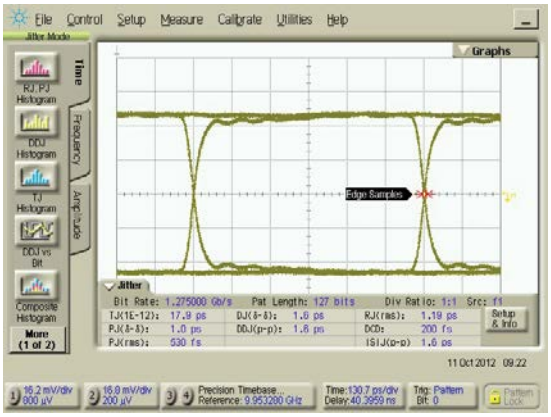
11473-025

Figure 26. Mode 2 Eye Diagram at 1.275 Gbps



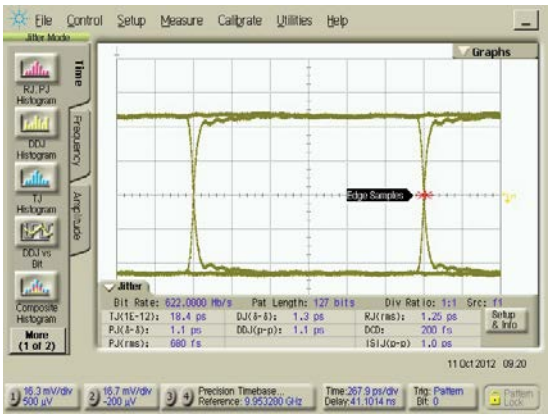
11473-028

Figure 29. Mode 3 Eye Diagram at 622.08 Mbps



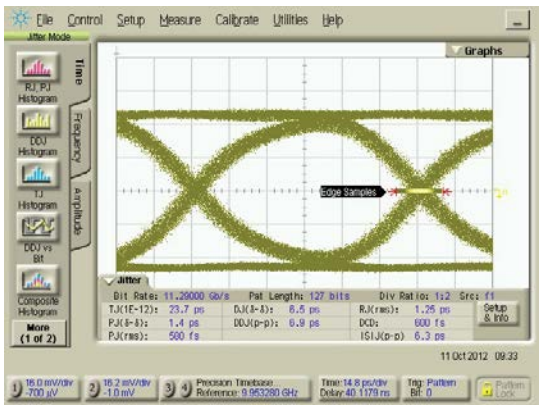
11473-029

Figure 30. Mode 4 Eye Diagram at 1.275 Gbps



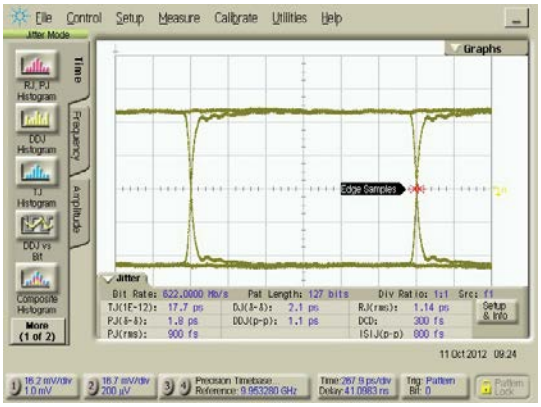
11473-030

Figure 31. Mode 4 Eye Diagram at 622.08 Mbps



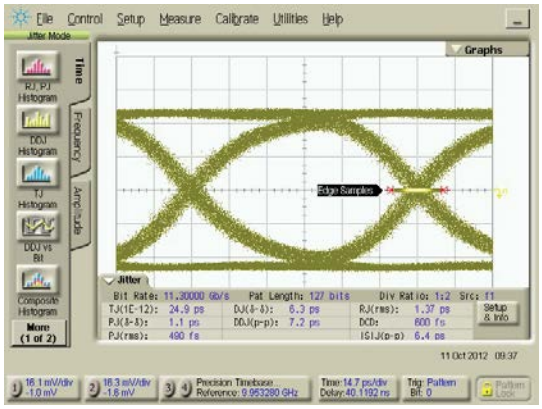
11473-031

Figure 32. Mode 5 Eye Diagram at 11.3 Gbps



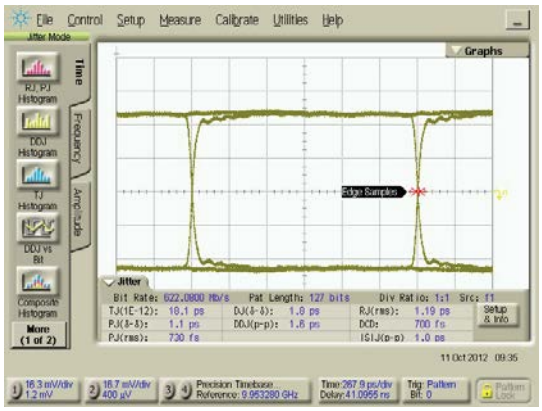
11473-032

Figure 33. Mode 5 Eye Diagram at 622.08 Mbps



11473-033

Figure 34. Mode 6 Eye Diagram at 11.3 Gbps



11473-034

Figure 35. Mode 6 Eye Diagram at 622.08 Mbps

RELATED LINKS

Resource	Description
ADN2915	Product Page: Continuous Rate 6.5 Mbps to 11.3 Gbps Clock and Data Recovery IC with Integrated Limiting Amp/EQ
AD9577	Product Page: Clock Generator with Dual PLLs, Spread Spectrum, and Margining
ADP1706	Product Page: 1 A, Low Dropout, CMOS Linear Regulator
EngineerZone	Online Community: Analog Devices Online Technical Support Community

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG11473-0-1/14(A)