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APPLICATION NOTE

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Synchronous Inverse SEPIC Using the ADP1870/ADP1872 Provides High Efficiency for Noninverting Buck/Boost Applications

by Matthew C. Kessler

INTRODUCTION

In many markets, demand is increasing for efficient noninverting dc-to-dc converters that can operate in either buck or boost mode, decreasing or increasing the input voltage to a desired regulated voltage, with minimal cost, component count, and power loss. The inverse single-ended primary inductor converter (SEPIC), also known as the Zeta converter, has many properties that make it ideal for this function (see Figure 1). An analysis of its operation and implementation with the ADP1870/ADP1872 synchronous switching controllers reveals its useful properties for this application.

INVERSE SEPIC FUNDAMENTALS

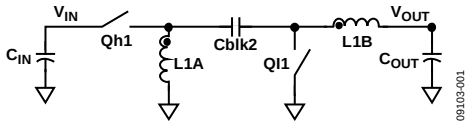

Figure 1. Inverse-SEPIC Topology

Primary Switch Qh1 and Secondary Switch Ql1 operate in opposite phase from one another. During the on time, Qh1 is conducting and Ql1 is off. Current flows in two paths, as shown in Figure 2. The first is from the input, through the primary switch, the energy-transfer capacitor (Cblk2), the output inductor (L1B), and the load, finally returning back to the input through ground. The second path is from the input, through the primary switch, the ground-reference inductor (L1A), and back to the input through ground.

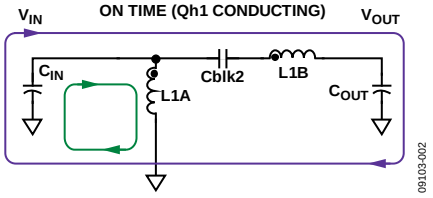

Figure 2. Current-Flow Diagram—Qh1 Closed and Ql1 Open

During the off time, the switch positions are reversed. Ql1 is conducting, and Qh1 is off. The input capacitor (C_{IN}) is disconnected, but current continues to flow through the inductors in two paths, as shown in Figure 3. The first is from the output inductor, through the load, through ground, and back to the output inductor through the secondary switch. The second path is from the ground-reference inductor, through the energy-transfer capacitor, the secondary switch, and back to the ground-reference inductor.

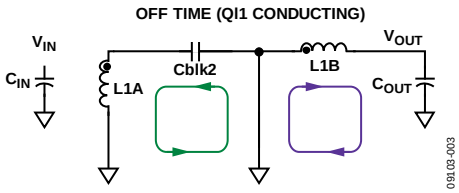

Figure 3. Current Flow Diagram—Ql1 Closed and Qh1 Open

By applying the principles of inductor volt-second balance and capacitor charge balance, the user finds the equilibrium dc conversion ratio specified in Equation 1.

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} \quad (1)$$

where D is the duty cycle of the converter (on-time fraction of the switching cycle).

Equation 1 suggests that if the duty cycle is more than 0.5, a higher voltage is regulated at the output (boost); if the duty cycle is less than 0.5, the regulated voltage is lower (buck). Other relevant results of this analysis are that the steady-state voltage across the energy-transfer capacitor (Cblk2) is equal to V_{OUT} in a lossless system; the dc value of the current through the output inductor (L1B) is equal to I_{OUT}; and the dc value of the current through the ground-reference inductor (L1A) is $I_{OUT} \times V_{OUT}/V_{IN}$. The energy-transfer capacitor also provides dc blocking from V_{IN} to V_{OUT}. This property can be attractive when there is a risk of a shorted output.

The analysis also shows that the output current in the inverse SEPIC is continuous, yielding a lower peak-to-peak output voltage ripple for a given output capacitor impedance. This allows the use of smaller, less costly output capacitors as compared to discontinuous output current topologies.

TABLE OF CONTENTS

REVISION HISTORY

9/10—Rev. A: Rev. B

Changes to Inductor Coupling, Energy-Transfer Capacitor Section 5
Changes to Power Component Stresses Section 6

7/10—Rev. 0: Rev. A

Changes to Figure 9, Figure 10, and Figure 11 7

6/10—Revision 0: Initial Version

INVERSE SEPIC TOPOLOGY IMPLEMENTED WITH THE ADP1870/ADP1872

SYNCHRONOUS IMPLEMENTATION

Typically, the secondary switch (Ql1) is a unidirectional power diode, which limits the peak efficiency of this topology. However, with the Analog Devices, Inc., ADP1870/ADP1872 single-channel synchronous switching controllers (see Appendix A), an inverse SEPIC can be designed in a fully synchronous configuration, employing a bidirectional MOSFET as the secondary switch. This allows the peak efficiency to increase considerably, while decreasing the size and cost of the converter at output currents greater than approximately 500 mA.

Figure 5 shows the power stage of the fully synchronous inverse SEPIC configuration, as implemented with the ADP1870/ADP1872. The implementation requires only three small, inexpensive additional components (Cblk1, Ddrv, and Rdrv) that dissipate negligible power.

The ideal steady-state waveforms of the inverse SEPIC are shown in Figure 4. The switch node, SW, (see Figure 5) is toggled between (V_{IN} + V_{OUT}) during the on time and 0 V during the off time. Connecting Charge-Pump Capacitor Cbst to SW imposes a voltage that is approximately equal to V_{IN} + V_{OUT} + V_{DD} on the bootstrapped upper rail of the high-side internal driver (BST pin) and the output of the high-side driver (DRVH pin) during the on time, thus enhancing the primary floating N-channel MOSFET switch, Qh1. The clamping diode, Ddrv, ensures that Cblk1 has approximately V_{OUT} + V_{FWD} (Ddrv) across it during steady-state, as referenced from the DRVH pin to the gate of Qh1, by effectively putting Cblk1 and Cblk2 in parallel during the off time. The voltage across Cblk1 keeps the primary switch from developing a gate-to-source voltage that is higher than its threshold during the off time when the Node X voltage is approximately equal to $-V_{OUT}$.

The ADP1871 and ADP1873 are members of the ADP187x family that have a pulse-skip mode (PSM) that increases the efficiency at light loads by decreasing the switching rate, delivering just enough energy to the output to keep the output voltage in regulation, considerably decreasing the gate charge and switching loss in the buck topology. It is not recommended to implement the ADP1871 and ADP1873 in the synchronous inverse SEPIC topology.

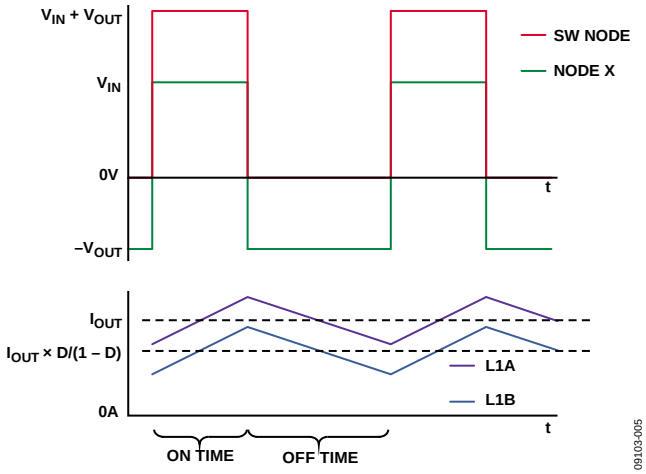

Figure 4. Ideal Waveforms of Synchronous Inverse SEPIC, Dead Time Ignored

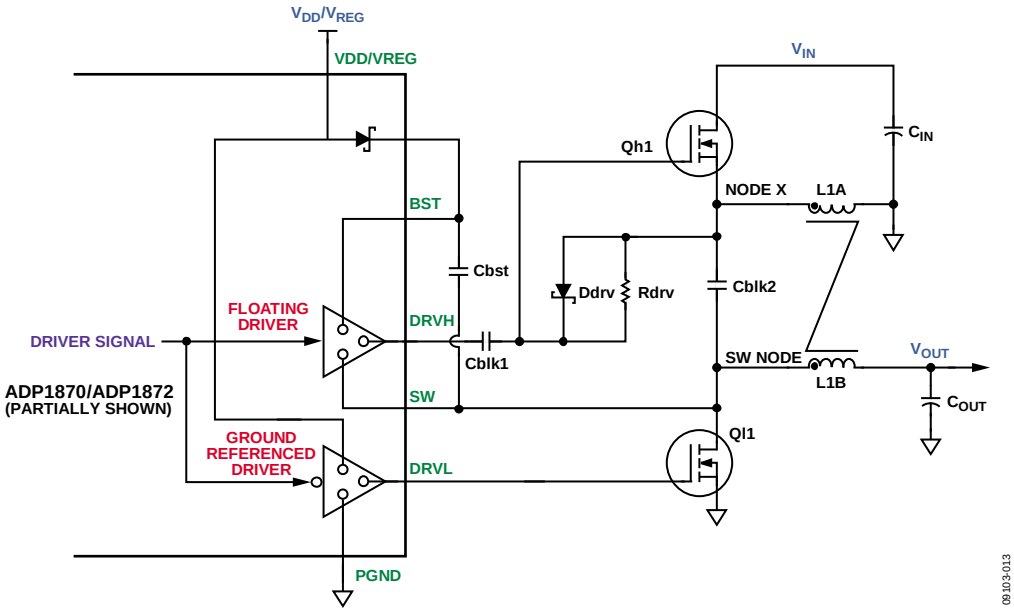

Figure 5. Power Stage with the ADP1870/ADP1872 Internal Drivers Shown

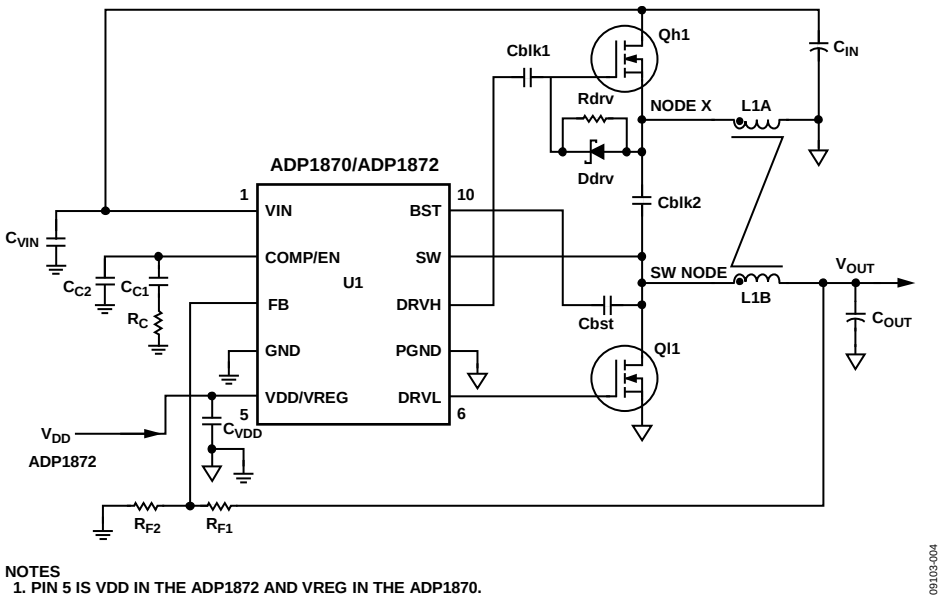

Figure 6. Complete Implementation of Synchronous Inverse SEPIC with ADP1870/ADP1872

PREDICTING SWITCHING FREQUENCY

As described in Appendix A, the ADP1870/ADP1872 use a constant on time architecture with feedforward and switch node averaging techniques to minimize switching frequency variations typically associated with constant on time architectures. The SW pin is connected to the SW node as implemented in the synchronous inverse SEPIC topology (see Figure 6). Accordingly, the switching frequency for each of the parts in the ADP1870/ADP1872 series can be predicted as follows:

$$\frac{1}{f_{SW}} = a \times \left(\frac{V_{OUT}}{V_{IN}} + 1\right) \quad (2)$$

ADP187xARMZ-0.3-R7 – $a = 3.33 \times 10^{-6}$

ADP187xARMZ-0.6-R7 – $a = 1.66 \times 10^{-6}$

ADP187xARMZ-1.0-R7 – $a = 1 \times 10^{-6}$

It should be noted that although these parts are designated as 300 kHz, 600 kHz, and 1 MHz, respectively, these designations only apply to the approximate switching frequency when implemented in the buck topology.

As shown in Figure 7, the switch node average is fed into the on timer. In a lossless system, this average is equal to the output voltage. As the output load increases and the losses in the converter increase, the switch node average becomes slightly less representative of the output voltage, resulting in an increase in switching frequency with an increase in output loading. Typically, this increase is not greater than 10% of the no load condition across the full load range of the load. In very lossy systems, the increase in the switching frequency can be greater than this.

INDUCTOR COUPLING, ENERGY-TRANSFER CAPACITOR

The L1A and L1B power inductors are shown coupled in Figure 6. The purpose for coupling the inductors in this topology is to reduce ripple in the output voltage and inductor current, and to increase the maximum potential closed-loop bandwidth, as explained in the Small-Signal Analysis and Loop Compensation section.

Even though the inductors are coupled, it is undesirable for the coupling to be tight enough to transfer significant energy from one winding to the other through the core. This can be avoided by finding the leakage inductance (L_{LKG}) of the coupled inductor and sizing the energy-transfer capacitor (Cblk2) such that the magnitude of its complex impedance is a tenth of the complex series impedance of the leakage inductance and DCR of a single winding as designated in Equation 2, Equation 3, and Equation 4. Designing the circuit to conform to this relationship minimizes the energy transfer through the coupled core. The leakage inductance can be calculated from the coupling coefficient, commonly found in coupled inductor data sheets.

$$|Z_{Cblk2}| = \sqrt{ESR^2 + \left(\frac{1}{2\pi Cblk2 f_{SW}}\right)^2} \quad (3)$$

$$|Z_{L_{LKG}}| = \sqrt{DCR^2 + (2\pi L_{LKG} f_{SW})^2} \quad (4)$$

$$|Z_{Cblk2}| \leq \frac{|Z_{L_{LKG}}|}{10} \quad (5)$$

As shown in the current flow diagrams, Figure 2 and Figure 3, charge is deposited and removed during the on time and off time, respectively. The current flow through the energy-transfer capacitor should not cause a voltage deviation greater than ±10% of its nominal dc voltage, V_{OUT}, as derived in the Synchronous Implementation section. Sizing Cblk2 such that the following inequality is true ensures that the voltage deviation is sufficiently small.

$$(V_{OUT} \times 0.1) \geq \frac{I_{OUT} D}{fswCblk2} + \left(\frac{V_{IN} D}{2L1Bf_{SW}} + I_{OUT}\right) Cblk2_{ESR} \quad (6)$$

When coupling the inductors, a 1:1 turns ratio is necessary and desirable because it requires half the inductance for each winding that discrete inductors need for a given level of output voltage ripple (see "Coupled-Inductor and Other Extensions of a New Optimum Topology Switching DC-DC Converter" by Ćuk and Middlebrook in the References section).

CAPACITIVELY COUPLED GATE DRIVE CIRCUIT

The value of the gate drive capacitor, Cblk1, is bounded by several operating parameters. It should be of sufficiently high capacitance that the deposition and removal of charge during the turn on and turn off, respectively, of the high-side switch do not cause the voltage to deviate more than ±10% from its nominal dc value. This dc value is V_{OUT} + V_{FWD} (Ddrv), as mentioned in the Synchronous Implementation section. The value of Cblk1 should also be a tenth of Cbst to avoid excessive BST-to-SW node voltage during fault conditions. Finally, the RC time constant of Cbst and Rdrv should be significantly longer than the switching period. Rdrv provides a discharge path for Qh1 after the converter is disabled. Good starting values for Cblk1 and Rdrv are 100 nF and 1 kΩ, respectively. Correspondingly, Cbst should be 1 µF. A common, small, and inexpensive BAT54 Schottky barrier diode is sufficient for Ddrv because it conducts very little current.

SMALL-SIGNAL ANALYSIS AND LOOP COMPENSATION

A complete small-signal analysis of the inverse SEPIC converter is beyond the scope of this application note. However, from an applications perspective, most of this analysis is unnecessary, and a robust circuit can be designed by following a few guidelines.

First, there are many complex impedance interactions at the resonant frequency (f_{RES}), which must be calculated initially to find the upper limit on the target crossover frequency. When the inductors are uncoupled, the resonant frequency decreases, significantly decreasing the potential maximum closed-loop bandwidth.

$$f_{RES} = \frac{1}{2\pi\sqrt{2L_{LKG}Cblk2}} \quad (7)$$

At this frequency, there can be 300° or more of high Q phase lag. To avoid a low phase margin converter across the full load range, the designer should target a crossover frequency (f_{UNITY}) at one-tenth of f_{RES}. Dampening of this resonance is largely dependent on the output loading resistance and the coupled dc resistance of the inductor. To a lesser extent, dampening is dependent on the equivalent series resistance (ESR) of the energy-transfer capacitor, and the on resistance of the power MOSFETs (Qh1 and Ql1). Therefore, as the output load resistance varies, the signature of the closed-loop transfer function may change dramatically at this frequency.

The coupling coefficient is often not a well-controlled parameter, so the target crossover frequency, f_{UNITY}, should be set to a decade below f_{RES}, assuming that f_{RES} is less than the switching frequency, f_{SW}. Standard Type II compensation, with two poles and a zero, can be used when f_{UNITY} is set appropriately.

$$f_{UNITY} = \text{Minimum}\left(\frac{f_{RES}}{10}, \frac{f_{SW}}{10}\right) \quad (8)$$

Figure 7 shows the equivalent circuit of the ADP1870/ADP1872 feedback loops when employed in a synchronous inverse SEPIC buck/boost topology. The upper box contains the power stage and inner current loop; the lower box contains the voltage feedback loop and compensation circuitry.

The compensation-component values in the lower box can be calculated as follows:

$$R_C = \frac{2\pi f_{UNITY} C_{OUT} (ESR + R_{LOAD})^2 V_{OUT}}{G_m G_{CS} R_{LOAD}{}^2 V_{REF}} \quad (9)$$

$$C_{C1} = \frac{C_{OUT}(R_{LOAD} + ESR)}{R_C} \quad (10)$$

$$C_{C0} = \frac{C_{C1} ESR}{R_{LOAD}} \quad (11)$$

where:
C_{OUT} is the output capacitance of the converter.
ESR is the equivalent series resistance of the output capacitor.
R_{LOAD} is the minimum output load resistance.
G_m is the transconductance of the error amplifier, 520 µs for the ADP1870/ADP1872 family.
V_{REF} is the reference voltage that is tied to the positive input of the error amplifier, 0.6 V for the ADP1870/ADP1872.

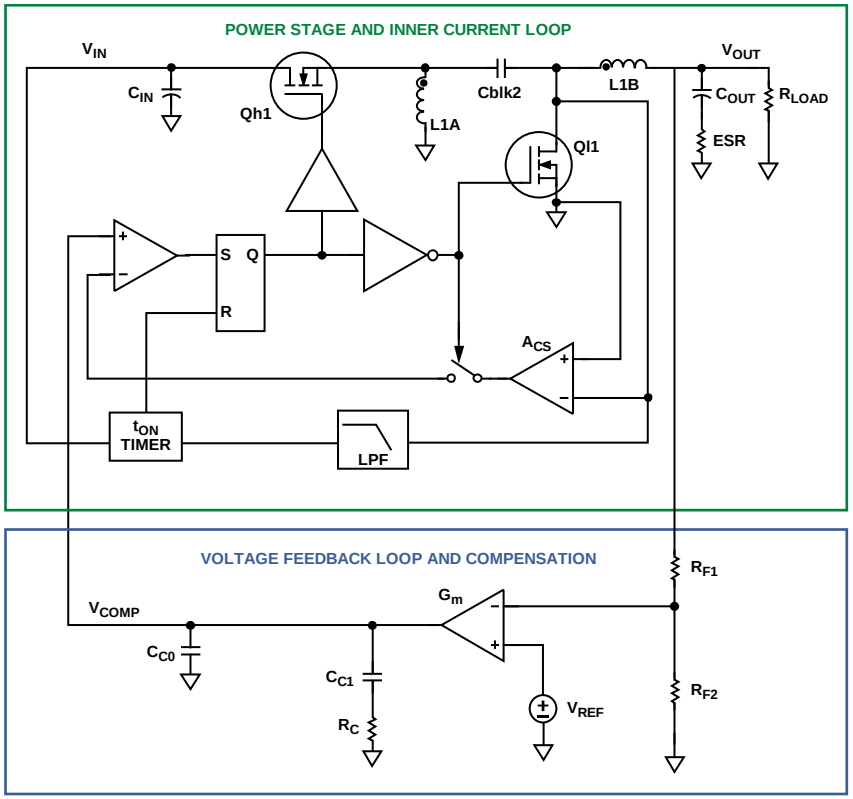

Figure 7. Power Stage with Inner Current-Sensing Loop and Compensation Scheme of the ADP1870/ADP1872 Configured in Synchronous Inverse SEPIC Topology

G_{CS}, the transconductance of the converter, is calculated by:

$$G_{CS} = \frac{1}{A_{CS} R_{DS(ON)MIN}\left(\frac{1}{1-D}\right)} = \frac{\Delta I_{OUT}}{\Delta V_{COMP}} \quad (12)$$

where:

G_{CS} is a frequency-independent gain term that varies with $R_{DS(ON)}$, the resistance of the secondary switch when enhanced, and duty cycle, D. It is expected that the highest crossover frequency occurs when this resistance and the duty cycle, D, are at their lowest.

A_{cs} is the current sense gain, which, with the ADP1870/ADP1872, is selectable in four discrete steps from 3 V/V to 24 V/V.

To ensure that current limit is not induced prematurely, the highest value of current-sense gain (A_{CS}) that obeys the following inequality should be selected:

$$2.53\,\text{V} \geq A_{CS} R_{DS(ON)MAX}\left(I_{OUT}\left(\frac{1}{1-D}\right) - \frac{\Delta I_L}{1.2}\right) + 1.15\,\text{V} \quad (13)$$

where ΔI_L is the peak-to-peak inductor ripple current.

$$\Delta I_L = \frac{V_{IN} D}{2L1Bf_{SW}} \quad (14)$$

Because the ADP1870/ADP1872 use a constant on time architecture, the sampling poles typically associated with current mode control are not present in the control loop. Therefore, the complexity of adding the appropriate amount of slope compensation to the sensed current signal is not necessary.

POWER COMPONENT STRESSES

The current-flow diagrams in Figure 2 and Figure 3 show that the power MOSFETs, when conducting, carry the sum of the inductor currents. Accordingly, the dc component of the current through both switches is

$$I_{DC} = I_{OUT} \frac{1}{1-D} \quad (15)$$

The ac component of the current through both switches is

$$I_{AC} = \frac{V_{IN} D}{L1Af_{SW}} \quad (16)$$

With dc and ac components of the MOSFET current known (shown in Figure 8), the designer can quickly calculate the rms values of the current through each switch. In conjunction with the $R_{DS(ON)MAX}$ of the selected MOSFETs, the rms values can be used to ensure that the MOSFETs are thermally stable, with power dissipation low enough to meet the efficiency requirements.

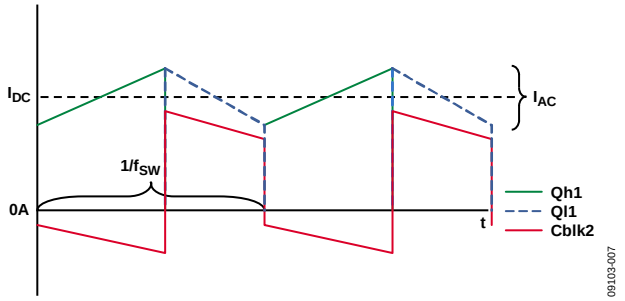

Figure 8. Ideal Current Waveforms of Synchronous Inverse SEPIC, Dead Time Ignored

Calculating switching loss in the primary switch accurately is beyond the scope of this application note, but it should be noted that, in transitioning from high resistance to low resistance states, the voltage across the MOSFET swings from ~(V_{IN} + V_{OUT}) to ~0 V, and the current through the device swings from 0 A to ~I_{OUT}(1/(1 – D)). Switching loss can be the predominant loss with swings of these magnitudes, a factor the user should be aware of when selecting a MOSFET for which the reverse transfer capacitance (C_{RSS}) and $R_{DS(ON)}$ are inversely proportional.

The drain-source breakdown voltage (BV_{DSS}) for both the primary and secondary switches must be greater than the input voltage plus the output voltage (see Figure 4).

The peak-to-peak output-voltage ripple (ΔV_{RIPPLE}) is approximated by

$$\Delta V_{RIPPLE} \approx \frac{\Delta I_L}{8 f_{SW} C_{OUT}} + \Delta I_L \times ESR \quad (17)$$

The rms value of the current through the output capacitor ($I_{rmsCout}$) is

$$I_{rmsCout} \approx \frac{\Delta I_L}{2\sqrt{3}} \quad (18)$$

The peak-to-peak inductor current (ΔI_L) designated in Equation 14 depends on the input voltage, so the designer must ensure that, as this parameter varies, the output-voltage ripple does not exceed the specification, and the rms current through the output capacitor does not exceed its rating.

As shown in Figure 8, the rms current through the energy-transfer capacitor, Cblk2, is

$$Irms_{Cblk2} = \sqrt{D \times I_{OUT}{}^2 + \frac{D}{3}\left[\frac{\Delta I_L}{2}\right]^2 + (1-D)\left[\frac{I_{OUT} D}{(1-D)}\right]^2 + \frac{(1-D)}{3}\left[\frac{\Delta I_L}{2}\right]^2}$$

For high output current applications, putting multiple capacitors in parallel for Cblk2 is often necessary to avoid exceeding the rms rating on an individual capacitor.

For synchronous inverse SEPICs implemented with the ADP1870/ADP1872, the input voltage plus the output voltage must not exceed 20 V because the charge-pump capacitor is connected to the switch node, which reaches V_{IN} + V_{OUT} when the primary switch is conducting.

LAB RESULTS

Figure 9, Figure 10, and Figure 11 show a comparison of the efficiencies achieved for a range of input voltages to 5 V out with both the synchronous inverse SEPIC and asynchronous SEPIC, a more traditional way of implementing a noninverting buck boost. Both circuits have been individually optimized for efficiency to meet a wide input voltage range application and are provided a low current 5 V bias.

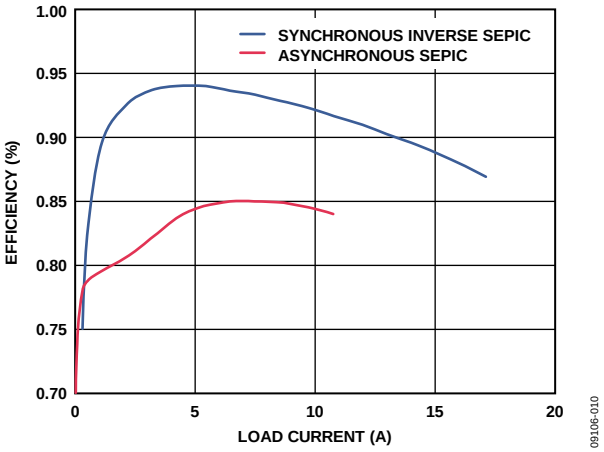

Figure 9. Efficiency vs. Load Current (V_{IN} = 12 V, V_{OUT} = 5 V)

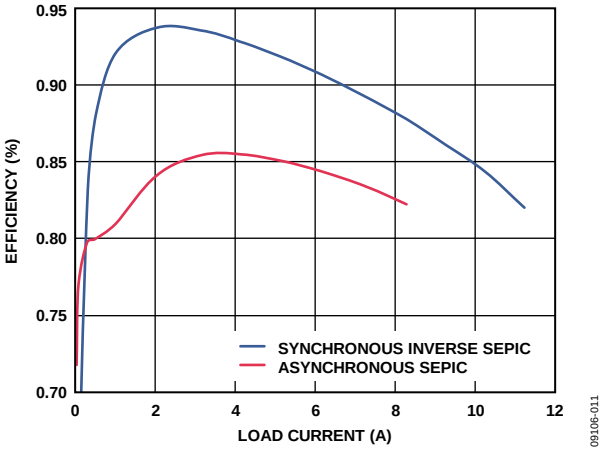

Figure 10. Efficiency vs. Load Current (V_{IN} = 5 V, V_{OUT} = 5 V)

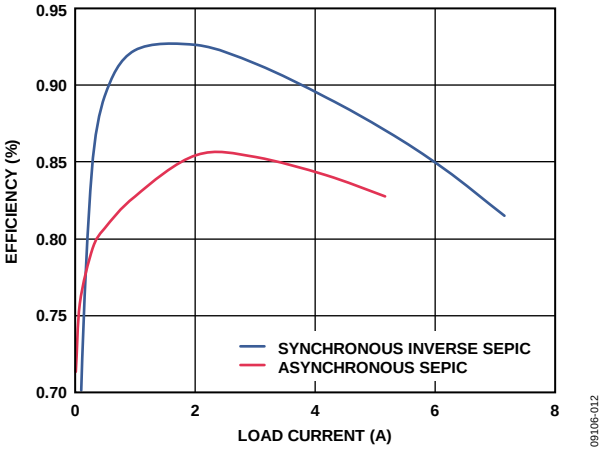

Figure 11. Efficiency vs. Load Current (V_{IN} = 3.3 V, V_{OUT} = 5 V)

The synchronous inverse SEPIC was implemented with the ADP1872, and the bill of materials for the relevant power components is shown in Table 1, which includes only common off-the-shelf components. The asynchronous SEPIC was implemented with an ADP1621 switching controller from Analog Devices. The bill of materials for the relevant power components is shown in Table 2.

As shown in Figure 9 to Figure 11, the synchronous inverse SEPIC is always more efficient than the asynchronous at any output current above approximately 500 mA. At each input voltage, the synchronous inverse SEPIC is capable of providing more output current, at higher efficiency, and with less components. As described in Table 1 and Table 2, the synchronous inverse SEPIC uses two MOSFETs for the power conversion, whereas the asynchronous SEPIC uses two MOSFETs and a large power diode for the power conversion. This result of this is a lower part count, smaller footprint, lower cost, and more output current capability when implemented in the synchronous configuration.

Table 1. Power Components—Synchronous Inverse SEPIC Implemented with ADP1872

Designator	Part Number	Manufacturer	Value	Package	Comment
Qh1	BSC090N03MS	Infineon	30 BV_{DDS}	SuperSO8	Power MOSFET, 11.2 mΩ (maximum) at 4.5 V_{GS}, T_J = 25°C
Ql1	BSC016N03MS	Infineon	30 BV_{DDS}	SuperSO8	Power MOSFET, 2 mΩ (maximum) at 4.5 V_{GS}, T_J = 25°C
L1A/L1B	PCA20EFD-U10S002	TDK	3.4 µH per winding	30 mm × 22 mm × 12 mm	1:1:1:1:1:1 coupled inductor, ferrite, 35.8 mΩ (maximum) DCR per winding

Table 2. Power Components—Asynchronous SEPIC Implemented with ADP1621

Designator	Part Number	Manufacturer	Value	Package	Comment
Power MOSFET	BSC057N03MS	Infineon	30 BV_{DDS}	SuperSO8	Quantity = 2, 7.2 mΩ (maximum) at 4.5 V_{GS}, T_J = 25°C
Power Diode	PDS1040L	Diodes Inc.	40 BV_{RRM}/10 I_O	PowerDI5	V_F = 0.46 V (maximum) at T_S = 25°C
Coupled Inductor	DRQ127-2R2-R	Cooper Bussmann	2.03 µH per winding	10 mm × 12.5 mm × 8 mm	1:1 coupled inductor, ferrite, 7 mΩ (maximum) DCR per winding

CONCLUSION

The need for high efficiency noninverting dc-to-dc converters that provide both higher and lower voltages than the input (boost and buck) is increasing in many markets. The Analog Devices ADP1870/ADP1872 single-phase synchronous switching controllers allow the high loss power diode commonly used in the power stage to be replaced by a low loss MOSFET. With this increase in efficiency comes a cost and solution size reduction that allows the system to meet stringent energy requirements. Robust compensation component values can be calculated quickly by following a few guidelines, and high efficiency can be achieved with common off-the-shelf components.

REFERENCES

Ćuk, Slobodan and R.D. Middlebrook. 1983. "Coupled-Inductor and Other Extensions of a New Optimum Topology Switching DC-DC Converter." *Advances in Switched-Mode Power Conversion*, Volumes I and II. Irvine, CA: Tesla Co.

APPENDIX A

The ADP1870/ADP1872, shown in Figure 12, are constant on time switching controllers with integrated drivers that drive N-channel synchronous power MOSFETs. The constant on time architecture uses input voltage feedforward and switch node averaging techniques to reduce switching frequency variation typically associated with constant on time architectures. The family also uses a leading edge modulation valley current mode control scheme.

The boost diode is built into the ADP1870/ADP1872, lowering the overall component count and system cost. The ADP1870 has an internal linear regulator, whereas the ADP1872 requires a 2.75 V to 5.5 V bias supply.

The ADP1870/ADP1872 include an internally set soft start period, hiccup mode current limit, thermal shutdown protection, and are available in three different switching frequencies. The ADP1870/ADP1872 provide an output voltage accuracy of −0.834%/+0.884% from −40°C to +85°C and −0.834%/+1.084% from −40°C to +125°C junction temperature. Powered by a 2.75 V to 20 V power stage input supply, the ADP1870/ADP1872 are available in the 10-lead MSOP package.

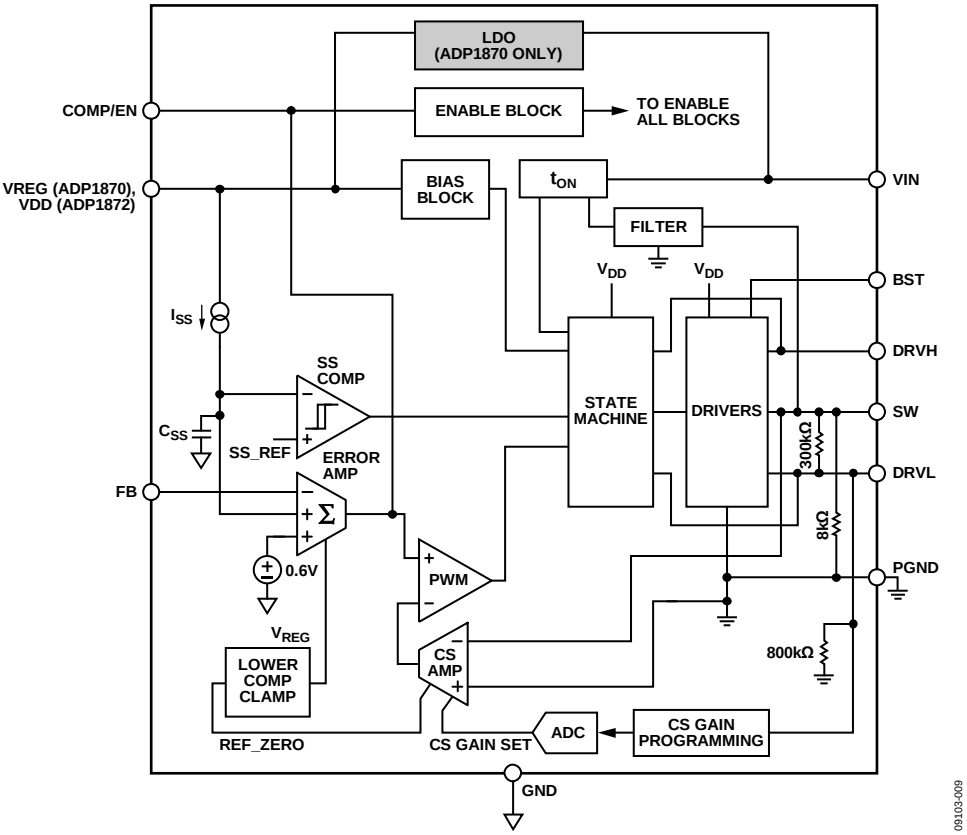

Figure 12. ADP1870/ADP1872 Simplified Block Diagram

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