ANALOG DEVICES

ADP5080CB-1-EVALZ User Guide
UG-752

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Operating the ADP5080 High Efficiency, 6-Channel PMU Evaluation Board

FEATURES

Input voltage range: 4.0 V to 15 V
5 synchronous buck regulators
1 synchronous buck boost regulator
2 keep alive LDOs
1 high voltage LDO
Integrated boost charge pump
Up to 2 MHz switching frequency
High efficiency, auto PSM mode
I²C programmable
4.5 mm × 4.0 mm, WLCSP package

EVALUATION KIT CONTENTS

ADP5080CB-1-EVALZ evaluation board
USB to I²C dongle
ADP5080 demo GUI software

REQUIRED DOCUMENTS

ADP5080 data sheet
ADP5080CB-1-EVALZ evaluation board user guide
ADP5080 Getting Started Software Guide

GENERAL DESCRIPTION

The ADP5080CB-1-EVALZ evaluation board is a complete multicell input, 6+ channel output, power management solution that allows users to evaluate the performance and functionality of the ADP5080. The evaluation board can operate as a standalone unit with the default settings shown in the data sheet. Combined with the GUI software and USB to I²C interface, the ADP5080CB-1-EVALZ evaluation board allows complete programmability of all channels, including the output voltage, switching frequency, startup sequence, and fault protection.

The ADP5080 is a highly integrated PMU with internal synchronous FETs on all channels, internal compensation, and an integrated drive voltage charge pump. The switching frequency is set to 1 MHz for all channels, and is programmable from 750 kHz to 2 MHz via I²C. Switching can also be synchronized to an external clock. Other key features include selectable automatic power save mode (auto PSM) for high efficiency, a high voltage LDO regulator, and global EN pin. The load current capability of the six switching channels ranges from 800 mA to 3 A, making the ADP5080 the highest power density product of its kind.

Complete specifications on the ADP5080 are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD PHOTOGRAPH

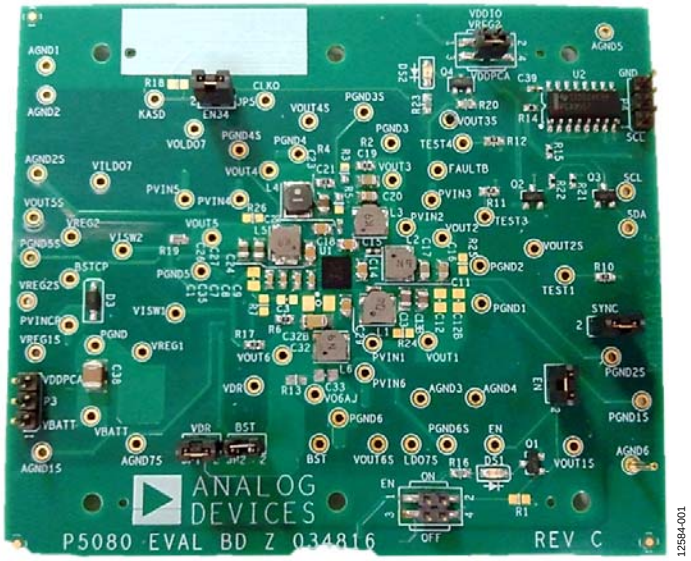

Figure 1.

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REVISION HISTORY

11/14—Revision 0: Initial Version

GETTING STARTED

QUICK SETUP

To get started, take the following steps:

1. Install the ADP5080 GUI software if using I²C control.
2. With the power off, connect an input supply voltage across the VBATT and PGND posts. Set the voltage between 4 V and 15 V.
3. Connect a 3.3 V supply to the VDDPCA post at P3. Either PGND or AGND can be used as ground for this supply.
4. Connect the USB to I²C dongle to the board at P4, and check for proper polarity. Connect the USB side of the dongle to the PC. (This step is not required for standalone operation.)
5. Set the jumpers for EN, SYNC, and VDDIO as desired. Ensure that the VDR and BST jumpers are installed. (Jumper functions are described in the Jumper Settings section.)
6. Connect the loads, DVMs, or other test equipment to Channel 1 through Channel 7 as needed. Connect the loads between the VOUTx and PGNDx pins. Other connections can be made at the VOUTxS and PGNDxS pins.
7. Turn on the input power supplies, VBATT and VDDPCA. If using I²C control, start the GUI software.
8. If the EN jumpers are set to manual control, pull EN and EN34 high to enable the startup sequencer. If the EN jumpers are set to I²C control, click the EN and EN34 buttons in the GUI window.
9. The ADP5080 starts up with Channel 1, Channel 2, Channel 3, Channel 4, and Channel 6 set to start up according to the default sequencer settings. If using I²C control, the default settings and status can be read back.
10. Begin evaluation. Note that all of the typical performance curves shown in the ADP5080 data sheet were taken using this evaluation board. Use the data sheet curves as a reference for evaluation board typical performance.

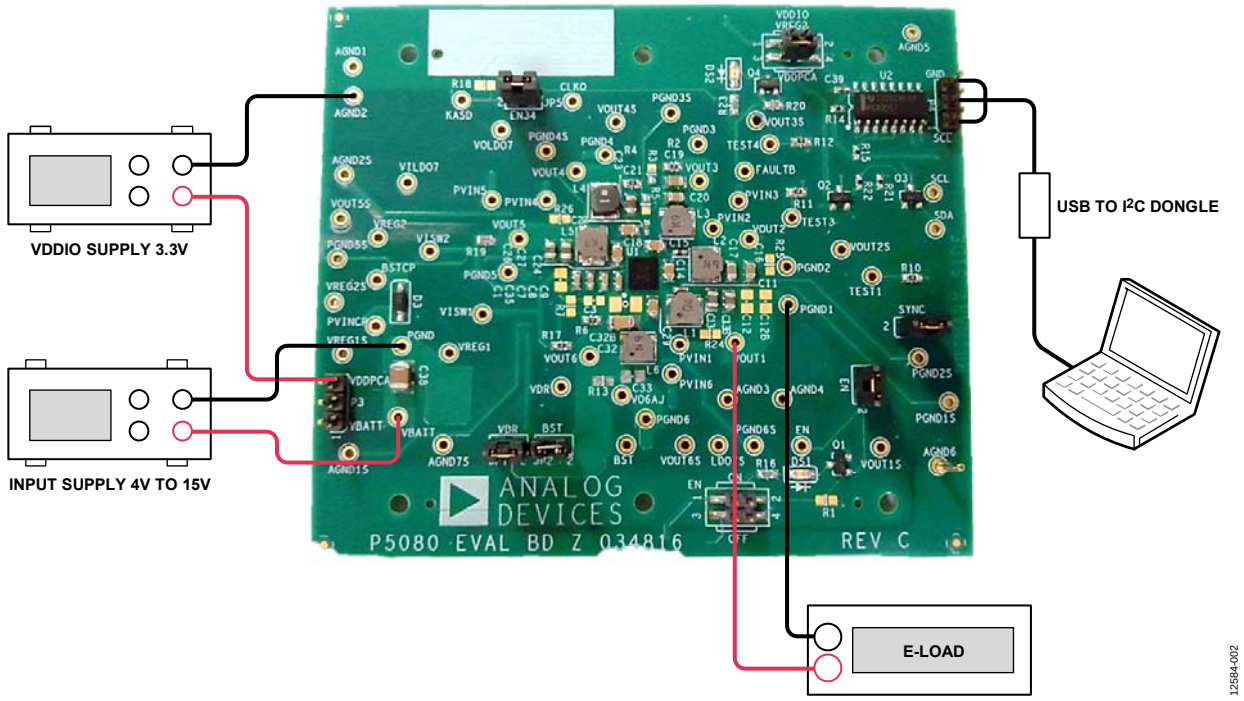
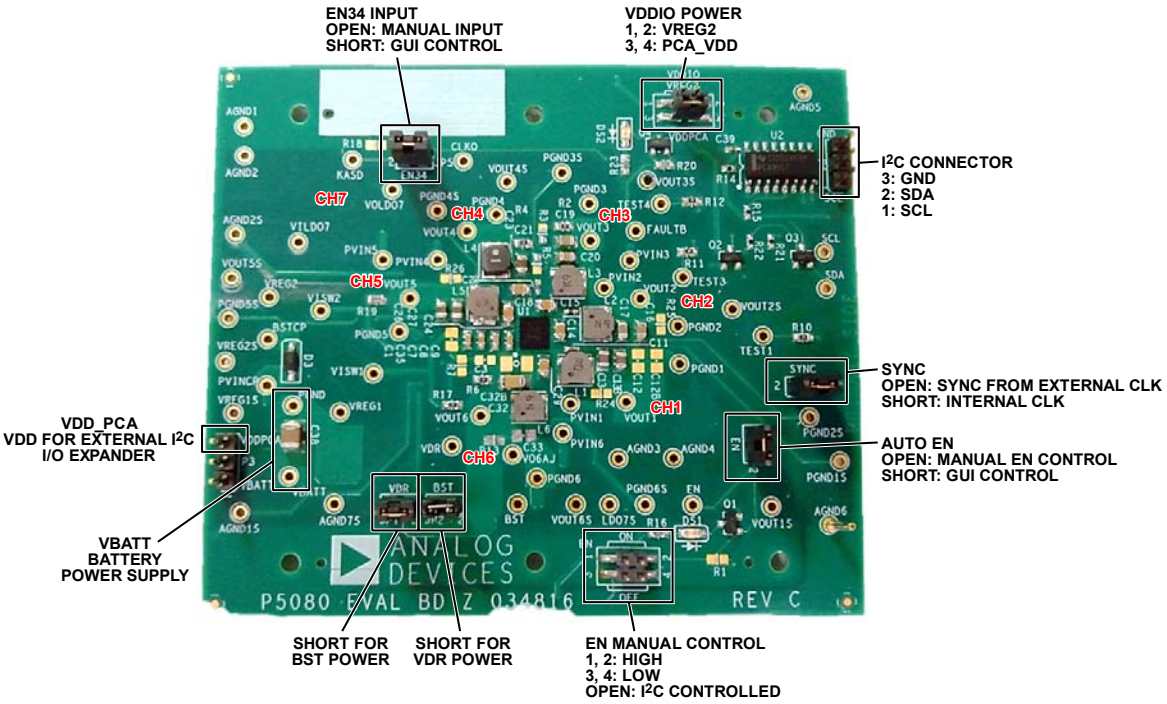


Figure 2. Evaluation Board Basic Hardware Setup with Only Channel 1 Loaded



NOTES
1. CHARGE PUMP FOR CH7 IS LOCATED ON THE BACK OF THE BOARD.

Figure 3. Evaluation Board Overview, Jumper, Power, and Channel Locations

EVALUATION BOARD HARDWARE AND SOFTWARE

OPERATION DETAILS

All of the following descriptions and references refer to the schematics shown in Figure 5 through Figure 7 and the bill of materials shown in Table 1. All components listed in the bill of materials are required, either for PMU system functionality or for individual channel functionality; optional components are listed in Table 2.

Each switching channel and the charge pump has independent input pins (PVINx), which are each connected to VBATT and locally bypassed with input caps. All channel outputs (including LDOs) have one or multiple output caps. The BSTx and VDRx pins provide gate drive voltage and are individually bypassed at the pins. The external components for the charge pump consist of a switching capacitor, protection diode, and input and output capacitors. For details about the selection of required components, refer to the ADP5080 data sheet. Optional components are described in the Optional Components section.

Before evaluating the ADP5080, verify all connections, input voltage, output load, and jumper settings. The leads connecting the input supply to the VBATT and PGND posts must be relatively short (less than approximately 50 cm). The inductance of long input leads can cause switching power supplies to oscillate in some conditions. If using electronic loads, it is recommended to use constant resistance mode; in constant current mode, some electronic loads can pull current from the output down to very low voltage, some down to 0 V. This condition, combined with trace and wire impedance, can create a negative output voltage, which can exceed the absolute maximum rating of the ADP5080 and potentially cause damage.

For each channel output, including the three LDOs, there are power output terminals labeled VOUTx and PGNDx. These should be used to connect all loads. For each channel output there are also sense terminals, labeled VOUTxS and PGNDxS; use these terminals for voltage measurements, but not for pulling currents. Scope measurements can be taken from either set of terminals, but noise or ripple measurements must be taken either directly across the output caps or at the VOUTx terminals.

There are two large connector landing patterns on the bottom side of the board, P1 and P2, which are used for Analog Devices, Inc., internal testing purposes only. Because all of the input and output signals are routed to these connectors, use caution to avoid inadvertently shorting the pads.

JUMPER SETTINGS

There are seven jumpers on the ADP5080CB-1-EVALZ evaluation board, as shown in Figure 2.

The BST jumper connects the output of the charge pump (BSTCP) to the three boost input pins (BST16, BST23, and BST45). All of the switching channels require this boost voltage to drive the high side power FETs; therefore, the BST jumper must be installed for normal operation.

The VDR jumper connects the VREG1 voltage to the four low side drive voltage pins (VDR12, VDR34, VDR5, and VDR6). Similar to the BST voltage, VDR is required by all switching channels as a drive voltage for the low side power FETs. The VDR jumper must be installed for normal operation. If VREG1 is used as an external voltage supply, use a 2.2 Ω resistor instead of a short across the VDR jumper to prevent damage to the ADP5080 in case of an accidental VREG1 short to ground.

The SYNC jumper connects the SYNC pin to ground for internal oscillator operation. To synchronize to an external clock, remove the jumper and connect the external clock signal to Pin 2 of the SYNC jumper.

The EN34 jumper connects the EN34 pin to the output of the I^2C interface IC, U2. To use the GUI to control EN34, connect this jumper. For manual control, leave the jumper open and drive the EN34 by connecting to the terminal post labeled EN34. The EN34 function controls Channel 3 and Channel 4, but can be disabled via I^2C so that EN controls all the channels including Channel 3 and Channel 4. By default, the EN34 function is on.

The EN jumper has the same function as the EN34 jumper, connecting the EN pin to the I^2C interface IC. Connect this jumper to control the EN pin through the GUI.

If the EN jumper is open, the pin can be driven directly at the terminal post labeled EN, or via Jumper JP3. Jumper JP3 pulls the EN pin high to VDDPCA by shorting Pin 1 to Pin 3. Alternately, shorting Pin 3 to Pin 4 pulls the EN pin to GND to disable the ADP5080.

The VDDIO jumper is used to select which voltage is applied to the VDDIO pin: VDDPCA or VREG2. Assuming that VDDPCA is 3.3 V, either setting can be used. A typical application uses the VDDIO voltage of the I^2C host.

OPTIONAL FUNCTIONS

Several installed components are optional: those related with the $\overline{\text{FAULT}}$ function, EN LED, I²C EN control, and the LDO7 input voltage doubler. The components associated with these functions can be omitted from designs without affecting the operation of the ADP5080.

R20 is the pull-up resistor for the open-drain fault flag. In normal operation, the $\overline{\text{FAULT}}$ terminal is pulled high to VDDPCA. In a fault condition, the Q4 and R23 components turn on the DS2 LED.

The DS1 LED similarly indicates the EN state. When EN is high, Q1 and R16 turn on the LED.

EN and EN34 can be controlled manually or, as a convenience, through the GUI software. When GUI control is selected, the I²C input/output expander U2 controls the EN and EN34 pins.

Although not required for operation, a voltage doubler is included in the evaluation board to provide a high voltage input to the Channel 7 LDO. This circuit provides a typical voltage of 10 V + VBATT at VILDO7 using C36, C37, and the D1 dual diode. In place of this doubler, any external voltage between 5 V and 25 V can be used as an input to LDO7.

OPTIONAL COMPONENTS

The ADP5080CB-1-EVALZ evaluation board provides several pad locations for optional components that are not installed, but which may be useful in some applications.

The ADP5080 has three channels with adjustable output voltage mode: Channel 3, Channel 4, and Channel 6. In adjustable mode, the FB voltage is 0.8 V and requires a resistor divider at the FBx pin to set the desired output voltage. These channels have a top side FB resistor of 0 Ω installed. The bottom side FB resistor is not installed. If using adjustable mode, calculate the required FB resistors as follows:

$$RFB_{TOP} = RFB_{BOTT} \times \left(\frac{V_{OUT}}{0.8\ \text{V}} - 1 \right)$$

A value between 10 kΩ and 50 kΩ is appropriate for the bottom side feedback resistor. For a fixed output voltage setting, neither resistor is required; VOUTx can be directly connected to FBx.

If the output voltage is modified from the default setting, the inductor and output capacitor values may also need to be changed. Refer to the ADP5080 data sheet for detailed component selection guidelines.

For the channels without adjustable mode, an uninstalled resistor is connected in the feedback path (R24, R25, and R26). These resistors are intended to be used when measuring the control loop gain and phase. For this measurement, cut the FB trace between the resistor pads, install the required resistance (typically 50 Ω), and inject the signal across the resistor.

There are three uninstalled input capacitor pads that can be used to reduce input ripple or noise coupling. C1 and C3 are input caps for the VISWx pins. If the internal LDOs are bypassed using the VISWx function, the VREG1 and VREG2 voltages are instead supplied from Channel 5 and Channel 6. This is the default setting. However, if other noisier voltage sources are used, C1 and/or C3 can be useful. C34 is an additional input capacitor for LDO7. Do not install this capacitor if using the charge pump double circuit installed on the evaluation board. However, if an external voltage source is used in place of the doubler, C34 can be installed if more input capacitance is needed. If installed, ensure that the connections to C+ and BSTCP are removed.

Channel 1 is a high current, low output voltage channel well suited to supply core voltage rails. Therefore, VOUT1 may need to have very low ripple. For this purpose, C12B and C13B are provided as optional output capacitor pads. Additional output capacitance can be added here to reduce ripple and noise on Channel 1. There is no practical limit on how much capacitance can be added.

The EN and EN34 pins are internally pulled low. However, R1 and R18 are optional components that can be used to increase the pull-down strength, if required.

Channel 6 is set to buck boost mode by default. To operate in buck only mode, several circuit modifications are required, which are enabled by R13 and C33. To switch the ADP5080 to buck only mode, install 0 Ω at R13 and move C32 to C33. After C32 is moved, cut the SW6B trace running between the C32 pads. Finally, ensure that buck only mode is set in the GUI before enabling Channel 6.

R13 and C33 cannot be installed if operating in buck boost mode; the capacitive discharge into the SW6B pins would damage the device.

TEMPERATURE AND PCB

The ADP5080CB-1-EVALZ evaluation board is a 6-layer board with 1 oz of copper per layer. Figure 8 to Figure 12 show five of the six layers. The PVINx and PGNDx layers are shown together on one image, and there is an additional AGND layer not shown. Note that each switching channel has somewhat isolated PVIN and PGND routing on the power layer, which is recommended to minimize switching noise. Five of the six layers are flooded with copper, which is also recommended to improve thermal performance.

With all channels on at full load, the evaluation board can operate in a maximum ambient temperature of approximately 80°C. The junction to ambient thermal resistance (θ_{JA}) of the ADP5080 mounted to the evaluation board is approximately 13°C/W. Temperature measurements can be taken by probing directly on the top side of the WLCSP package. The top case temperature is nearly identical to the junction temperature.

GUI SOFTWARE OPERATION

Although the evaluation board can be operated as a standalone unit, the comprehensive flexibility and feature set of the ADP5080 are not available without making use of its I²C programmability. The ADP5080 demo GUI software is an easy to use tool that provides access to all the programmable I²C registers.

Follow the instructions in the ADP5080 Getting Started Software Guide to install the GUI software. The software package also installs the driver for the USB to I²C dongle. When the installation is complete, connect the USB to I²C dongle between the PC and the evaluation board, apply power to VBATT and VDDPCA, and start the GUI software.

For detailed operation instructions for the GUI, refer to the ADP5080 Getting Started Software Guide.

There are three tabs within the GUI window: **Channels**, **Config**, and **History**. At the top of the screen are the status indicators and global commands, such as EN and EN34. Before enabling the ADP5080 (manually or via GUI control), review the register settings in the GUI.

In the **Channels** tab are controls for start and stop sequence, output voltages, switching frequency, independent enables for each channel, and other functions. All of the programmable registers of the ADP5080 are available in the GUI tabs. For detailed descriptions of each register, refer to the product data sheet.

The **Config** tab contains the controls for auto PSM mode, switching phase, $\overline{\text{FAULT}}$ and PGD status, and other functions. The **Config** tab is also where each channel is set to sequencer mode or manual mode. In sequencer mode, the channel is automatically enabled when EN goes high, according to the set EN delay time and soft start time. In manual mode, the channel starts only when the independent channel EN on the **Channels** tab is programmed high. Setting MODE_ENx to high enables sequencer mode.

The **History** tab allows the user to save a series of commands and to recall and implement the same sequence later. This tab is especially useful when multiple settings must be changed and reprogrammed after every power-down cycle.

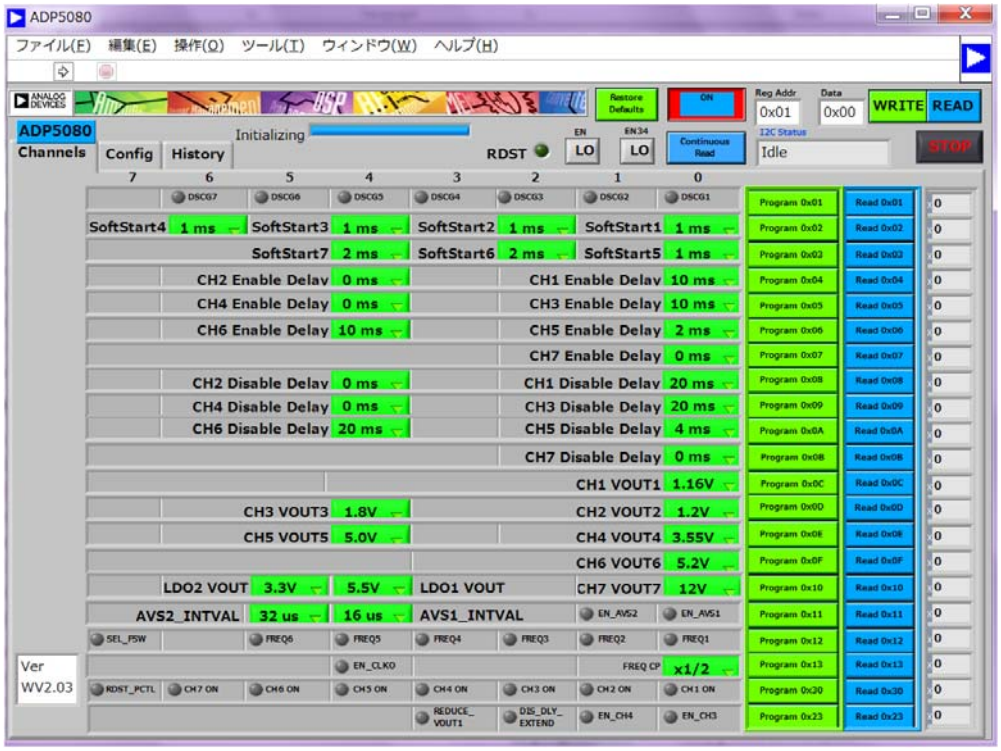


*Figure 4. GUI Window, **Channels** Tab*

EVALUATION BOARD SCHEMATICS AND LAYOUT

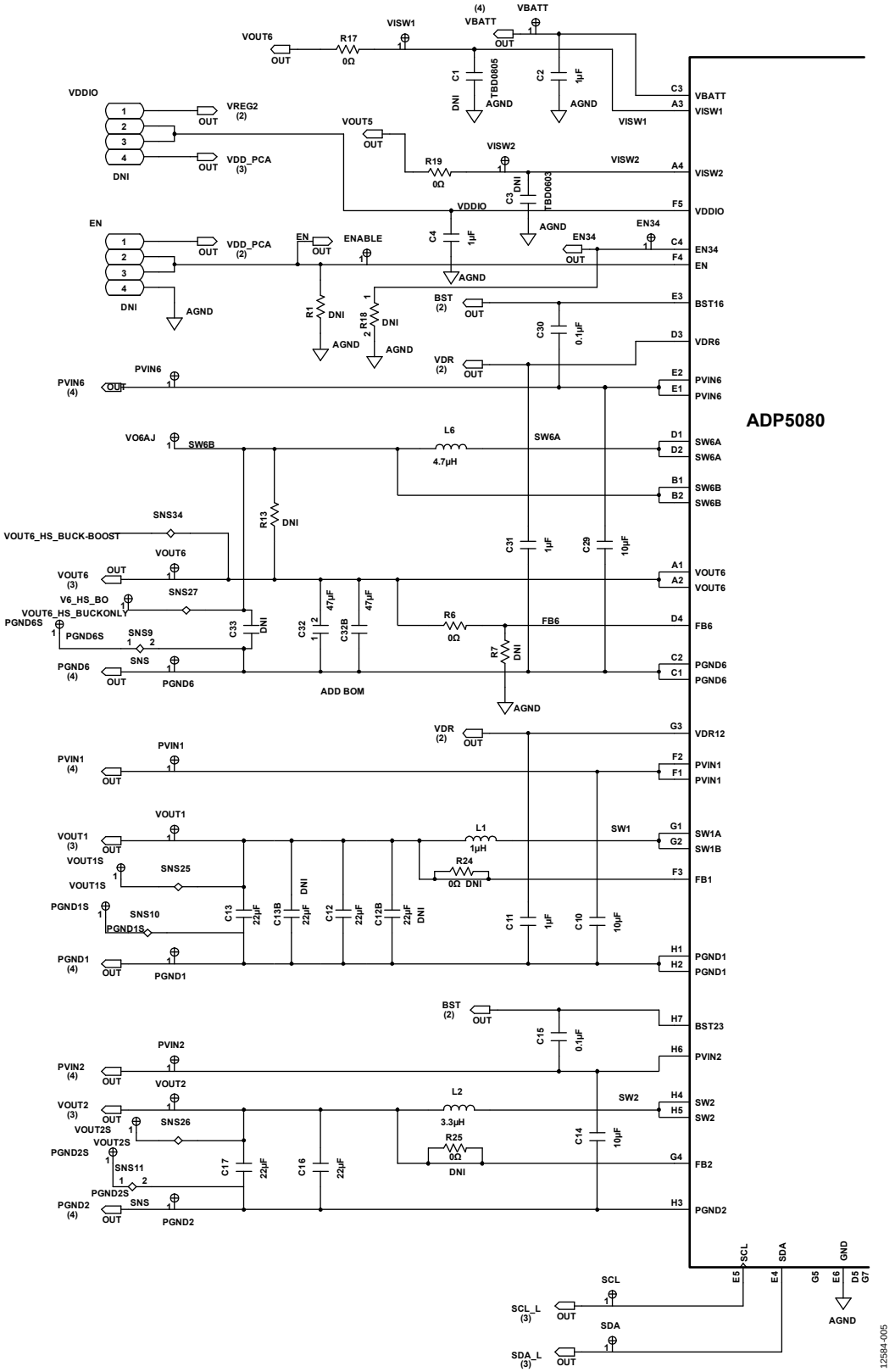


Figure 5. Evaluation Board Schematic, Page 1: Channel 1, Channel 2, and Channel 6

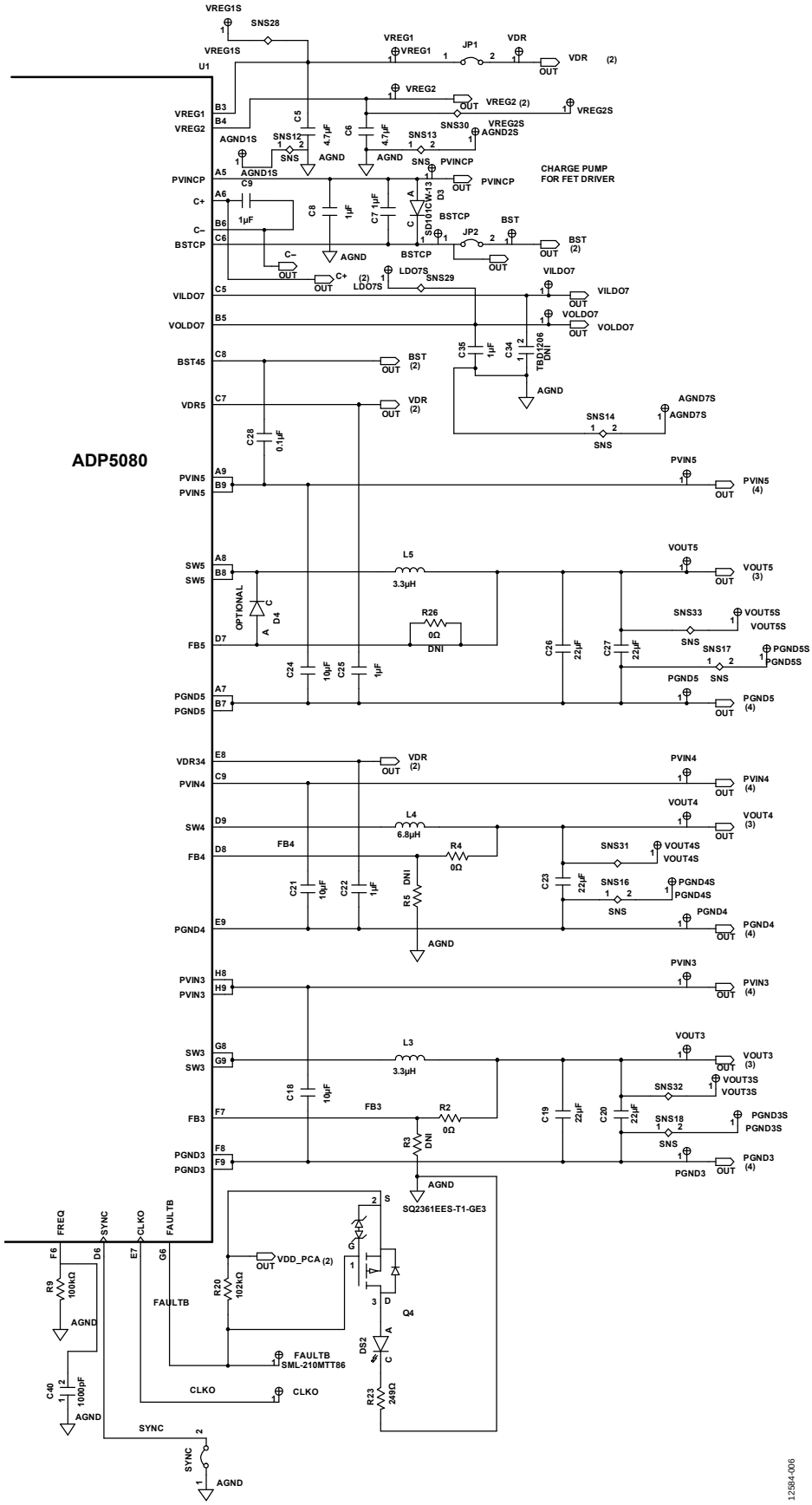


Figure 6. Evaluation Board Schematic, Page2: Channel 3, Channel 4, Channel 5, Channel 7, and Charge Pump

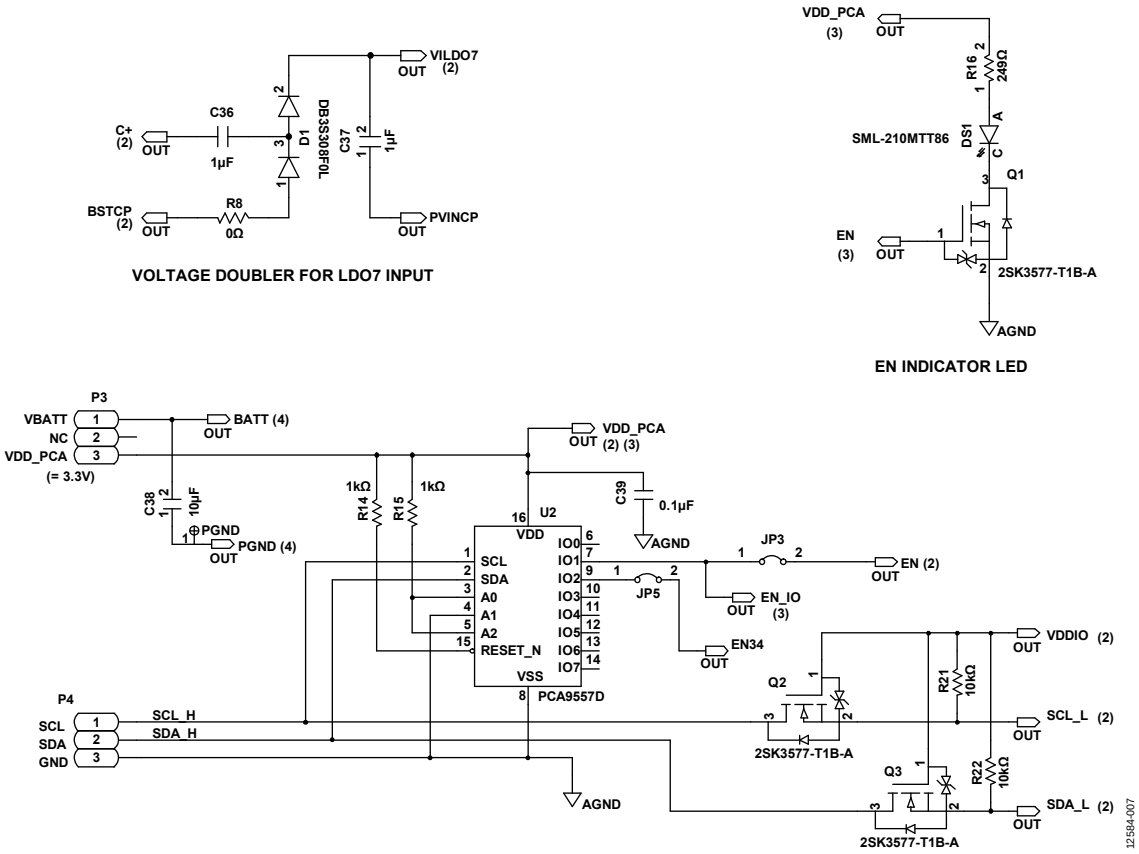


Figure 7. Evaluation Board Schematic, Page 3: LDO7 Input Doubler, EN LED, and I²C Interface

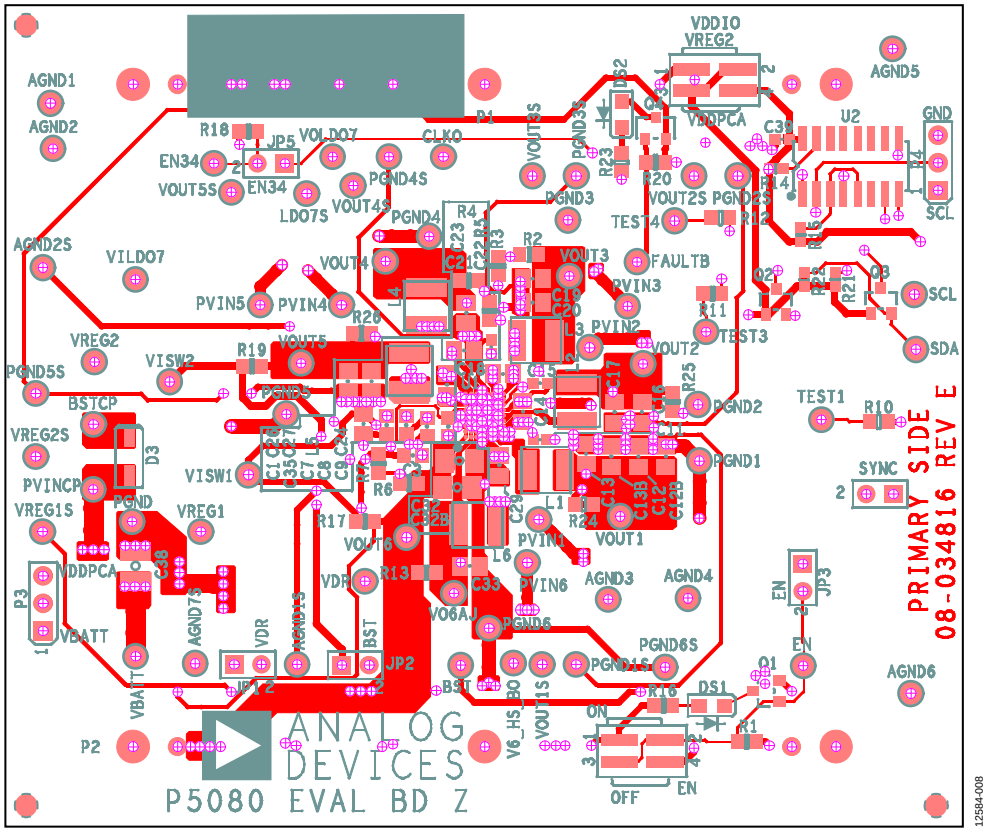


Figure 8. Top Layer PCB Layout

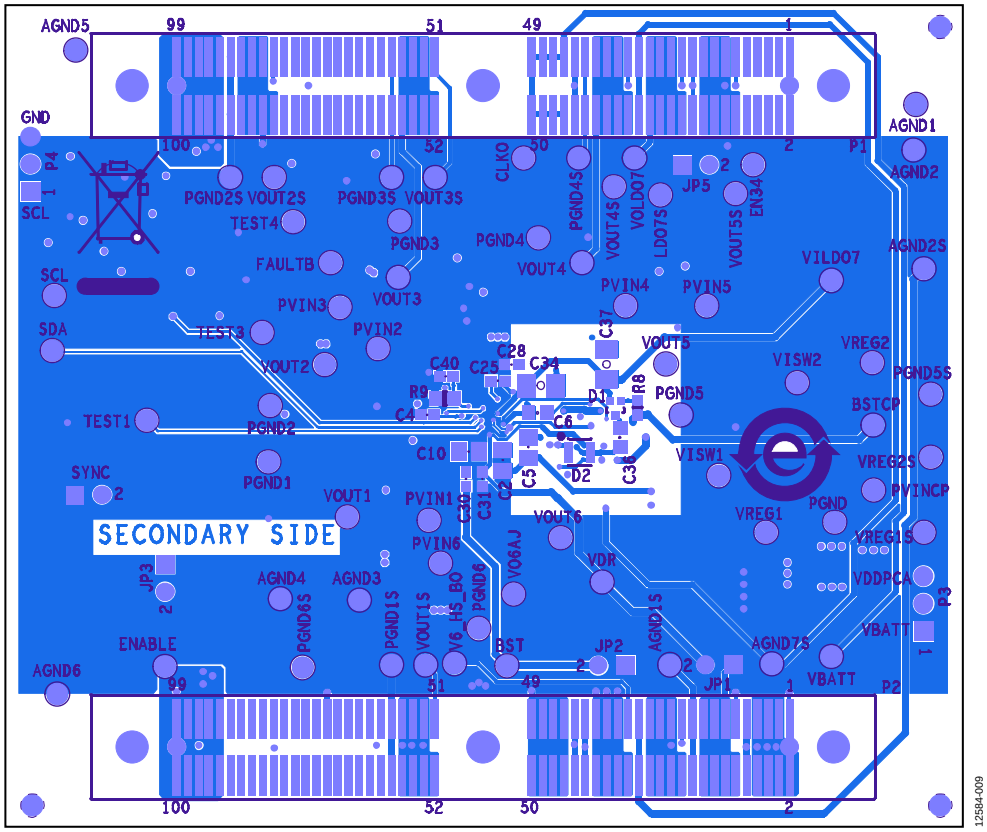


Figure 9. Bottom Layer PCB Layout (Bottom View)

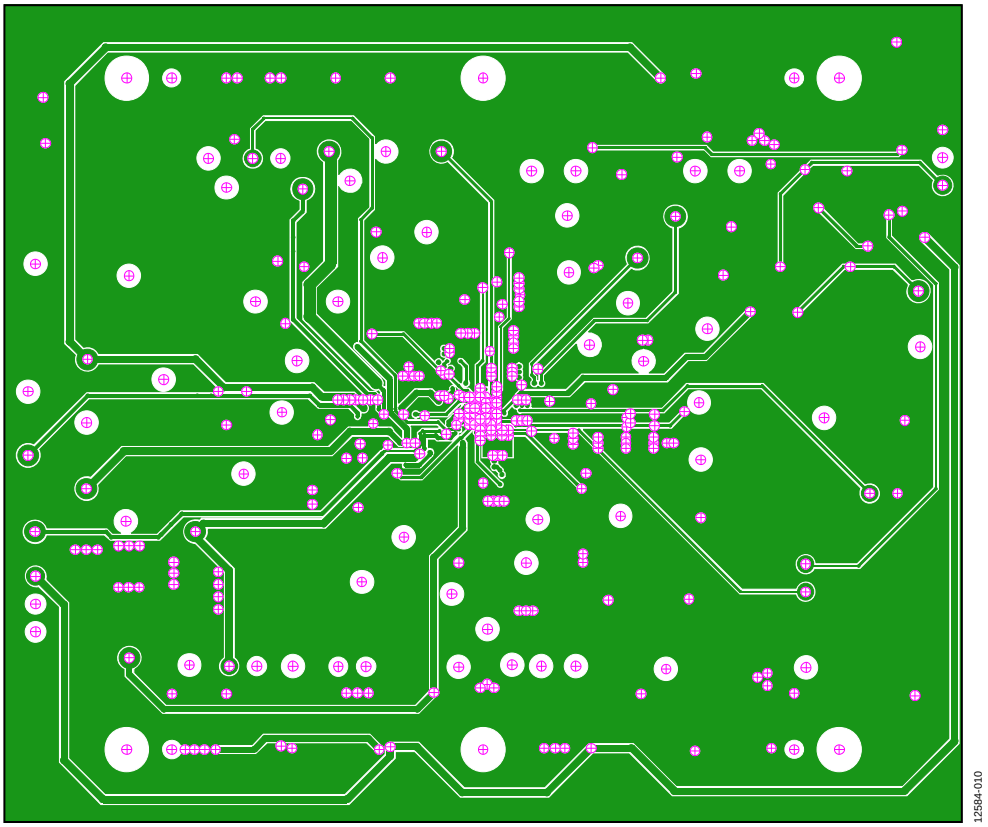


Figure 10. Inner Signal Layer PCB Layout

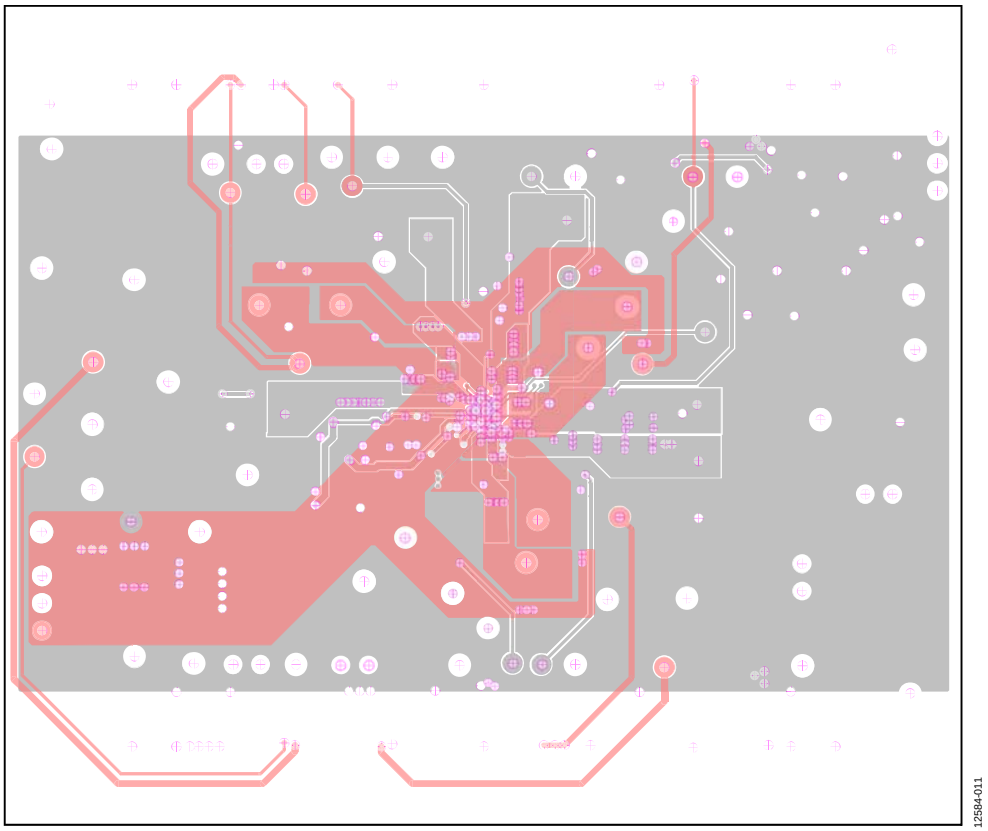


Figure 11. Inner Power and GND Plane PCB Layout

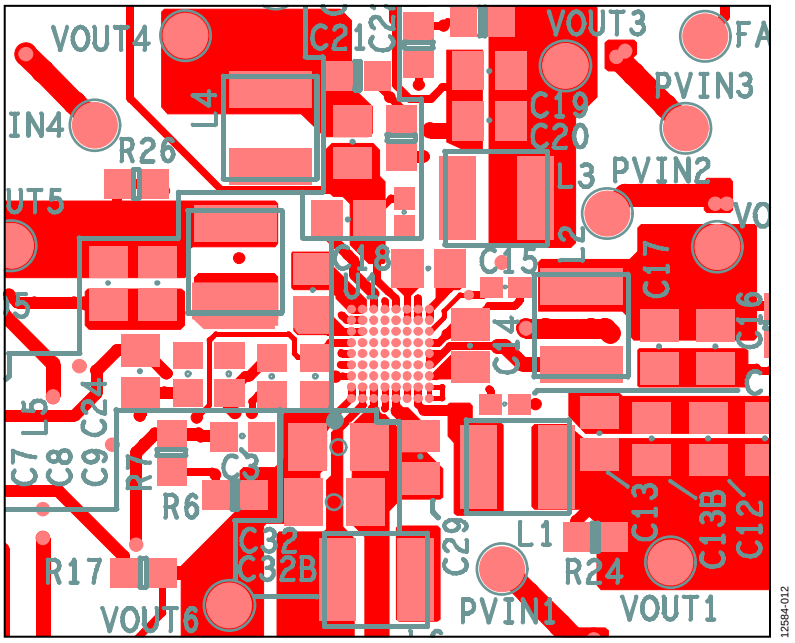


Figure 12. Top Layer PCB, ADP5080 Area Detail

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. Bill Of Materials

Qty	Designator	Description	Case	Manufacturer	Part Number
6	C10, C14, C18, C21, C24, C29	Capacitor, 10 µF, 25 V, X5R	0805	Murata	GRM21BR61E106KA73L
4	C11, C22, C25, C31	Capacitor, 1 µF, 10 V, X5R	0402	Murata	GRM155R61A105KE15D
7	C12, C13, C16, C17, C19, C20, C23	Capacitor, 22 µF, 6.3 V, X5R	0805	Murata	GRM21BR60J226ME39L
3	C15, C28, C30	Capacitor, 0.1 µF, 10 V, X5R	0402	Taiyo Yuden	LMK105BJ104KV-F
1	C2	Capacitor, 1 µF, 25 V, X7R	0805	Murata	GCM21BR71E105KA56L
2	C26, C27	Capacitor, 22 µF, 10 V, X5R	0805	Taiyo Yuden	LMK212BJ226MG-T
2	C32, C32B	Capacitor, 47 µF, 6.3 V, X5R	1206	Murata	GRM31CR60J476ME19L
4	C8, C9, C35, C36	Capacitor, 1 µF, 25 V, X5R	0603	Murata	GRM188R61E105KA12D
1	C37	Capacitor, 1 µF, 35 V, X7R	1206	Taiyo Yuden	GMK316B7105KL-T
1	C38	Capacitor, 10 µF, 25 V, X6S	1210	Murata	GRM32DC81E106KA12
1	C39	Capacitor, 0.1 µF, 16 V, X7R	0402	Murata	GRM155R71C104KA88D
1	C4	Capacitor, 1 µF, 6.3 V, X5R	0402	Murata	GRM155R60J105KE19D
1	C40	Capacitor, 1 nF, 50 V, C0G	0402	Murata	GRM1555C1H102JA01
1	C5	Capacitor, 4.7 µF, 16 V, X5R	0805	Taiyo Yuden	EMK212BJ475KG-T
1	C6	Capacitor, 4.7 µF, 6.3 V, X5R	0603	Murata	GRM188R60J475KE19
1	C7	Capacitor, 1 µF, 10 V, X7R	0603	Murata	GRM188R71A105KA61D
1	D1	Diode, 30 V, silicon	SC89	Panasonic	DB3S308F0L
1	D3	Diode, 40 V, Schottky	SOD123	Diodes	SD101CW-13
2	DS1, DS2	LED, green, 20 mA	0805	Rohm	SML-210MTT86
1	L1	Inductor, 1 µH, 6 A	4.2 x 4.2 mm	Toko	FDSD0420-H-1R0M
3	L2, L3, L5	Inductor, 3.3 µH, 3.4 A	4.2 x 4.2 mm	Toko	FDSD0420-H-3R3M
1	L4	Inductor, 6.8 µH, 1.45 A	4.0 x 4.0 mm	Taiyo Yuden	NRS4018T6R8MDGJ
1	L6	Inductor, 4.7 µH, 3.2 A	4.2 x 4.2 mm	Toko	FDSD0420-H-4R7M
3	Q1, Q2, Q3	N-Channel MOSFET, 30 V, 3.5 A	SC-96	Renesas	2SK3577-T1B-A
1	Q4	P-Channel MOSFET, 60 V, 2.5 A	SOT23-M3	Vishay	SQ2361EES-T1-GE3
8	R2, R4, R6, R10 to R12, R17, R19	Resistor, 0 Ω, 1/10 W	0603	Panasonic	ERJ-3GEY0R00V
2	R14, R15	Resistor, 1 kΩ, 1/10 W	0402	Panasonic	ERJ-2RKF1001X
2	R16, R23	Resistor, 249 Ω, 1/10 W	0603	Vishay	TNPW0603249RBEEA
1	R20	Resistor, 102 kΩ, 1/10 W	0603	Vishay	TNPW0603102KBEEA
2	R21, R22	Resistor, 10 kΩ, 1/16 W	0402	Panasonic	ERJ-2RKF1002X
1	R8	Resistor, 0 Ω, 1/16 W	0402	Panasonic	ERJ-2GE0R00X
1	R9	Resistor, 100 kΩ, 1/10 W	0603	Rohm	MCR03EZPD1003
1	U1	IC, Integrated PMU	WLCSP72	Analog Devices, Inc.	ADP5080ACBZ-1-RL
1	U2	IC, CMOS 8-bIT I^2C bus expander	SO16	NXP	PCA9557D

Table 2. Optional Components, Not Installed

Qty	Designator	Description	Case
1	C1	Optional VISW1 bypass cap	0805
2	C12B, C13B	Optional Channel 1 output caps	0805
1	C3	Optional VISW2 bypass cap	0603
1	C34	Optional Channel 7 input cap	1206
1	C33	Optional Channel 6 output cap for buck only mode	0805
1	D2	Not installed	MCPH6
3	R3, R5, R7	Optional FB resistors for adj VOUT	0603
3	R24, R25, R26	Optional FB loop injection resistors	0603
2	R1, R18	Optional EN, EN34 pull-down resistors	0603
1	R13	Optional, 0 Ω for Channel 6 buck only mode	0603

RELATED LINKS

Resource	Description
ADP5080	ADP5080 product page
EngineerZone	Analog Devices online technical support community
Circuits from the Lab	Circuit designs that have been built and tested to ensure function and performance and that address common analog, RF/IF, and mixed-signal design challenges

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG12584-0-11/14(0)

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