Engineer To Engineer Note

Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division Phone: (800) ANALOG-D or (781) 461-3881, FAX: (781) 461-3010, EMAIL: dsp.support@analog.com

SHARC Internal Power Consumption Measurements

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There have been many customer inquiries concerning typical power consumption of the SHARC processors. As you all know we only supply a maximum Pint which is based on experimentation. Iddin is measured while executing a radix-2 FFT butterfly with instruction in cache, one data fetch from each block of memory and a DMA transfer from internal memory to internal memory. A similar method of experimentation to try to determine "typical power".

The first issue was to determine what "typical" instructions would be so "typical" power can be determined. A guess was taken. The following is a description of the test cases:

Test Case 1 executes an addition, a subtraction, a PM data access and a DM data access.

Test Case 2 executes a multiplication, an addition, a PM data access and a DM data access.

Test case 3 executes a multiplication, an addition, a subtraction, a PM data access and a DM data access.

Test Case 4 executes a multiplication, an addition and a subtraction.

Test Case 5 executes an addition and a subtraction.

Test Case 6 executes a PM data access and a DM data access.

Test cases were selected assuming "typical" instructions would be associated with number crunching. A jump statement was used to sustain these instructions.

The experiments where performed on an ADSP 21062 rev 2.0 using 3 separate clock rates, 25MHz, 33 MHz, and 40 MHz. (A rev 0.6 part with a 24 MHz clock was also tested. The results were almost identical to those of the rev 2.0). Vddin was fixed at 5.25v. The following table describes the results:

Test CaseIddin @ 24 MHz MHz		Iddin @ 33 MHz	Iddin @ 40
1	380 mA	410 mA	470 mA
2	400 mA	440 mA	500 mA
3	400 mA	440 mA	510 mA
4	280 mA	330 mA	370 mA
5	280 mA	320 mA	360 mA
6a	320 mA	380 mA	420 mA
(50%)	Switching)		
6b		390 mA	440 mA
(100%	Switching)		

The following is a copy of the program used.

#include "def21060.h" #define N 22

.SEGMENT/DM seg_dmda; .VAR buffdm[4] =0x00000000, 0x55555555, 0xFFFFFFF, 0xAAAAAAAA;

.ENDSEG;

.SEGMENT/PM seg_pmda; .VAR buffpm[N] =0x4AA14B47, 0x8DF675D4, 0x43D49B8A, 0xD14BA018, 0x406E4387, 0xCDE5483D, 0x83C36DCA, 0x113A7239, 0x805D15C7, 0x363B3B7C, 0xC3B24032, 0x799065C0, 0x07076A2F, 0x762A0DBC, 0x03A1122C. 0x72C3B5B9, 0x28A1DB6F, 0xB618E025, 0x6BF705B2, 0xF96E0A21, 0x6890ADAF. 0x1E6ED365;

.ENDSEG;

.SEGMENT/PM seg_rth; nop; jump start;

.ENDSEG;

.SEGMENT/PM seg_pmco; start: 10=@buffdm; b0= buffdm; m0 = 0x1;18=@buffpm; b8= buffpm; m8 = 0x1;r0=dm(i0,m0), r4 = pm(i8,m8);r8=dm(i0,m0), r12=pm(i8,m8); call addsub; addsub: r7=r0+r4, r15=r0-r4, r0=dm(i0,m0), r4 =pm(i8,m8); jump addsub (db); r7=r0+r4, r15=r0-r4, r0=dm(i0,m0), r4 =pm(i8,m8); r7=r0+r4, r15=r0-r4, r0=dm(i0,m0), r4 =pm(i8,m8); mulacc: r7=r0*r4(SSFR), r15=r8+r12, r0=dm(i0,m0), r4 =pm(i8,m8); jump mulacc (db); r7=r0*r4(SSFR), r15=r8+r12, r0=dm(i0,m0), r4 =pm(i8,m8); r7=r0*r4(SSFR), r15=r8+r12, r0=dm(i0,m0), r4 =pm(i8,m8); mas: r7=r0*r4(SSFR), r15=r8+r12, r14=r8-r12, r0=dm(i0,m0), r4 = pm(i8,m8);jump mas (db); r7=r0*r4(SSFR), r15=r8+r12, r14=r8-r12,

r/=r0*r4(SSFR), r15=r8+r12, r14=r8-r12, r0=dm(i0,m0), r4 =pm(i8,m8); r7=r0*r4(SSFR), r15=r8+r12, r14=r8-r12, r0=dm(i0,m0), r4 =pm(i8,m8);

.ENDSEG;

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