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Interfacing AD7676 ADCs to ADSP-21065L SHARC® Processors

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Introduction

This application note explains how to interface an AD7676 analog-to-digital (ADC) converter in master serial mode (internal discontinuous clock) with SHARC® ADSP-21065L processors. This application note also provides example code to demonstrate how to program the ADSP-21065L processor's serial port to receive data from the AD7676 converter when the AD7676 is configured in master serial mode, supplying a discontinuous serial data clock to the processor's serial port.

About AD7676 ADCs

AD7676 ADCs are 16-bit, 500 kSPS, charge-redistribution SAR, fully differential analog-to-digital converters (ADCs) that operates from a single 5-V power supply. In addition to the high-speed 16-bit sampling ADC, these parts also contain an internal conversion clock, error correction circuits, and serial and parallel system interface ports.

AD7676 ADCs are factory-calibrated and are comprehensively tested, ensuring that they meet or exceed their AC parameters such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional DC parameters of gain, offset, and linearity.

AD7676 applications include:

- CT Scanners
- Data Acquisition
- Instrumentation
- Spectrum Analysis
- Medical Instruments
- Battery-Powered Systems
- Process Control

AD7676 ADCs can operate in serial mode as well as parallel mode. In serial data mode, they can be configured to supply a serial data clock (master serial interface – internal clock) or they can take serial data clock externally (slave serial interface). In master serial mode, AD7676 converters provide a discontinuous bit clock. This guarantees that the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

AD7676 Product Highlights

The AD7676 A/D converter provides:

- Excellent INL

  The AD7676 has a maximum integral non-linearity (INL) of 1.0 LSB with no missing 16-bit code.

- Superior AC performances

  The AD7676 has a minimum dynamic of 92 dB (94 dB typical).

- Fast throughput

The AD7676 is a 500 kSPS, charge-redistribution, 16-bit SAR ADC with internal error correction circuitry.

- Single-supply operation

  The AD7676 operates from a single 5 V supply and typically dissipates only 67 mW. It consumes 7 µW maximum in power-down.

- Serial or Parallel interface

  Versatile parallel (8 or 16 bits) or 2-wire serial interface arrangement compatible with 3 V or 5 V logic.

About ADSP-21065L Processors

ADSP-21065L processors are general-purpose, programmable, 32-bit processors that allow you to program with equal efficiency in fixed-point or floating-point arithmetic. This programming flexibility combined with the high-performance core and integrated peripherals give the ADSP-21065L SHARC processors an outstanding price/performance value for a wide range of consumer, communications, automotive, industrial, and computer applications.

ADSP-21065L processors are code compatible with the Analog Devices (ADI) SHARC family of processors. As such, customers have immediate access to software and hardware development tools from ADI and third parties.

ADSP-21065L Serial Ports

ADSP-21065L processors feature two synchronous serial ports (SPORTs) that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at 1x clock frequency, providing each with a maximum data rate of 33 Mbit/s. Each serial port has a primary and a secondary set of transmit and receive channels. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be transferred to and from on-chip memory via DMA automatically. Each serial port supports three operation modes: DSP serial port mode, I2S mode (an interface commonly used by audio codecs), and TDM (time division multiplex) multichannel mode.

The serial ports can operate with little endian or big endian transmission formats, with selectable word lengths of 3 bits to 32 bits. Serial port clocks and frame syncs can generated internally or externally.

Figure 1 shows the serial port in core driven mode.

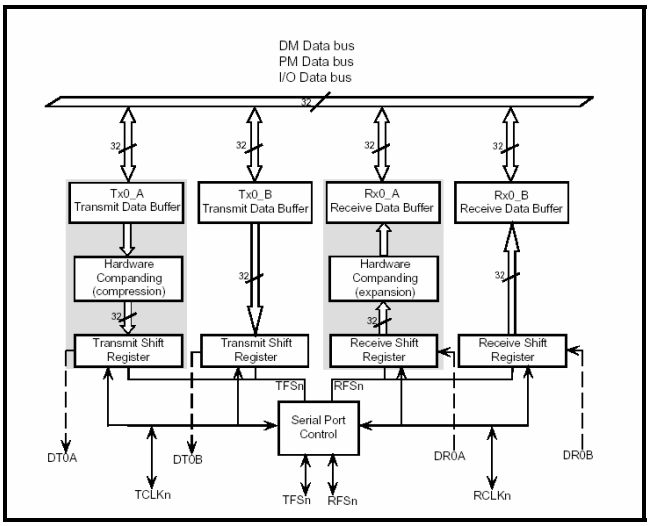

Figure 1. ADSP-21065L Serial Port Block Diagram

AD7676-to-ADSP-21065L Interface

AD7676 ADCs can be configured in serial mode or in parallel mode to transfer 16-bit digitized data to a DSP/processor or a micro-controller. In serial mode, it can be configured to provide a serial bit clock for transferring data to a DSP (called master serial mode). In this mode, the serial clock is discontinuous (or gated) and is present only while transferring data. This provides better noise immunity. This application note discusses the interface in master serial mode because the serial clock supplied by the A/D converter is gated and requires a specific sequence to receive data over the serial port.

The AD7676 converter's serial interface signals that are used with DSP serial port interface comprises the following:

- /CNVST This convert start signal starts conversion. A falling edge on this signal puts the internal sample-and-hold into hold state and initiates a conversion.
- SDOUT The AD7676 drives out conversion results on this pin. The data bits are clocked out on the rising edge or falling edge of the serial clock, based on the state of the INVSCLK pin.
- SCLK The converter clocks the data bits out on the serial clock edges. This can be an input (Slave Serial Mode) or an output (Master Serial Mode).
- SYNC This signal is used as digital output frame synchronization with the internal data clock. This can be configured as an active high or an active low signal from the converter.

Figure 2 shows the timing for the serial interface protocol.

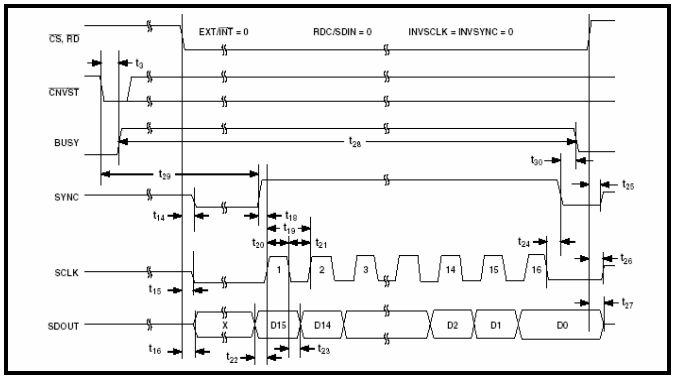

Figure 2. AD7676 Serial Interface Timing Diagram in Master Serial Mode – Read after conversion

Refer to the AD7676 data sheet for detailed information about the timing specifications.

ADSP-21065L SPORT to AD7676

Serial port SPORT0 is used for this interface. The SPORT0 transmit frame sync (TFS0) generates /CNVST for the ADC. The SPORT0 transmit frame sync is configured to be an active low and early frame sync. Also, the frame sync is configured as a data-independent frame sync so that the frame sync is periodically generated to acquire samples from the ADC.

SPORT0 receive clock (RCLK0) and receive frame sync (RFS0) are configured as external. The SPORT receive frame sync is configured to be an active low, late frame sync. The ADC is configured to strobe data bits on the clock's falling edges; thus, the serial port is configured to sample data on the serial clock's rising edges.

Refer to Figure 3 for signal connections between the SHARC processors and the ADC.

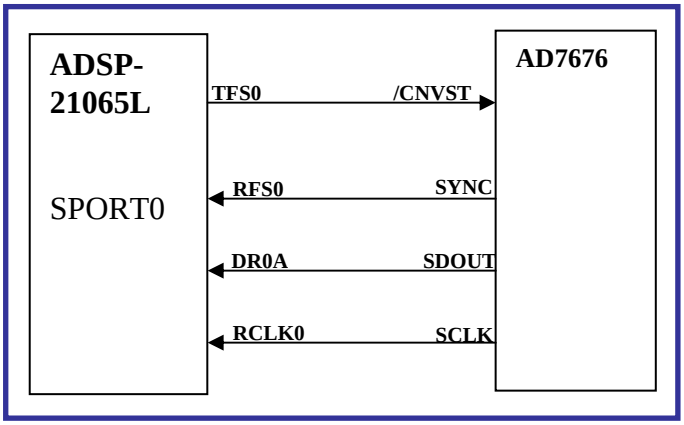

Figure 3. ADSP-21065L Serial Port Interface with AD7676 - Block Diagram

SPORT0, which reads digitized samples from the ADC, must configured initially for a serial word length of 15 bits. Inside the first receive interrupt service routine (ISR), the serial world length should be changed on-the-fly to 16 bits. Note that the first two reads (the 15-bit read and the next immediate read) must be dummy reads for the interface to function properly.

Figure 4 is one example of the serial interface signals is one example.

Figure 4. ADSP-21065L SPORT Interface with AD7676 – Oscilloscope Capture of Interface Signals

As shown in Figure 4, the ADC drives serial data on the serial clock's falling edges. The ADSP-21065L processor's serial port samples the data on the serial clock's rising edges.

The interface functions satisfactorily with either a framed mode or unframed mode for receive frame sync.

Appendix

The project files are included in a ZIP file attached to this application note.

ADSP-21065L_SerialPort_with_AD7676.asm

```
/*****************************************************************************/
//
// Name:     Interfacing ADSP-21065L with AD7676
//
/*****************************************************************************

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File Name:       ADSP-21065L_SerialPort_with_AD7676.asm

Date Modified:   08/19/04                      Rev 1.0

Software:       VisualDSP++3.5 (July update)

Hardware:        ADSP-21065L EZ-KIT Lite

Purpose:     To receive data from AD7676

*****************************************************************************/

#include <def21065l.h>

#define FRAMED_MODE
//#define UNFRAMED_MODE

.section/dm seg_dmda;
    .var adc_data;
    .var counter = 0;

.section/pm seg_rth;
    nop;nop;nop;nop;
    nop;jump start;

 // Sport receive interrupt
.section/pm seg_sp;
    nop;jump isr; rti;rti;

.section/pm seg_pmco;
start:
    // Configure TFS (CONVST) to be generated continuously
    r0 = 0x0;
    dm(STCTL0) = r0;

    r0 = 0xf0012;
    dm(TDIV0) = r0;

    r0 = DITFS | SPEN_A | SLEN32 | LTFS | ICLK | ITFS | TFSR ;
    dm(STCTL0) = r0;
```

```
    r0 = 0x12345678;
    dm(TX0_A) = r0;

    // Enable interrupts
    bit set mode1 IRPTEN;
    bit set imask SPR0I;

    r0 = 0x0;
    dm(SRCTL0) = r0;

    r1 = 0x0;
    r7 = 0x2;

#ifdef UNFRAMED_MODE
    r0 = SPEN_A|SLEN15|LRFS|LAFS|CKRE;
#endif
#ifdef FRAMED_MODE
    r0 = SPEN_A|SLEN15|LRFS|LAFS|RFSR|CKRE;
#endif
    dm(SRCTL0) = r0;

    nop;
    nop;
    jump(pc,0);

.section/pm seg_pmco;
isr:
    r3 = dm(RX0_A);

    // If it is the first word received, reconfigure the sport for
    // 16 bits
    r0 = dm(counter);
    comp(r0,r1);
    if eq jump reconfigure;

    // Incrementing the counter
    r6 = dm(counter);
    r6 = r6 + 1;
    dm(counter) = r6;

    comp(r6,r7);
    if eq rti;

    dm(adc_data) = r3;
    rti;

.section/pm seg_pmco;
reconfigure:
    // Reconfiguring the serial port for 16 bits.
#ifdef UNFRAMED_MODE
    r0 = SPEN_A|SLEN16|LRFS|LAFS|CKRE;
#endif

#ifdef FRAMED_MODE
    r0 = SPEN_A|SLEN16|LRFS|LAFS|RFSR|CKRE;
#endif
```

```
    dm(SRCTL0) = r0;

    r2 = 1;
    dm(counter) = r2;

    rti;
```

References

[1] *ADSP-21065L DSP Hardware Reference Manual.* Rev 2.0, July 2003. Analog Devices, Inc.

[2] *AD7676 Preliminary Technical Data Sheet.* Rev B. Analog Devices, Inc.

[3] *ADSP-21065L DSP EZ-KIT Lite Evaluation System Manual.* Rev 2.0, January 2003. Analog Devices, Inc.

[4] *Interfacing Gated Clocks to ADSP-21065L SHARC Processors (EE-244).* Rev 1, September 2004. Analog Devices Inc.

Document History

Revision	Description
Rev 1 – October 05, 2004 *by Aseem Vasudev Prabhugaonkar*	Initial Release