Engineer To Engineer Note   EE-106

Technical Notes on using Analog Devices' DSP components and development tools
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Link Port Open Systems Interconnect Cable Standard

Last Modified: *11/10/99*

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Overview

This note describes a cabling standard for connecting multiple SHARC DSPs located on boards that are installed in close proximity to each other in the same system. This standard applies to ADSP-21160 and future SHARC products that use 8-bit link port data transfers.

Cable Specifications

The standard is based on the Honda 26 pin connector.

The cable consists of twelve 50 Ohm coax strands and two 28 AWG stranded wires inside a shield, which ensures minimum cross talk and emissions. The outer shield is a mesh conductor enclosed in an outer shell of nonconductive material.

Users can define the function of the two 28 AWG stranded wires.

This standard is intended for use with cable of arbitrary length. But, unless the signals are buffered at each end, the maximum length of the cable must not exceed one meter.

Honda 26 Pin Connector

The Honda connector RMCA-26JL-AD consists of two rows of thirteen pins. Facing the PC board, they are arranged as shown in Figure 1.
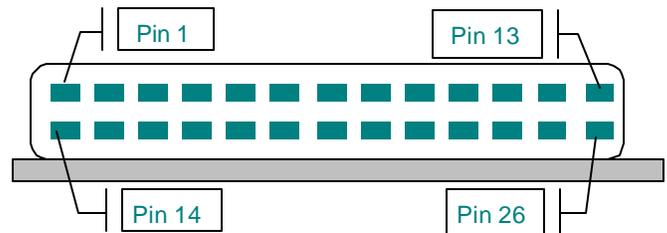
Figure 1. Honda RMCA-26JL-AD connector

At the surface mount pads, pins 14 through 26 are interleaved between pins 1 through 13 as shown in Figure 2.
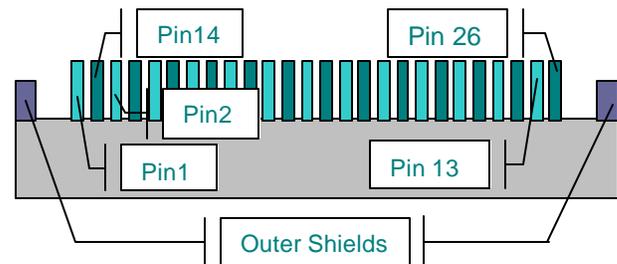
Figure 2. Connector pin arrangements at the surface mount pads

Table 1 lists and describes the pin and signal assignments for the connector on the printed circuit board.

Pin	ADSP-21160 Connection
1	UD1
2	CLOCK
3	ACK
4	D0
5	D1
6	D2
7	D3
8	D4

ANALOG DEVICES

Pin	ADSP-21160 Connection
9	D5
10	D6
11	D7
12	No connect
13	No connect
14	CLOCK SHIELD
15	ACK SHIELD
16	D0 SHIELD
17	D1 SHIELD
18	D2 SHIELD
19	D3 SHIELD
20	D4 SHIELD
21	D5 SHIELD
22	D6 SHIELD
23	D7 SHIELD
24	No connect
25	No connect
26	UD2
—	Outer shields connect to chassis GND

Table 1. Connector pin assignments

Signal Usage

The data sheets for ADI's SHARC DSPs define the use and behavior of most of the signals listed in Table 1.

Guide lines for the use of the user-defined signals, UD1 and UD2, are:

- Since the cable has no provisions to prevent user-defined outputs shorted to user-defined outputs, these outputs must have a 50 Ohm series resistor added to the circuit board.

- User-defined signals must use 3.3V logic levels and have 5V tolerance.

- User-defined signals are intended for low-frequency communications, such as reset or functional synchronization signals.

- To use reset as an input or an output on the link port cable, use the UD1 connection. (For a detailed description of a recommended reset circuit, see

- Reset and Synchronization on page 3.)

Required Cable Materials

Table 2 lists and describes the materials needed to make a link port cable that adheres to this open systems interconnect standard.

Qty.	Mfr.	Part #	Description
2	Honda	RMCA-E26F1S-A	Cable connector
2	Honda	RMCA-E26L1A	Shroud
12 × length	Gore	DXN2132	50 Ohm coax
2 × length	Any		28 AWG wire
Length	Any		Braided outer shield
Length	Any		Nonconductive outer coating

Table 2. Cable manufacturing materials

The male PC board connector is the Honda RMCA-26JL-AD, which provides above-board mounting.

Additional form factors of this PC board connector that require a cut out to enable the board to accept the connector are:

- RMCA-EA26LMY-OM03

- RMCA-EA26LMY-OM06

- RMCA-EA26LMY-OM09

Cable Assembly

The methods of assembly mentioned in this note are a recommendation only. Reasonable deviations that do not affect the function of the finished product are permitted without written approval.

Individual coax strands were chosen instead of a preassembled cable to enable machine fabrication of wire ends and cable assembly.

The connector pin out was chosen so designers could attach an assembly of an inner layer of coax to the connector—COAX1, COAX3, COAX5, COAX7, and so on—and later attach the outer layers—COAX2, COAX4, COAX 6, and so on

Cable Wire

Table 3 lists and describes the conductors and end connections of the cable wires. COAX 11 and 12 are the only twisted conductor wires.

Conductor	Cable End A	Cable End B
Wire 1	Pin 1	Pin 1
COAX 1 center	Pin 2	Pin 2
COAX 1 shield	Pin 14	Pin 14
COAX 2 center	Pin 3	Pin 3
COAX 2 shield	Pin 15	Pin 15
COAX 3 center	Pin 4	Pin 4
COAX 3 shield	Pin 16	Pin 16
COAX 4 center	Pin 5	Pin 5
COAX 4 shield	Pin 17	Pin 17
COAX 5 center	Pin 6	Pin 6
COAX 5 shield	Pin 18	Pin 18
COAX 6 center	Pin 7	Pin 7
COAX 6 shield	Pin 19	Pin 19
COAX 7 center	Pin 8	Pin 8
COAX 7 shield	Pin 20	Pin 20
COAX 8 center	Pin 9	Pin 9
COAX 8 shield	Pin 21	Pin 21
COAX 9 center	Pin 10	Pin 10
COAX 9 shield	Pin 22	Pin 22
COAX 10 center	Pin 11	Pin 11
COAX 10 shield	Pin 23	Pin 23
COAX 11 center	Pin 12	Pin 13
COAX 11 shield	Pin 24	Pin 25
COAX 12 center	Pin 13	Pin 12
COAX 12 shield	Pin 25	Pin 24
Wire 2	Pin 26	Pin 26

Table 3. Cable end connections

Figure 3 shows the connections at each end of the cable.
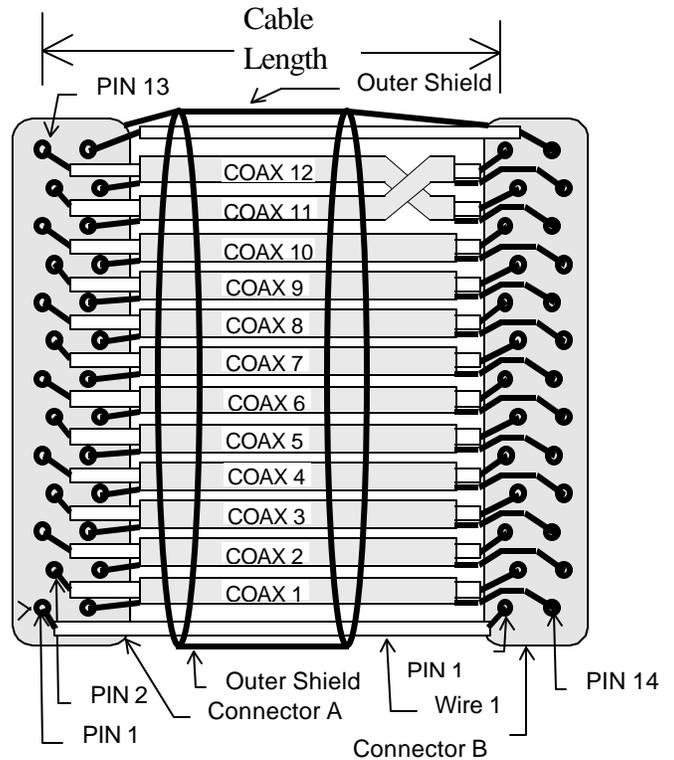
Figure 3. Link port standard cable assembly

Reset and Synchronization

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Currently, the proposed link port cable for the ADSP-21160 and future 8-bit link ports has two user-defined signals. These signals are defined as UD1 and UD2 and connect to pins 1 and 26, respectively, on the Honda 26-pin connector.

Since these signals are not twisted in the cable, pin 1 at one end of the cable connects to pin 1 at the other end of the cable. Likewise, pin 26 at one end of

the cable connects to pin 26 at the other end of the cable.

Transtech proposes to use UD1 as an active-low reset signal and UD2 as a general-purpose synchronization signal. Since the mechanism to transmit and receive synchronization is the same mechanism used for the reset signal, the following description of the reset mechanism describes the synchronization mechanism too.

Figure 4 shows an ADSP-21160 board with four link connectors, one boot link connector (A), and three other link connectors (B, C, and D) on its front panel.

Figure 4. Example ADSP-21160 board

The design can use the boot link connector's UD1 signal to receive a reset and to drive all UD1 signals on all links through open collector outputs.

The PLD contains a small arbiter state machine that arbitrates between the LKAUD1 signal and the internal reset source (such as a register).

If the LKAUD1 signal goes low first, it becomes the "controlling" signal. The state machine asserts the board reset and, by driving the /LKXUD1_OUT signal high, drives low the other UD1 signals, except LKAUD1, through the open collector drivers.

The state machine holds the board in reset and continues to drive the other UD1 signals until the controlling LKAUD1 signal goes high again. Then the state machine deasserts the board reset and releases the other UD1 lines. When it detects another reset, the state machine repeats this procedure.

If the internal reset signal asserts first, the state machine asserts the board reset if needed and drives both /LXXUD1_OUT and /LKAUD1_OUT high to assert all UD1 signals.

The state machine continues to assert the board reset and drives the UD1 signals low until the source deasserts the internal reset signal. Then it deasserts the board reset and releases the UD1 signals. But the state machine must now wait for LKAUD1 to go high again before it can detect new resets. (This is so because the open collector driver of another board might be driving LKAUD1 low.)

The arbiter scheme guarantees that no feedback loops occur. You can expand this scheme to use every link UD1 signal as a reset input, which requires each UD1 signal to have its own output control signal from the arbiter.

The first UD1 to go low becomes the "controlling" signal, and the arbiter drives low all other UD1 signals, except the controlling UD1 signal, through the open collector drivers. Again, the arbiter must wait for all UD1 inputs to go high again before it detects new resets.