# Engineer-to-Engineer Note

# EE-246

## Interfacing AD7276 High-Speed Data Converters to ADSP-21262 SHARC® Processors

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## Introduction

This application note explains how to interface AD7276 high-speed data converters to ADSP-21262 SHARC® processors. This application note also provides example code to demonstrate how the SHARC processor's serial ports (SPI and SPORTs) can be programmed to receive data from AD7276 devices in core and DMA modes. The power-down scheme for AD7276 ADCs between conversions in DMA mode is also described.

## About AD7276/7277/7278 ADCs

The AD7276/AD7277/AD7278 devices are 12-, 10-, and 8-bit, high-speed, low-power, successive-approximation ADCs, respectively. The parts operate from a single 2.35 V to 3.6 V power supply and feature throughput rates up to 3 million samples per second (MSPS).

The conversion process and data acquisition are controlled using the /CS signal and the serial clock, allowing the devices to interface with variety of microprocessors or DSPs. The input signal is sampled on the falling edge of /CS, and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7276/AD7277/AD7278 ADCs use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from VDD. This allows the widest dynamic input range to the ADC. Thus, the analog input range for the part is from 0 V to VDD. The conversion rate is determined by the serial clock SCLK.

### AD7276/7277/7278 Product Highlights

- 3 MSPS ADCs in a 6-lead TSOT package

- Pin compatible to AD7476/7477/7478 and AD7476A/7477A/7478A parts

- High throughput with low power consumption

- Flexible power / serial clock speed management

  The conversion rate is determined by the serial clock. Increasing the serial clock speed reduces the conversion time. This reduces average power consumption while in power-down mode (i.e., while not converting). The part also features a power-down mode to maximize power efficiency at lower throughput rates. Current consumption is 1 µA max in power-down mode.

- Reference derived from the power supply

- No pipeline delay

  The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a /CS input and once-off conversion control.

### AD7276/7277/7278 A/D Applications

AD7276/7277/7278 applications include:

- Battery-Powered Systems
- Personal Digital Assistants
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems
- Data Acquisition Systems
- High-Speed Modems
- Optical Sensors

## About ADSP-21262 Processors

The ADSP-21262 is the first member of the third-generation of SHARC programmable processors. A range of applications such as high-quality audio and automotive entertainment systems, voice recognition, medical appliances and measurement devices benefit from the ADSP-21262 processor's integration of large on-chip memory with a wide variety of peripherals—thereby speeding time to market and keeping costs low.

The ADSP-21262 derivative, which is based on the SHARC processor core, supports execution of 32-bit fixed-point and 32/40-bit floating-point arithmetic formats. With its core running at 200 MHz (5-ns instruction cycle time), the ADSP-21262 processors are capable of executing complex Fast Fourier Transform (FFT) operations—a 1024-point complex FFT in 46 µs, more than 2.6 times faster than comparatively priced processors. In audio applications, the single-instruction, multiple-data (SIMD) mode effectively doubles the processor's performance.

The ADSP-21262 processor is designed with the highest level of integration, including 2 Mbits of on-chip dual-ported SRAM and 4 Mbits of mask-programmable ROM memory. This large amount of on-chip dual-ported memory enables sustained processor and I/O performance without the need for external memory. System I/O is achieved through six full-duplex serial ports, four timers, a 16-bit parallel port, a serial peripheral interface (SPI), 22 zero-overhead Direct Memory Access (DMA) channels delivering fast data transfers without processor intervention, and an innovative Digital Applications Interface (DAI) offering complete software control through its Signal Routing Unit (SRU).

## AD7276-to-ADSP-21262 Interface

This application note uses an AD7276 high-speed data converter for the interface. The other converters in this family (AD7277 and AD7278) are functionally identical. The ADC has a serial interface for DSPs and micro-controllers to transfer the 12-bit digitized data. The ADC supports SPI (Serial Peripheral Interface) and SPORT (DSP Serial Port interface) protocols. ADSP-21262 processors can connect to AD7276 ADCs over their SPI or SPORT interfaces.

The serial interface of AD7276 comprises three signals:

- `/CS` Chip Select is an active low input. This signal initiates A-to-D conversion and frames the serial data transfer.

- `SDATA` The AD7276 drives conversion results onto this pin. The data bits are clocked out on the falling edge of the serial clock.

- `SCLK` Serial clock is an input to the ADC. The converter clocks the data bits out on the falling serial clock edges.

The falling edge on `/CS` puts track-and-hold in to hold mode and also initiates conversion. For compatibility with a 16-bit word length supported by SPI, the ADC outputs 16 bits. The first two bits (zeros) are followed by 12 valid data bits and two zero bits in the end of the serial data stream. Though the ADC data is 12 bits wide, every word is transferred as a 16-bit word. This helps since the SPI word length in ADSP-21262 processor is configurable as 8, 16, or 32 bits only. When interfaced to a serial port, the

serial word length can be configured as 14 bits; hence, the last two bits are not necessary. On the SCLK's 14th rising edge, the converter logic goes back to track mode.
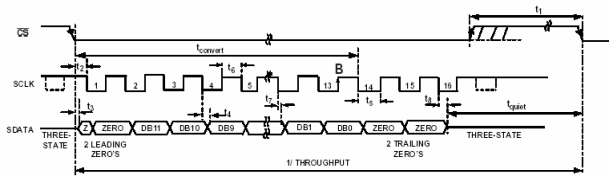


Figure 1. AD7276 Serial Interface Timing Diagram

Refer to the AD7276 data sheet for detailed information about the timing specifications.

## SPI Interface Details

This section discusses the AD7276 interface with SPI of ADSP-21262. The SPI port supports communication with a variety of peripheral devices including codecs, data converters, and sample-rate converters.

The ADSP-21262 SPI is a four-wire interface with two data pins (MOSI - Master Out Slave In, and MISO - Master In Slave Out), one serial clock, and a device select pin. The ADSP-21262 SPI operates in full duplex mode, allowing the processor to transmit and receive data simultaneously on the same port. SPI baud rate, clock polarity, and clock phase are programmable. The DMA capability on the SPI port allows transfers without core overhead.

The ADSP-21262 processor is an SPI master for this interface, supplying a serial bit clock and /CS to the AD7276. The ADSP-21262 receives data on the MISO pin. Refer to Figure 2 for interface details.
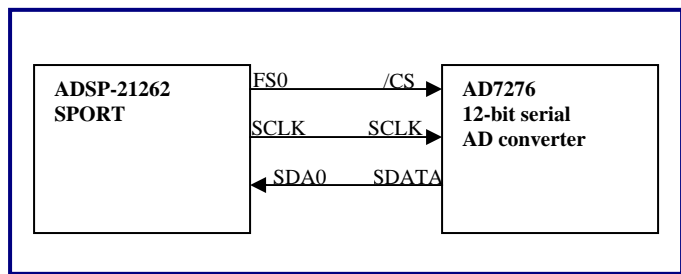


Figure 2. ADSP-21262 SPI Interface with AD7276

The ADSP-21262 SPI to AD7276 interface can be accomplished using CPHASE=0, CLKPL=1 mode as well as CPHASE=1, CLKPL=1 mode. These two modes have been tested with a serial clock frequency of about 12.5 MHz. The advantage of using CPHASE=0 mode over CPHASE=1 mode is that it can be used with the DMA mode of operation. For CPHASE=1 mode, the slave device select (FLAGx) must be asserted and de-asserted manually. When CPHASE=0, the slave device select (/CS for AD7276) is controlled by the SPI hardware; hence, it is automated. The code supplied with this application note includes core mode as well DMA SPI mode.

In both the core and DMA modes of SPI operation, the SPI is configured for a word length of 16 bits by setting the WL16 bit in the SPICTL register.

### CPHASE=0, CLKPL=1 SPI Modes

Core mode as well as DMA SPI mode of operation are possible with CPHASE=0. Refer to Figure 3 for timing information.



Figure 3. CPHASE=0, CLKPL=1 in Core Mode

In CPHASE=0, CLKPL=1 mode, the received word must be right-shifted by 2 bits before being stored in internal memory because the last two bits are zero. The data is driven on the falling edge of the serial clock. The ADSP-21262 SPI samples the data on the serial clock's falling

edges. The data hold time specification of AD7276 makes this scheme possible.

### CPHASE=1, CLKPL=1 SPI modes

With CPHASE=1, only core mode is possible as the device chip select has to be controlled manually. Refer to the Figure 4 for timing information.
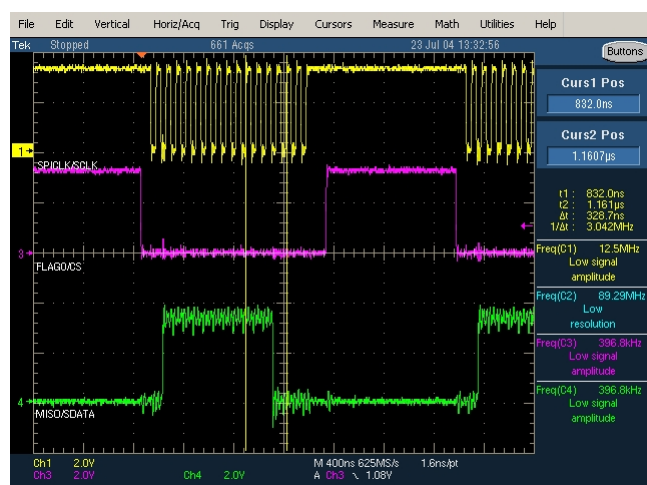


*Figure 4. CPHASE=1, CLKPL=1 in Core Mode*

In CPHASE=1, CLKPL=1 mode, the received word must be right-shifted by 3 bits before being stored in internal memory. Since SPI samples the serial data on the serial clock's rising edges, the second bit latched is *not* the *second* zero bit driven by the ADC; it is the first valid MSB driven by the converter.

## AD7276 Power-Down Mode

AD7276/7277/7278 has a power-down mode for power-sensitive designs, allowing power savings between conversions. To enter power down, the conversion process must be interrupted by bringing /CS high between the SCLK's second falling edge and the $10^{th}$ falling edge. This feature, which is demonstrated in the accompanying code, shows the DMA mode of operation. Inside the DMA completion interrupt, the SPI is configured for a data word length of 8 bits, and a dummy write is performed to ensure that the /CS for AD7276 is brought high before

$10^{th}$ SCLK. This drives the AD7276 into power-down mode.

## SPORT Interface Details

ADSP-2126x processors have up to six independent, synchronous serial ports (SPORTs) that provide an I/O interface to a wide variety of peripheral devices. Each serial port has two bi-directional channels (A and B), configurable as either transmitters or receivers. Each serial port can also be configured as two receivers or two transmitters, permitting two unidirectional streams into or out of the same serial port.

The AD7276 can be interfaced to the ADSP-21262 processor's serial port. The interface can work with both early and late frame syncs. The serial port is configured for internal frame sync and internal serial port clock. Configure the serial port for a 14-bit word length. Potentially, this increases the A/D converter's throughput since it does not have to pad two trailing zero bits at the end of the 12-bit word. Since the SPORT is configured for 14-bit word length, bit shifting is *not* required, unlike in the case of SPI.
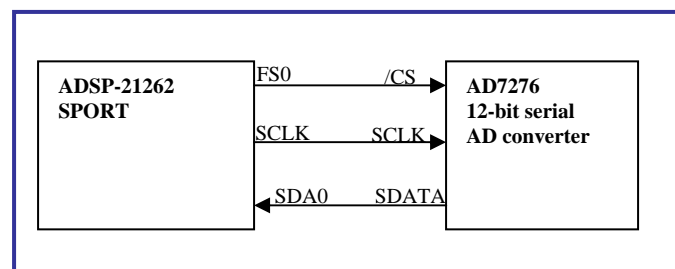


*Figure 5. ADSP-21262 SPORT Interface with AD7276*

The code supplied with this application note includes both early and late frame sync options.

### Early Frame Sync Option

When programmed for an early frame sync option, configure the frame sync as an active high frame sync. Data can be sampled at the serial clock's rising or falling edges. Figure 6 shows timing details in the core mode of

operation. Data is sampled on the clock's rising edges.



Figure 6. SPORT Early Frame Sync Mode

### Late Frame Sync Option

When programmed for late frame sync option, configure the frame sync as an active low frame sync. Data can be sampled at the serial clock's rising or falling edges. Figure 7 shows timing details in the core mode of operation. Again, data is sampled on the clock's rising edges.
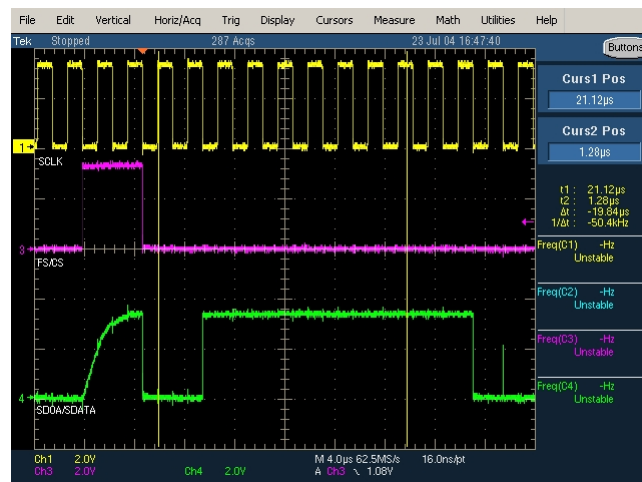


Figure 7. SPORT Late Frame Sync Mode

## Summary

As seen in this application note, you can interface ADSP-21262 and AD7276 gluelessly and use a variety of interface methods and modes.

## Appendix

Refer to the code in the attached ZIP file for various modes of operation.

## References

[1]    *ADSP-21262 DSP Hardware Reference Manual.* Rev 2.0, January 2004. Analog Devices, Inc.

[2]    *AD7276 Preliminary Technical Data Sheet.* Rev PrF, June 2004. Analog Devices, Inc.

[3]    *ADSP-21262 DSP Evaluation System Board Schematics.* Analog Devices, Inc.

## Document History

| Revision | Description |
|---|---|
| *Rev 1 – October 05, 2004*<br>*by Aseem Vasudev Prabhugaonkar* | Initial Release |