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External Port DMA Modes of Operation for SHARC® Processors

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Introduction

This EE-Note describes the External Port DMA modes of operation supported on SHARC® processors. All described modes are supported on ADSP-2106x and ADSP-2116x processors. The ADSP-21367, ADSP-21368, ADSP-21369 (hereafter referred to as ADSP-21368 processors), and ADSP-2137x processors external port supports master mode DMA operation only. These processors do not have the extra logic to support slave mode, paced master mode, or handshake mode. These three modes are possible on ADSP-2106x and ADSP-2116x processors as they have dedicated /DMAR and /DMAG pins.

The example code for master mode and slave mode DMA operation on ADSP-2106x and ADSP-2116x processors and code for master mode DMA operation on ADSP-21368, and ADSP-2137x processors is provided with this EE-Note.

Modes of Operation

The external port DMA transfers the data between the internal memory and external memory/devices connected to the external port without core intervention. The DMA controller must be programmed with the internal memory buffer size and address, the address increment, and the direction of transfer. Once setup programming is complete, DMA transfers begin automatically and continue until the entire buffer is transferred to or from internal memory.

There are five external port DMA modes (Table 1): slave mode, handshake mode, external handshake mode, master mode, and paced master mode. Control bits in the DMACx register select the external port DMA mode.

Mode	Operation	Supported in Processors
Slave	Int Memory <-> DMA Buffer	ADSP-2106x, ADSP-2116x
Master	Int Memory <-> DMA Buffer <-> Ext memory *Uses strobes and address, no /DMAR and /DMAG*	ADSP-2106x, ADSP-2116x, ADSP-21368, ADSP-2137x
Paced Master	Int Memory <-> DMA Buffer <-> Ext memory *Uses /DMAR, strobes and address, no /DMAG*	ADSP-2106x, ADSP-2116x
Handshake	Int Memory <-> DMA Buffer <-> Ext latch/buffer *Uses /DMAR and /DMAG, no strobes and address*	ADSP-2106x, ADSP-2116x
External Handshake	Ext Latch/Buffer <-> Ext Memory *Uses /DMAR, /DMAG, strobes and address*	ADSP-2106x, ADSP-2116x

Table 1. External Port DMA Modes

For ADSP-2106x and ADSP-2116x processors, the MASTER, HSHAKE, and EXTERN bits (Table 2) of each DMACx control register are used to select the DMA mode of operation. Each external port DMA channel can be set up to operate in one of five DMA modes. The master mode initiates transfers while the other modes act as "slaves", where an external device must initiate each transfer.

M	H	E	DMA Mode of Operation
0	0	0	Slave Mode
0	1	0	Handshake Mode
0	1	1	External Handshake Mode
1	0	0	Master Mode
1	1	0	Paced Master Mode

Table 2. MASTER, HSHAKE, and EXTERN bits of DMACx control register for ADSP-2106x and ADSP-2116x processors

All other assignments of the MASTER, HSHAKE, and EXTERN bits (001, 101, 111) are reserved and should not be used.

External Port FIFO Buffers (EPBx)

For ADSP-2106x and ADSP-2116x processors, the external port DMA channels are associated with corresponding external port FIFO data buffers. Each buffer acts as a FIFO. It has two ports: a read port, and a write port. Each port can be connected to the External Port Data (EPD) bus or to a local bus, which in turn can connect to the I/O Data (IOD) bus, PM Data bus, or DM Data bus. This structure allows data to be written to the FIFO on one port while being read from the other port, allowing DMA transfers at the full processor clock frequency. The external port FIFO buffers can also be used for non-DMA, single word data transfers

For ADSP-2106x processors, the DMA channels 6, 7, 8, and 9 are associated with external port FIFO data buffers EPB0, EPB1, EPB2, and EPB3. Each buffer acts as a six-deep FIFO. For ADSP-2116x processors, DMA channels 10, 11, 12, and 13 are associated with external port FIFO data buffers EPB0, EPB1, EPB2, and EPB3. Each buffer acts as an eight-deep FIFO. For ADSP-21368 and ADSP-2137x processors, the DMA controller has a four-deep data FIFO for the received/transmitted data.

External Port DMA Data Packing

The ADSP-2106x external port buffer contains data packing logic to allow 16-bit or 32-bit external bus words to be packed into 32-bit or 48-bit internal words. The packing logic is also fully reversible, so that 32-bit or 48-bit internal data can be unpacked into 16-bit or 32-bit external word widths. The packing mode is selected by the PMODE bits in the DMACx control register for each external port buffer.

For ADSP-2116x processors, the external port buffer contains the data packing logic to pack 8-, 16-, or 32-bit external bus words into 32/64 or 48-bit internal words. The packing logic works in reverse to unpack 32/64-bit data or 48-bit internal data into 8-, 16-, or 32-bit external data.

For ADSP-21368 and ADSP-2137x processors, data packing of 16 to 32 bits or 8 to 32 bits is supported for transfers directly from 32-, 16, or 8-bit-wide external memories to and from internal memory.

ADSP-21065L, ADSP-21161, ADSP-21368, and ADSP-2137x processors have an on-chip SDRAM controller for SDRAM interface. Packing mode also applies to the SDRAM interface.

External Port DMA Channel Registers

The IOP has dedicated channels for the external port DMA. Each external port DMA channel has its own control register and the parameter registers. Table 3 shows the list of the DMA parameter registers.

Register Name	Description
IIx or IIEPx	Internal index register
IMx or IMEPx	Internal modify register
Cx or CEPx	Internal count register
CPx or CPEPx	Chain pointer register
EIx or EIEPx	External index register
EMx or EMEPx	External modify register
ECx or ECEPx	External count register

Table 3. DMA parameter registers

Configuring External Port DMA

DMA operation is programmed by writing to the memory-mapped DMA control registers and parameter registers. The DMA operations can be programmed by the core processor, by an external host processor, or by an external ADSP-2106x/ADSP-2116x bus master. A DMA channel is set up by writing a set of memory buffer parameters to the DMA parameter registers. The `IIx`, `IMx`, and `Cx` registers must be loaded with a starting address for the buffer, an address modifier, and a word count, respectively.

For ADSP-2106x processors, the registers are named `DMAC6` through `DMAC9`, corresponding to DMA channels six through nine. For ADSP-21061 processors, only channels six and seven are applicable for external port DMA. For ADSP-2116x processors, the registers are named `DMAC10` through `DMAC13`, corresponding to DMA channels ten through thirteen. For ADSP-21368 and ADSP-2137x processors, the registers are named `DMAC0` and `DMAC1`.

Slave Mode

When a particular DMA channel is configured as a slave, this particular DMA channel cannot initiate external memory transfers independently, regardless of the programmed direction of data transfer. The `TRAN` bit of the `DMACx` control register determines the direction of the data transfer. In a slave configuration, the external host device can write directly to the SHARC processor's external port buffer.

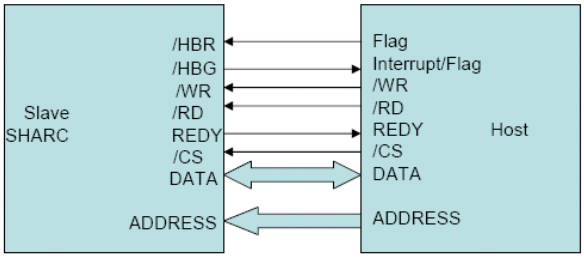

Figure 1. Example: slave mode configuration

For an external device to transfer a block of data to a SHARC processor's internal memory, the host would write to the DMA channel parameter registers (`IIx`, `IMx`, and `Cx`) and to the `DMACx` control register to initialize the channel. Then the device would begin writing data to the `EPBx` buffer, monitoring the status of the `REDY` signal (for asynchronous, host-driven accesses) or the `ACK` signal (for synchronous accesses) of the SHARC processor in case of a DMA hold-off. A hold-off occurs when the `EPBx` FIFO becomes full. For the buffer to operate in this fashion, the `BHD` (Buffer Hang Disable) bit must be cleared in the `SYSCON` register. Figure 1 shows an example of a slave mode configuration system between a host processor and a SHARC processor.

The same holds true for host reads in slave mode.

If internal DMA transfers cannot fill the `EPBx` FIFO buffer at the same rate as the external device empties it, the external device will be held off with the `REDY` signal (for asynchronous, host-driven accesses) or the `ACK` signal (for synchronous accesses). Again, for the buffer to operate in this fashion, the `BHD` bit must be cleared in the `SYSCON` register. This mode applies to ADSP-2106x and ADSP-2116x processors.

The slave mode example code associated with this EE-Note demonstrates the slave mode DMA operation in a multiprocessor system. The

example code is provided for the slave write DMA cases and the slave read DMA case. For both cases, one processor acts as the master and the other processor acts as the slave. For the slave write DMA test case, the slave processor is configured for slave mode DMA to transfer data from internal memory; the master processor reads the data from the slave processor's EPBx buffer. For the slave read DMA test case, the slave processor is configured for slave mode DMA to copy the data to the internal memory; the master processor writes the data to the slave processor's EPBx buffer. The code uses DMA chaining mode to transfer the data.

Master Mode

When a DMA channel is configured to operate in master mode, the processor's DMA controller will generate internal DMA requests for this channel until the DMA sequence is completed. Master mode can be specified independently for each external port DMA channel. In this configuration, the processor asserts the appropriate external address and /RD and /WR strobes, but does not use the /DMARx and /DMAGx signals.

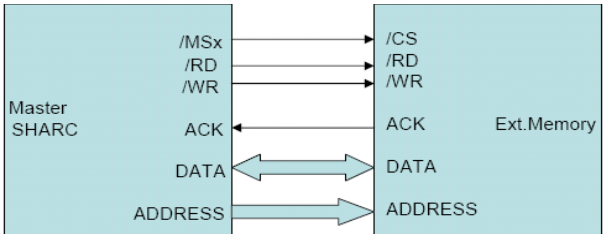

Figure 2. Example: master mode configuration with external memory

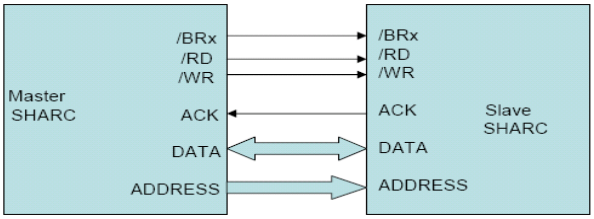

Figure 3. Example: master mode configuration in a multiprocessor system

In a multiprocessor environment, the most efficient method (i.e., for maximum throughput) requires the master/slave DMA mode. This configuration allows for a 1-cycle/transfer data throughput rate. Another advantage is that the slave generates an interrupt automatically upon completion of the DMA transfer. The disadvantage is that both the master and slave must be programmed for the appropriate DMA transfer. Figure 2 shows an example master mode configuration between a SHARC processor and external memory. This mode of operation applies to all ADSP-2106x, ADSP-2116x, ADSP-21368, and ADSP-2137x processors. Figure 3 shows an example master mode configuration between two SHARC processors. This mode of operation is applies only to ADSP-2106x and ADSP-2116x processors.

The master mode example code associated with this EE-Note demonstrates master mode DMA operation between the processor and an external memory. The processor core initiates the DMA transfer by configuring the DMACx and DMA parameter registers. Once DMA is started, the data will be transferred automatically between internal memory and external memory.

Handshake Mode

On ADSP-21060 and ADSP-21062 processors, each of DMA channels 7 and 8 (for external port buffers EPB1 and EPB2) has a set of external handshake controls. /DMAR1 and /DMAG1 are the request and grant signals for EPB1 and channel 7, and /DMAR2 and /DMAG2 are the request and grant signals for EPB2 and channel 8.

On ADSP-21061 processors, each of DMA channels 7 and 6 (for external port buffers EPB1 and EPB0) has a set of external handshake controls. /DMAR1 and /DMAG1 are the request and grant signals for EPB1 and channel 7, and /DMAR2 and /DMAG2 are the request and grant signals for EPB0 and channel 6.

On ADSP-21065L processors, each of DMA channels 8 and 9 (for external port buffers EPB0 and EPB1) has a set of external handshake controls. /DMAR1 and /DMAG1 are the request and grant signals for EPB0 and channel 8, and /DMAR2 and /DMAG2 are the request and grant signals for EPB1 and channel 9.

On ADSP-2116x processors, each of DMA channels 11 and 12 (for external port buffers EPB1 and EPB2) has a set of external handshake controls. /DMAR1 and /DMAG1 are the request and grant signals for EPB1 and channel 11, and /DMAR2 and /DMAG2 are the request and grant signals for EPB2 and channel 12.

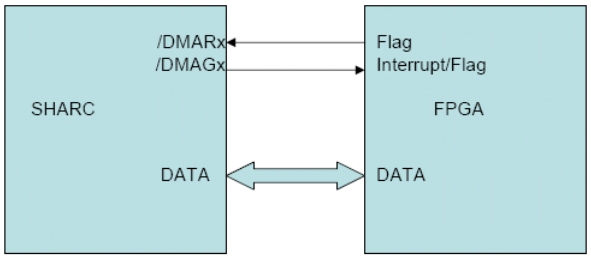

Figure 4. Example: handshake mode configuration

If an external port DMA channel is enabled and handshake signals are not used, keep the corresponding /DMARx signal high.

These signals facilitate a hardware handshake between the processor and an external device that does not have bus mastership capability.

To request an access of the EPBx buffer, the external device pulls /DMARx low. When the processor recognizes the request, it begins to arbitrate for the external bus (if it is not already the bus master). When it becomes the bus master, it drives /DMAGx low. The processor keeps /DMAGx asserted until /DMARx is deasserted. This allows the external device to hold the processor until it is ready to proceed. Figure 4 shows an example handshake mode configuration between a SHARC processor and a "smart" external device such as an FPGA. This mode applies only to ADSP-2106x and ADSP-2116x processors.

External Handshake Mode

External devices can use the /DMARx and /DMAGx handshake signals to control DMA transfers between an external device and external memory. In this mode, the processor operates as an independent DMA controller.

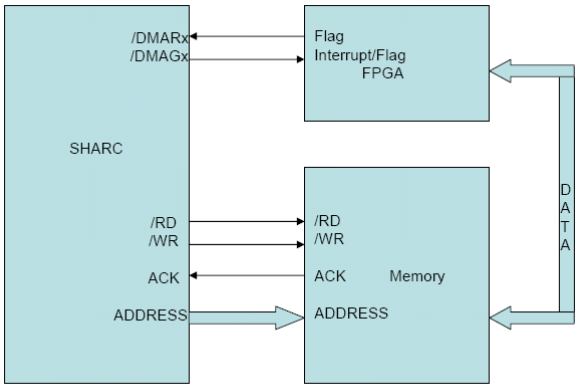

Figure 5. Example: external handshake mode configuration

External handshake mode transfers require the processor's DMA controller to generate external memory access cycles. /DMARx and /DMAGx retain the same functionality in this mode, but instead of simply generating /DMAGx, the processor also outputs addresses, memory selects (/MS3-0), /RD and /WR strobes. The processor also responds to ACK. /DMAGx will be held low until ACK is released or any wait states are completed.

The processor's EPBx buffers do not latch or drive data, and no internal memory DMA transfers are performed. The EI, EM, and EC registers of the DMA channel must be preloaded to generate the external memory addresses and word count.

For example, let's say your system design has an FPGA, external RAM, and a SHARC processor configured for external handshake mode. The

/DMARx and /DMAGx signals would be connected between the processor and the FPGA, and the data bus would be connected between the FPGA and the memory device. The processor would communicate with the memory device using the address bus, /RD and /WR signals, and possibly the ACK signal (if wait states are needed or to hold off the processor). Figure 5 shows external handshake mode for a SHARC processor, external memory, and an FPGA. Note that external handshake mode cannot be used for SDRAM memory accesses by an external device. This mode applies only to ADSP-2106x and ADSP-2116x processors.

Paced Master Mode

In paced master mode, /DMARx requests operate the same way as in handshake mode, but /DMAGx is not active. The processor responds to requests only with the /RD and /WR strobes. In this configuration, an external device such as an FPGA asserts the /DMARx signal, allowing the SHARC processor access to the external bus only when the FPGA is ready.

Paced master mode gets its name from the fact that an external device (which also has control over the external bus) can hold off the processor from the bus only when it is ready for a DMA transfer from the processor. This differs from master mode, because in master mode the processor is *always* in control of the external bus. Paced master mode accesses can be extended by the ACK pin, by wait states programmed in the WAIT register, and by holding the /DMARx pin low.

Figure 6 shows an example of a paced master mode configuration in which an FPGA controls the DMA accesses and the SHARC processor has control of the system bus. This mode applies only to ADSP-2106x and ADSP-2116x processors.

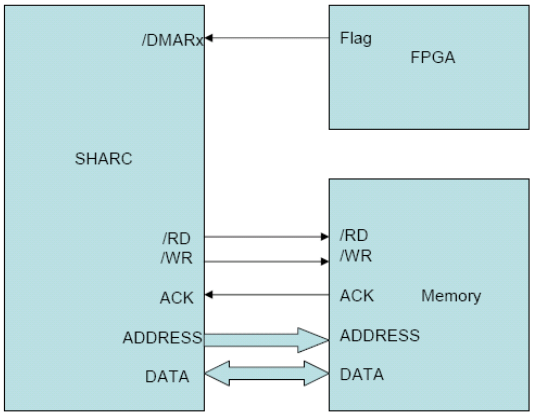

Figure 6. Example: paced master mode configuration

Interfacing AD7865 Parallel ADCs to ADSP-21161 SHARC Processors (EE-259)[6] discusses the parallel ADC interface to the external port of the ADSP-21161 processors using paced master mode. Refer to this document for details.

Summary

This EE-Note discusses the external port DMA modes of operation supported on the ADSP-2106x, ADSP-2116x, ADSP-21368, and ADSP-2137x processors. Example code is provided to demonstrate the master and slave modes of DMA operation.

References

[1] *ADSP-2106x SHARC Processor User's Manual.* Rev 2.1, March 2004. Analog Devices, Inc.

[2] *ADSP-21065L SHARC Processor User's Manual.* Rev 2.0, July 2003. Analog Devices, Inc.

[3] *ADSP-21160 SHARC Processor Hardware Reference.* Rev 3.0, November 2003. Analog Devices, Inc.

[4] *ADSP-21161 SHARC Processor Hardware Reference.* Rev 4.0, February 2005. Analog Devices, Inc.

[5] *ADSP-21368 SHARC Processor Hardware Reference.* Rev 1.0, September 2006. Analog Devices, Inc.

[6] *Interfacing AD7865 Parallel ADCs to ADSP-21161 SHARC Processors (EE-259),* Rev. 1.0, December 2004, Analog Devices Inc.

Document History

Revision	Description
Rev 2 – February 28, 2007 *by P. Mallikarjun Reddy and Jeyanthi Jegadeesan*	Generalized the document for the ADSP-2106x, ADSP-2116x, ADSP-21368 and ADSP-2137x processors.
Rev 1 – March 16, 1998 *Greg Fowler*	Initial release for ADSP-2106x processors.