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Estimating Power for ADSP-214xx SHARC® Processors

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Introduction

This EE-Note discusses power consumption of ADSP-214xx SHARC® processors based on characterization data measured over power supply voltage, core frequency (CCLK), and junction temperature (T_J). The intent of this document is to assist board designers in estimating their power budget for power supply and thermal relief designs using ADSP-214xx processors.

Furthermore, the associated .ZIP file contains spreadsheets for ADSP-2146x, ADSP-2147x, and ADSP-2148x processors, all aimed to assist in power estimation. The accompanying spreadsheets allow users to enter their application-specific operating conditions and system-level utilization of resources, and use these inputs to calculate the total power consumed by the processor.

The ADSP-214xx family of processors is member of the SIMD (single instruction multiple data) SHARC family of processors, featuring the Analog Devices Super Harvard architecture and an enhanced SIMD VISA (variable instruction size architecture) core. Like other SHARC processors, they are 32-bit floating-point processors optimized for high-precision signal processing applications. They also contain dedicated hardware units for performing FIR (finite impulse response), IIR (infinite impulse response), and FFT (fast Fourier transform) algorithms without any core intervention, thereby providing an efficient saving of core MIPs.

ADSP-2146x processors are offered in the commercial temperature range at core clock frequencies of up to 450 MHz, core operating voltage of 1.1V (V_{DD_INT}), a DDR2 (dual data RAM) voltage of 1.8 V (V_{DD_DDR2}), and at an I/O voltage of 3.3 V (V_{DD_EXT}). They are also offered in automotive and industrial temperature ranges at core clock frequencies of up to 400 MHz, core operating voltage of 1.05 V (V_{DD_INT}), DDR2 voltage of 1.8 V (V_{DD_DDR2}), and I/O voltage of 3.3 V (V_{DD_EXT}). For specific information regarding operating temperature ranges and part numbers, refer to the processor data sheet[0].

ADSP-2147x processors are offered in the commercial, industrial and automotive temperature range at core clock frequencies of up to 300 MHz, core operating voltage of 1.2V (V_{DD_INT}), and at an I/O voltage of 3.3 V (V_{DD_EXT}). For specific information regarding operating temperature ranges and part numbers, refer to the processor data sheet[0].

ADSP-2148x processors are offered in the commercial, industrial and automotive temperature range at core clock frequencies of up to 400 MHz, core operating voltage of 1.1V(V_{DD_INT}), and at an I/O voltage of 3.3 V (V_{DD_EXT}). For specific information regarding operating temperature ranges and part numbers, refer to the processor data sheet[0].

The total power consumption of the ADSP-214xx processors can be viewed as the sum of the power consumed for all of the power supply domains (V_{DD_INT}, V_{DD_EXT}, and V_{DD_DDR2} – DDR2

supply applicable only for ADSP-2146x processors). The total power consumption has two components: one due to internal circuitry (i.e., the core and the PLL), and the other due to the switching of external output drivers (such as DDR2 DRAM/SDRAM and I/O).

The following sections detail how to derive both of these components for estimating total power consumption, based on different dynamic activity levels, I/O activity, power supply settings, core frequencies, and environmental conditions.

Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the V_{DD_INT} supply) is the sum of the static power component and dynamic power component of the processor's core logic.

The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

The dynamic portion of the internal power is dependent on the instruction execution sequence, the data operands involved, and the instruction rate.

Refer to the corresponding processor data sheet for static as well as baseline dynamic current consumption figures.

The following section describes scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for an ADSP-214xx processor in a given application.

Internal Power Vector Definitions and Activity Levels

The following power vector definitions explain the dynamic activity levels that apply to the internal power vectors for ADSP-214xx processors. The dynamic activity levels correspond to ADSP-2146x, ADSP-2147x and ADSP-2148x processors are shown in Table 1, Table 2, and Table 3 respectively.

- $I_{DD\text{-}IDLE}$ V_{DD_INT} supply current for idle activity. Idle activity is the core executing the `IDLE` instruction only, with no core memory accesses, no DMA (direct memory access), and no interrupts.
- $I_{DD\text{-}INLOW}$ V_{DD_INT} supply current for low activity. Low activity is the core executing a single-function instruction fetched from internal memory, with no core memory accesses, no DMA, and no activity on the external port.
- $I_{DD\text{-}INMEDIUMLOW}$ V_{DD_INT} supply current for low activity. Medium low activity is the core executing a multi-function instruction fetched from internal memory, with no core memory accesses, no DMA, and no activity on the external port.
- $I_{DD\text{-}INMEDIUMHIGH}$ V_{DD_INT} supply current for medium high activity. Medium high activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 4 core memory accesses per `CLKIN` cycle (based on a `CLKCFG1-0` setting of 16:1 and DMx64 [i.e., long word accesses on DM bus]) and DMA through three SPORTs (Serial Ports) running at an eighth of the core clock frequency, AMI (Asynchronous Memory Interface) DMA data transfers with two wait states at one-sixth of the core clock frequency, and one SPI (Serial Peripheral Interface) DMA at one sixty-fourth of the core clock frequency. The DMAs are chained to themselves (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random. There are also two channels of IIR

filter running in the background on the dedicated IIR hardware accelerator unit.

- $I_{DD\text{-}INHIGHTYPICAL}$ V_{DD_INT} supply current for high typical activity. High typical activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 12 core memory accesses per `CLKIN` cycle (based on a `CLKCFG1-0` setting of 16:1 and DMx64 [i.e., long word accesses on DM bus]) and DMA through three SPORTs (Serial Ports) running at an eighth of the core clock frequency, AMI (Asynchronous Memory Interface) DMA data transfers with two wait states at one-sixth of the core clock frequency, and one SPI (Serial Peripheral Interface) DMA at one sixty-fourth of the core clock frequency. The DMAs are chained to themselves (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random. There are also two channels of IIR filter running in the background on the dedicated IIR hardware accelerator unit.
- $I_{DD\text{-}INHIGH}$ V_{DD_INT} supply current for high activity. High activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 16 core memory accesses per `CLKIN` cycle (based on a `CLKCFG1-0` setting of 16:1 and DMx64 [i.e., long word accesses on DM bus]) and DMA through three SPORTs (Serial Ports) running at an eighth of the core clock frequency, AMI (Asynchronous Memory Interface) DMA data transfers with two wait states at one-sixth of the core clock frequency, and one SPI (Serial Peripheral Interface) DMA at one sixty-fourth of the core clock frequency. The DMAs are chained to themselves (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random. There are also two channels of IIR filter running in the background on the dedicated IIR hardware accelerator unit.
- $I_{DD\text{-}INPEAK}$ V_{DD_INT} supply current for peak activity. Peak activity is the core, executing a multi-function instruction fetched from internal memory and/or cache, with 32 core memory accesses per `CLKIN` cycle (based on a `CLKFG1-0` setting of 16:1 and DMx64, PMx64 [i.e., long word accesses simultaneously occurring on both DM and PM buses]), DMA through six SPORTs running at one eighth of the core clock frequency, SPI DMA based transfers occurring on two SPIs running at one eighth of the core clock frequency, AMI DMA data transfers with two wait states, one UART DMA at 1/32 of the core . Also, there are two PCGs (Precision Clock Generators) running at one sixteenth of the core frequency, and four SRCs (Sample Rate Converters) running at one eighth of the core frequency. All DMAs are chained to themselves (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random. In addition, there are also three channels of FIR filter running in the background on the dedicated FIR hardware accelerator unit.

  

  The test code used to measure $I_{DD\text{-}INPEAK}$ represents worst-case operation. This activity level is not sustainable under normal application conditions.

- $I_{DD\text{-}INPEAK\text{-}TYP}$ V_{DD_INT} supply current for *typical* peak activity. *Typical* peak activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 32 core memory accesses per `CLKIN` cycle

(DMx64, PMx64), DMA through six SPORTs running at one-eighth of the core frequency, DMA through one SPI running at one four-hundredth of the core frequency, and external memory accesses at maximum data rate. For ADSP-2146x processors, this will be 225 MHz clock / 450 MHz data rate, for ADSP-2147x it will be 133Mhz data rate, while for ADSP-2148x processors, it will be 160 MHz data rate. The bit pattern for each core memory access and DMA and external memory (DDR2 SDRAM/SDR SDRAM) access is random. The external memory (DDR2 SDRAM/SDR SDRAM) read-to-write access ratio is 60:40. Three different scenarios are covered in terms of the ratio of continuous instruction loop to external memory (DDR2 SDRAM/SDR SDRAM) control code: 70% reads with 30% writes, 50% reads with 50% writes, and 60% reads with 40% writes.

Operation	**Idle**	**Low**	**High**	**Peak**	**Peak (Typical)**
Instruction Type	IDLE	Single-function	Multi-function	Multi-function	Multi-function
Instruction Fetch	Int Memory	Int Memory	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache
Core Memory Access[1]	None	None	16 per t_{CK} cycle[2]	32 per t_{CK} cycle[3]	32 per t_{CK} cycle[3]
Ext Port:	DDR2_CLK0 only	DDR2_CLK0 only	225/450 MHz	225/450 MHz	225/450 MHz
AMI/DDR2	N/A	N/A	Wait-state = 2	Wait-state = 2	Different RD/WR ratios
SPORTs	N/A	N/A	3 @ 1/8*CCLK	6 @ 1/8*CCLK	6 @ 1/8*CCLK
SPI	N/A	N/A	1 @ 1/64*CCLK	2 @ 1/8*CCLK	1 @ 1/400*CCLK
MediaLB I/F	N/A	N/A	N/A	1024 Fs	N/A
UART	N/A	N/A	N/A	1 @ 1/32*CCLK	N/A
PCG	N/A	N/A	N/A	2 @ 1/16*CCLK	N/A
SRC	N/A	N/A	N/A	4 @ 1/8*CCLK	N/A
FIR HW Unit	N/A	N/A	N/A	3 channels	N/A
IIR HW Unit	N/A	N/A	2 channels	N/A	N/A
Data Bit Pattern for Core Memory Access and DMA	N/A	N/A	Random	Random	Random
Ratio – Continuous Instruction Loop to DDR2 DRAM Control code	N/A	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	50:50 60:40 70:30

Table 1. Dynamic activity level definitions for ADSP-2146x processors

1 t_{CK} = CLKIN; Core clock ratio 16:1
2 DMx64 Access
3 DMx64 Access, PMx64 Access

Operation	Idle	Low	Medium Low	Medium High	High Typical	High	Peak	Peak (Typical)
Instruction Type	IDLE	Single-function	Multi-function	Multi-function	Multi-function	Multi-function	Multi-function	Multi-function
Instruction Fetch	Int Memory	Int Memory	Int Memory	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache
Core Memory Access[1]	None	None	None	4 per t_{CK} cycle[2]	12 per t_{CK} cycle[2]	16 per t_{CK} cycle[2]	32 per t_{CK} cycle[3]	32 per t_{CK} cycle[3]
Ext Port: SDRAM	SDCLK only	SDCLK only	SDCLK only	133 MHz / 266 MHz	133 MHz / 266 MHz	133 MHz / 266 MHz	133 MHz / 266 MHz	133 MHz / 266 MHz, RD/WR ratios – 60:40
AMI	N/A	N/A	N/A	Wait-state = 2	Wait-state = 2	Wait-state = 2	Wait-state = 2	N/A
SPORTs	N/A	N/A	N/A	3 @ 1/8*CCLK	3 @ 1/8*CCLK	3 @ 1/8*CCLK	6 @ 1/8*CCLK	6 @ 1/8*CCLK
SPI	N/A	N/A	N/A	1 @ 1/64*CCLK	1 @ 1/64*CCLK	1 @ 1/64*CCLK	2@ 1/8*CCLK	1 @ 1/400*CCLK
Media LB I/F	N/A	N/A	N/A	N/A	N/A	N/A	1024 Fs	N/A
UART	N/A	N/A	N/A	N/A	N/A	N/A	1 @ 1/32*CCLK	N/A
PCG	N/A	N/A	N/A	N/A	N/A	N/A	2 @ 1/16*CCLK	N/A
SRC	N/A	N/A	N/A	N/A	N/A	N/A	4 @ 1/8*CCLK	N/A
FIR HW Unit	N/A	N/A	N/A	N/A	N/A	N/A	3 channels	N/A
IIR HW Unit	N/A	N/A	N/A	2 channels	2 channels	2 channels	N/A	N/A
Data Bit Pattern for Core Memory Access and DMA	N/A	N/A	N/A	Random	Random	Random	Random	Random
Ratio – Continuous Instruction Loop to SDRAM Control code	N/A	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	50:50 60:40 70:30

Table 2. Dynamic activity level definitions for ADSP-2147x processors

1 t_{CK} = CLKIN; Core clock ratio 16:1
2 DMx64 Access
3 DMx64 Access, PMx64 Access

Operation	Idle	Low	Medium Low	Medium High	High Typical	High	Peak	Peak (Typical)
Instruction Type	IDLE	Single-function	Multi-function	Multi-function	Multi-function	Multi-function	Multi-function	Multi-function
Instruction Fetch	Int Memory	Int Memory	Int Memory	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache
Core Memory Access[1]	None	None	None	4 per t_{CK} cycle[2]	12 per t_{CK} cycle[2]	16 per t_{CK} cycle[2]	32 per t_{CK} cycle[3]	32 per t_{CK} cycle[3]
Ext Port: SDRAM	SDCLK only	SDCLK only	SDCLK only	160 MHz / 400 MHz	160 MHz / 400 MHz	160 MHz / 400 MHz	160 MHz / 400 MHz	160 MHz / 400 MHz, RD/WR ratios – 60:40
AMI	N/A	N/A	N/A	Wait-state = 2	Wait-state = 2	Wait-state = 2	Wait-state = 2	N/A
SPORTs	N/A	N/A	N/A	3 @ 1/8*CCLK	3 @ 1/8*CCLK	3 @ 1/8*CCLK	6 @ 1/8*CCLK	6 @ 1/8*CCLK
SPI	N/A	N/A	N/A	1 @ 1/64*CCLK	1 @ 1/64*CCLK	1 @ 1/64*CCLK	2@ 1/8*CCLK	1 @ 1/400*CCLK
Media LB I/F	N/A	N/A	N/A	N/A	N/A	N/A	1024 Fs	N/A
UART	N/A	N/A	N/A	N/A	N/A	N/A	1 @ 1/32*CCLK	N/A
PCG	N/A	N/A	N/A	N/A	N/A	N/A	2 @ 1/16*CCLK	N/A
SRC	N/A	N/A	N/A	N/A	N/A	N/A	4 @ 1/8*CCLK	N/A
FIR HW Unit	N/A	N/A	N/A	N/A	N/A	N/A	3 channels	N/A
IIR HW Unit	N/A	N/A	N/A	2 channels	2 channels	2 channels	N/A	N/A
Data Bit Pattern for Core Memory Access and DMA	N/A	N/A	N/A	Random	Random	Random	Random	Random
Ratio – Continuous Instruction Loop to SDRAM Control code	N/A	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	50:50 60:40 70:30

Table 3. Dynamic activity level definitions for ADSP-2148x processors

1 t_{CK} = CLKIN; Core clock ratio 16:1
2 DMx64 Access
3 DMx64 Access, PMx64 Access

Estimating Internal Dynamic Current, $I_{DD\text{-}DYN}$

Two steps are involved in estimating the dynamic power consumption due to the internal circuitry (i.e., on the V_{DD_INT} supply).

The first step is to determine the dynamic baseline current under the application's operating conditions, and the second step is to determine the fraction of time the application spends performing each type of activity corresponding to each discrete power vector specified above, with respect to the entire application.

The baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for ADSP-214xx processors can be determined from the "*Baseline Dynamic Current in CCLK Domain*" table in the processor data sheet. Note that the $I_{DD\_BASELINE\_DYN}$ current corresponds to $I_{DD\text{-}INPEAK\text{-}TYP}$ dynamic activity level 70:30, measured as a function of core frequency. Each entry in the table represents a baseline I_{DDINT} dynamic current for a given power supply setting.

From the table, the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for the V_{DD_INT} power supply domain can be estimated at the operating frequency of the processor in the application. For example, for ADSP-2146x processors operating at a core voltage of 1.10 V (V_{DD_INT}) and a core frequency of 450 MHz, the corresponding baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) comes out to be approximately 0.385 A.

I_{DD} Dynamic Current for a specific Application

The "Activity Scaling Factor (ASF)" data for ADSP-214xx processors at each activity level is used to estimate the dynamic current for each specific application. This information is also available in the processor datasheet. With knowledge of the program flow and an estimate of the fraction of an application's time spent at each activity level, the system developer can use the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) derived from the previous section and the corresponding activity scaling factor from the processor datasheet determine the dynamic portion of the internal current ($I_{DD\text{-}DYN}$) for each ADSP-214xx processor in a system.

The ADSP-214xx dynamic current consumption in a specific application is calculated according to the following formula, where "%" is the percentage of the overall time that the application spends in that state:

(% *Peak Typical activity level* x $I_{DD\text{-}INPEAK\text{-}TYP}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+ (% *Peak activity level* x $I_{DD\text{-}INPEAK}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+ (% *High activity level* x $I_{DD\text{-}INHIGH}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+ (% *HighTypical activity level* x $I_{DD\text{-}INHIGHTYPICAL}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+ (% Medium *High activity level* x $I_{DD\text{-}INMEDIUMHIGH}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+ (% Medium Low *activity level* x $I_{DD\text{-}INMEDIUMLOW}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+ (% *Low activity level* x $I_{DD\text{-}INLOW}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+(% *Idle activity level* x $I_{DD\text{-}IDLE}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)

= *Total Dynamic Current for* V_{DD_INT} (I_{DD_DYN})

Equation 1. Internal dynamic current ($I_{DD\text{-}DYN}$)

If, for example, after profiling the application code for a particular system, it is determined that half of the time the processor is spent performing "peak" activity, 40% of the time spent in "peak typical" activity, and 10% of the time is spent in "low" activity, then the application's $I_{DD\text{-}DYN}$ is calculated as follows:

(0% High Activity Level)
+ (50% Peak Activity Level)
+ (40% Peak Typical Activity Level)
+ (0% High Typical Activity Level)
+ (0% Medium High Activity Level)
+ (0% Medium Low Activity Level)
+ (10% Low Activity Level)
+ (0% Idle Activity Level)

= *Total Dynamic Current for* V_{DD_INT} (I_{DD_DYN})

Equation 2. $I_{DD\text{-}DYN}$ for specific application

For ADSP-2146x processors, using the activity scaling factor (*ASF*) provided for each activity level in the processor data sheet, and the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for the core operating at 1.1 V (V_{DDINT}), and a core frequency of 450 MHz) as 0.385A, the value for the dynamic portion of the internal current consumption of a single processor can be estimated to be as follows:

*(50% **x 1.35 x** 0.385)*
*+ (40% **x 1.00 x** 0.385)*
*+ (10% **x 0.58 x** 0.385)*

$I_{DD\text{-}DYN}$ = *0.436 A*

Equation 3. Internal dynamic current estimation

Thus, the total estimated dynamic current on the V_{DD_INT} power supply in this example is 0.436 A.

For ADSP-2147x processors, using the activity scaling factor (*ASF*) provided for each activity level in the processor data sheet, and the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for the core operating at 1.2 V (V_{DDINT}), and a core frequency of 266 MHz as 0.225A, the value for the dynamic portion of the internal current consumption of a single processor can be estimated to be:

*(50% **x 1.34 x** 0.225)*
*+ (40% **x 1.00 x** 0.225)*
*+ (10% **x 0.53 x** 0.225)*

$I_{DD\text{-}DYN}$ = *0.252 A*

Equation 4. Internal dynamic current estimation for ADSP-2147x processors

Thus, the total estimated dynamic current on the V_{DD_INT} power supply in this example is 0.252 A for ADSP-2147x processors.

For ADSP-2148x processors, using the activity scaling factor (*ASF*) provided for each activity level in the processor data sheet, and the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for the core operating at 1.1 V (V_{DDINT}), and a core frequency of 400 MHz as 0.344A, the value for the dynamic portion of the internal current consumption of a single processor can be estimated to be as follows:

*(50% **x 1.31 x** 0.344)*
*+ (40% **x 1.00 x** 0.344)*
*+ (10% **x 0.53 x** 0.344)*

$I_{DD\text{-}DYN}$ = *0.381 A*

Equation 5. Internal dynamic current estimation for ADSP-2148x processors

Thus, the total estimated dynamic current on the V_{DD_INT} power supply in this example is 0.381 A for ADSP-2148x processors.

Estimating Internal Static Current, $I_{DD\text{-}STATIC}$

The $I_{DD\text{-}STATIC}$ current tables for ADSP-214xx processors are found in the processor data sheets. The static current on the V_{DD_INT} power supply domain is a function of temperature and voltage, but *not* a function of frequency or activity level.

Therefore, unlike the dynamic portion of the internal current, the static current does not need to be calculated for each discrete activity level or power vector. Using the static current table corresponding to the application (i.e., at the specific V_{DD_INT}), the baseline static current ($I_{DD\text{-}STATIC}$) can be estimated versus junction temperature (T_J) of the ADSP-214xx processor.

Estimating Total I_{DDINT} Current

The total current consumption due to the internal core circuitry (I_{DDINT}) is the sum of the dynamic current component and the static current component as shown in Equation 6:

$$I_{DDINT} = I_{DD\text{-}DYN} + I_{DD\text{-}STATIC}$$

Equation 6. Internal core current (I_{DDINT}) calculation

For ADSP-2146x processor operating at 1.10 V and core frequency of 450 MHz, with the code as profiled, assume that the resulting junction temperature (T_J) is estimated to be +45°C. The total internal current consumed by the processor core under these conditions would then be:

$$I_{DDINT} = 0.436 + 0.428 = 0.864 \text{ A}$$

Equation 7. Total internal core current estimation for ADSP-2146x processors

For the ADSP-2147x processor operating at 1.20 V and core frequency of 266 MHz, with the code as profiled, assume that the resulting junction temperature (T_J) is estimated to be +45°C. The total internal current consumed by the core under these conditions would then be:

$$I_{DDINT} = 0.252 + 0.005 = 0.258 \text{ A}$$

Equation 8. Total internal core current estimation for ADSP-2147x processors

For the ADSP-2148x processor operating at 1.10 V and core frequency of 400 MHz, and with the code as profiled, assume that the resulting junction temperature (T_J) is estimated to be +45°C. The total internal current consumed by the processor core under these conditions would then be:

I_{DDINT} = 0.381 + 0.389 = 0.770 A

Equation 9. Total internal core current estimation for ADSP-2148x processors

Total Estimated Internal Power, P_{DDINT}

The resulting internal power consumption (P_{DDINT}) is given by Equation 10:

$P_{DDINT} = V_{DDINT} \ x \ I_{DDINT}$

Equation 10. Internal power (P_{DDINT}) calculation

Using Equation 10, the total estimated internal power consumed by the ADSP-2146x processor in the application described in this example would be:

P_{DDINT} = 1.10 V x 0.864 A = 0.95 W

Applying Equation 10, the total estimated internal power consumed by the ADSP-2147x processor in the application described in this example would be:

P_{DDINT} = 1.20 V x 0.258 A = 0.310 W

Using Equation 10, the total estimated internal power consumed by the ADSP-2148x processor in the application described in this example would be:

P_{DDINT} = 1.10 V x 0.770 A = 0.847 W

Estimating External Power Consumption

The external power consumption is dependent on the switching of the output pins. For ADSP-2146x processors, it includes the switching in V_{DD_DDR2} and V_{DD_EXT} supply domains. For ADSP-2147x and ADSP-2148x processors, it includes the switching in V_{DD_EXT} supply domain. The magnitude of the external power depends on:

- The number of output pins that switch during each cycle, O
- The maximum frequency at which the output pins can switch, f
- The voltage swing of the output pins, V_{DD_DDR2} or V_{DD_EXT}
- The load capacitance of the output pins, C_L

In addition to the input capacitance of each device connected to an output, the total load capacitance should include the capacitance (C_{OUT}) of the processor pin itself, which is driving the load.

Equation 11 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

$I_{DDEXT} = O \ x \ f \ x \ V_{DD} \ x \ C_L$

Equation 11. External current calculation

Where, $V_{DD} = V_{DD\_DDR2}$ or V_{DD_EXT}.

The estimated average external power consumption (P_{DDEXT}) can be calculated as follows:

$P_{DDEXT} = V_{DD\_DDR2} \ x \ I_{DD\_DDR2} + V_{DD\_EXT} \ x \ I_{DD\_EXT}$

Equation 12. External power (P_{DDEXT}) calculation for ADSP-2146x processors

$P_{DDEXT} = V_{DD\_EXT} \ x \ I_{DD\_EXT}$

Equation 13. External power (P_{DDEXT}) calculation for ADSP-2147x and ADSP-2148x processors

External power consumption for ADSP-2146x processors

For the system in Figure 1, we can estimate the external current and thereby the external power consumption with the following assumptions:

- Processor core running at 450 MHz (CCLK)
- 64M x 16-bit external DDR2 memory, C_L = 10 pF (trace capacitance ignored). During external memory writes, 50% of the ADDR23-0 and DATA15-0 pins are switching
- DAI configured as SPORT transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- DPI configured as SPI master transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- Output capacitance of processor pin, C_{OUT} = 5 pF

For the purpose of this example, it is assumed that the ADSP-2146x processor's DDR2 controller is running at the maximum specified speed of 225 MHz clock. The switching frequency is quite high for a typical application, and is provided here merely to illustrate a worst-case calculation. In addition to DDR2, it is also assumed that one serial port (SPORT) and one serial peripheral interface (SPI) are running at one-eighth (1/8) the processor core clock rate (CCLK). With a core clock of 450 MHz, this corresponds to a maximum switching frequency of 28.125 MHz for SDATA and MOSI/MISO, and a maximum switching frequency of 56.25 MHz for SCLK and SPICLK. The external current can be calculated for each class of pins that can drive (Table 4). The total external current for the sample configuration is 0.0972 A for V_{DD_DDR2} and 0.013 A for V_{DD_EXT} power supply domains.

Using these currents, the estimated average external power is calculated as:

P_{DDEXT} = (1.8V x 0.0972) + (3.3 V x 0.013 A) = 0.218 W

Equation 14. External power (P_{DDEXT}) calculation for ADSP-2146x processors

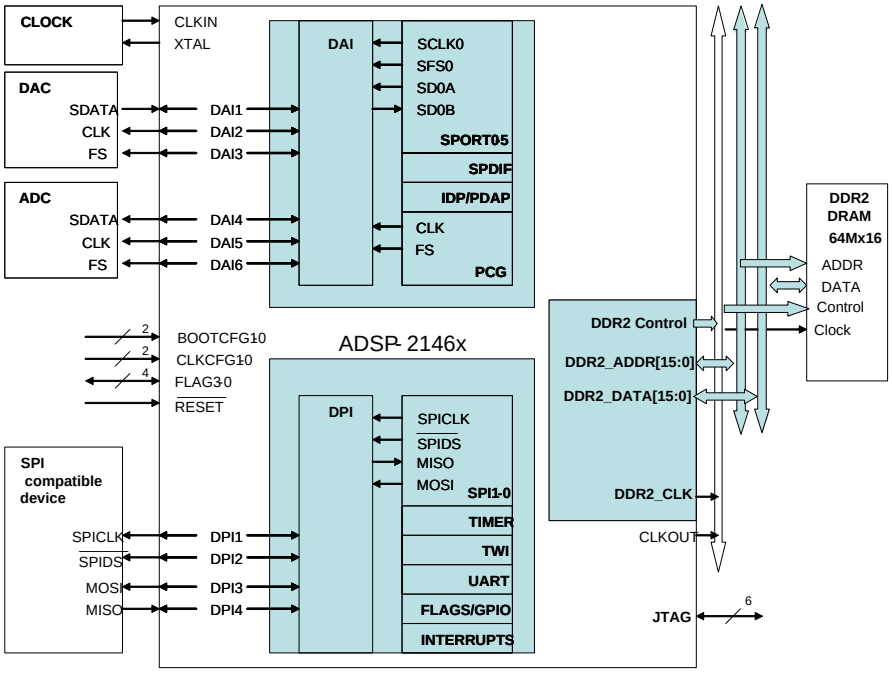

Figure 1. ADSP-2146x system example configuration

Pin Type	No. of Pins	% Switching (activity factor)	x f	x V_{DDEXT}	x C	I_{DDEXT}
DDR2_ADDR[15:0]	16	50	225 MHz	1.8V	5pF + 10pF	0.0486
DDR2_DATA[150]	16	50	450 MHz	1.8V	5pF + 10pF	0.0972
DDR2_CTRL	9	50	56.25 MHz	1.8V	5pF + 10pF	0.0068
DDR2_CLK	1	100	225 MHz	1.8V	5pF + 10pF	0.0061
DAI_P1 (SDATA)	1	100	28.125 MHz	3.3V	5pF + 10pF	0.0014
DAI_P2 (SCLK)	1	100	56.25 MHz	3.3V	5pF + 10pF	0.0028
DAI_P3 (FS)	1	100	3.5 MHz	3.3V	5pF + 10pF	0.00017
DAI_P4 (SDATA)	1	100	28.125 MHz	3.3V	5pF + 10pF	0.0014
DAI_P5 (SCLK)	1	100	56.25 MHz	3.3V	5pF + 10pF	0.0028
DAI_P6 (FS)	1	100	3.5 MHz	3.3V	5pF + 10pF	0.00017
DPI_P1 (SPICLK)	1	100	56.25 MHz	3.3V	5pF + 10pF	0.0028
DPI_P3 (MOSI)	1	100	28.125 MHz	3.3V	5pF + 10pF	0.0014

Table 4. External current (I_{DDEXT}) summary for ADSP-2146x processors

External power consumption for ADSP-2147x processors

For the ADSP-2147x processors also, the example configuration will be the same as Figure 1 but replacing the DDR2 controller with the SDRAM controller. We can estimate the external current and thereby the external power consumption with the following assumptions:

- Processor core running at 266 MHz (`CCLK`)
- 64M x 16-bit external SDRAM memory, C_L = 10 pF (trace capacitance ignored). During external memory writes, 50% of the `ADDR23-0` and `DATA15-0` pins are switching
- DAI configured as SPORT transmitting and receiving 32-bit words at 1/8*`CCLK`, C_L = 10 pF (trace capacitance ignored)
- DPI configured as SPI master transmitting and receiving 32-bit words at 1/8*`CCLK`, C_L = 10 pF (trace capacitance ignored)
- Output capacitance of processor pin, C_{OUT} = 5 pF

For the purpose of this example, it is assumed that the ADSP-2147x processor's SDRAM controller is running at the maximum specified speed of 133 MHz clock with a Core clock of 266 MHz. The switching frequency is quite high for a typical application, and is provided here merely to illustrate a worst-case calculation. In addition to SDRAM, it is also assumed that one serial port (SPORT) and one serial peripheral interface (SPI) are running at one-eighth (1/8) the processor core clock rate (`CCLK`). With a core clock of 266 MHz, this corresponds to a maximum switching frequency of 16.625 MHz for `SDATA` and `MOSI/MISO`, and a maximum switching frequency of 33.25 MHz for `SCLK` and `SPICLK`. The external current can be calculated for each class of pins that can drive and is shown in Table 5. The total external current for the sample configuration is 0.102 A.

Using these currents, the estimated average external power is calculated as:

P_{DDEXT} = 3.3 V x 0.0.083 A = 0.274 W

Equation 15. External power (P_{DDEXT}) calculation for ADSP-2147x processors

Pin Type	No. of Pins	% Switching (activity factor)	x f	x V_{DDEXT}	x C	I_{DDEXT}
ADDR[18:0]	19	50	66.5 MHz	3.3V	5pF + 10pF	0.03127
DATA[15:0]	16	50	66.5 MHz	3.3V	5pF + 10pF	0.02633
SDRAM_CTRL	7	50	66.5 MHz	3.3V	5pF + 10pF	0.01152
SDCLK	1	100	133 MHz	3.3V	5pF + 10pF	0.00658
DAI_P1 (SDATA)	1	100	16.625 MHz	3.3V	5pF + 10pF	0.000822
DAI_P2 (SCLK)	1	100	33.25 MHz	3.3V	5pF + 10pF	0.001645
DAI_P3 (FS)	1	100	2.078 MHz	3.3V	5pF + 10pF	0.000102
DAI_P4 (SDATA)	1	100	16.625 MHz	3.3V	5pF + 10pF	0.000822
DAI_P5 (SCLK)	1	100	33.25 MHz	3.3V	5pF + 10pF	0.001645
DAI_P6 (FS)	1	100	2.078 MHz	3.3V	5pF + 10pF	0.000102
DPI_P1 (SPICLK)	1	100	33.25 MHz	3.3V	5pF + 10pF	0.0001645
DPI_P3 (MOSI)	1	100	16.625 MHz	3.3V	5pF + 10pF	0.000822

Table 5. External current (I_{DDEXT}) summary for ADSP-2147x processors

Pin Type	No. of Pins	% Switching (activity factor)	x f	x V_{DDEXT}	x C	I_{DDEXT}
ADDR[18:0]	19	50	80 MHz	3.3V	5pF + 10pF	0.03762
DATA[15:0]	16	50	80 MHz	3.3V	5pF + 10pF	0.03168
SDRAM_CTRL	7	50	80 MHz	3.3V	5pF + 10pF	0.01386
SDCLK	1	100	160 MHz	3.3V	5pF + 10pF	0.00792
DAI_P1 (SDATA)	1	100	25 MHz	3.3V	5pF + 10pF	0.00123
DAI_P2 (SCLK)	1	100	50 MHz	3.3V	5pF + 10pF	0.002475
DAI_P3 (FS)	1	100	3.1255 MHz	3.3V	5pF + 10pF	0.000154
DAI_P4 (SDATA)	1	100	25 MHz	3.3V	5pF + 10pF	0.00123
DAI_P5 (SCLK)	1	100	50 MHz	3.3V	5pF + 10pF	0.002475
DAI_P6 (FS)	1	100	3.1255 MHz	3.3V	5pF + 10pF	0.000154
DPI_P1 (SPICLK)	1	100	50 MHz	3.3V	5pF + 10pF	0.002475
DPI_P3 (MOSI)	1	100	25 MHz	3.3V	5pF + 10pF	0.00123

Table 6. External current (I_{DDEXT}) summary for ADSP-2148x processors

External power consumption for ADSP-2148x processors

For the ADSP-2148x processors, the example configuration will be the same as Figure 1 but replacing the DDR2 controller with the SDRAM controller. We can estimate the external current and thereby the external power consumption with the following assumptions:

- Processor core running at 400 MHz (CCLK)
- 64M x 16-bit external SDRAM memory, C_L = 10 pF (trace capacitance ignored). During external memory writes, 50% of the ADDR23-0 and DATA15-0 pins are switching
- DAI configured as SPORT transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- DPI configured as SPI master transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- Output capacitance of processor pin, C_{OUT} = 5 pF

For the purpose of this example, it is assumed that the ADSP-2148x processor's SDRAM controller is running at the maximum specified speed of 160 MHz clock with a Core clock of 400 MHz. The switching frequency is quite high for a typical application, and is provided here merely to illustrate a worst-case calculation. In addition to SDRAM, it is also assumed that one serial port (SPORT) and one serial peripheral interface (SPI) are running at one-eighth (1/8) the processor core clock rate (CCLK). With a core clock of 400 MHz, this corresponds to a maximum switching frequency of 25 MHz for SDATA and MOSI/MISO, and a maximum switching frequency of 50 MHz for SCLK and SPICLK. The external current can be calculated for each class of pins that can drive and is shown in Table 6. The total external current for the sample configuration is 0.102 A.

Using these currents, the estimated average external power is calculated as:

P_{DDEXT} = 3.3 V x 0.109 A = 0.336 W

Equation 16. External power (P_{DDEXT}) calculation for ADSP-2148x processors

The power calculator spreadsheets available with this EE-Note can be used for calculating the external power consumption for different applications. User can choose the number of DAI/DPI pins switching, the % switching and the load on each pin to calculate the external power consumption specific to their application. For automotive parts the power consumption by MLB pins can also be added to this one. The spread sheets have default options for external consumption based on the example described in this EE-Note.

Total Power Consumption

For a particular system, the total power consumption becomes the sum of its individual components, which is the power consumed by the internal circuitry plus the power consumed due to the switching of the external pins, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT}$$

Equation 17. Total power (P_{TOTAL}) calculation

Where:
P_{DDINT} = Internal power consumption as defined by Equation 10.
P_{DDEXT} = External power consumption as defined by Equation 12 and Equation 13

In our example, we have considered an ADSP-2146x processor operating at a core voltage of V_{DDINT} = 1.10 V, core frequency of 450 MHz, and code as profiled in Equation 2, and also assuming the resulting junction temperature (T_J) has been estimated to be +45°C. Under these conditions, the total estimated power consumption is:

P_{TOTAL} = 0.95 W + 0.218 W = 1.168 W

Equation 18. Total estimated power consumption for ADSP-2146x processors

For ADSP-2147x processor operating at a core voltage of V_{DDINT} = 1.20 V, core frequency of 266 MHz, and code as profiled in Equation 2, and also assuming the resulting junction temperature (T_J) has been estimated to be +45°C. Under these conditions, the total estimated power consumption is:

P_{TOTAL} = 0. 310 W + 0.274 W = 0.584 W

Equation 19. Total estimated power consumption for ADSP-2147x processors

For ADSP-2148x processor operating at a core voltage of V_{DDINT} = 1.10 V, core frequency of 400 MHz, and code as profiled in Equation 2, and also assuming the resulting junction temperature (T_J) has been estimated to be +45°C. Under these conditions, the total estimated power consumption is:

P_{TOTAL} = 0. 847 W + 0.336 W = 1.183 W

Equation 20. Total estimated power consumption for ADSP-2148x processors

Appendix

Correct functional operation of the ADSP-214xx processor is guaranteed when the junction temperature of the device does not exceed the allowed junction temperature (T_J) as specified in the data sheet. For the ADSP-214xx processor, the total power budget is limited by the maximum allowed junction temperature (T_J) as specified in the data sheet.

The ABSOLUTE MAXIMUM RATINGS table in the ADSP-214xx processor data sheet states that exposure to junction temperatures greater than +125^{O}C for extended periods of time may affect device reliability.

References

[1] *ADSP-21469 SHARC Processor Data Sheet*, Rev 0, June 2010. Analog Devices, Inc

[2] *ADSP-21478/9 SHARC Processor Data Sheet*, Rev 0, April 2011. *Analog Devices, Inc*

[3] *ADSP-21483/6/7/8/9 SHARC Processor Data Sheet*, Rev 0, January 2011. Analog Devices, In

[4] *ADSP-214xx SHARC Processor Hardware Reference*, Rev 0.3, July 2010. Analog Devices, Inc.

Document History

Revision	Description
Rev 4 – Feb 22, 2011 *by Divya Sunkara*	Added the information specific to ADSP-2147x processors. Also, included the ADSP-2147x power calculator spreadsheet in the associated .ZIP file.
Rev 3 – Dec 17, 2010 *by Jeyanthi Jegadeesan*	Initial public release. Includes updated ADSP-2148x power calculator spreadsheet.
Rev 2 – Sep 9, 2010 *by Jeyanthi Jegadeesan*	Added the information specific to ADSP-2148x processors and changed the title from "Estimating Power for ADSP-2146x SHARC processors" to "Estimating Power for ADSP-214xx SHARC processors". In addition to the ADSP-2146x power calculator spreadsheet, added the same for ADSP-2148x processors in the associated .ZIP file.
Rev 1 – April 5, 2010 *by Ramdas Chary*	Preliminary release.