ADZS-21569-EZKIT Manual

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Copyright Information

Regulatory Compliance

The *ADZS-21569-EZKIT* evaluation board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer-end product or as a portion of a consumer-end product. The board is an open system design, which does not include a shielded enclosure and, therefore, may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The *ADZS-21569-EZKIT* evaluation board is in the process of being certified to comply with the essential requirements of the European EMC directive 2004/108/EC and, therefore, carries the *"CE"* mark.

The *ADZS-21569-EZKIT* evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused boards in the protective shipping package.

Contents

Hardware Reference

1   Preface

Thank you for purchasing the Analog Devices, Inc. *ADZS-21569-EZKIT* evaluation system.

Purpose of This Manual

This manual provides instructions for installing the product hardware (board). This manual describes operation and configuration of the board components and provides guidelines for running code on the board.

Manual Contents

The manual consists of:

- *Using the board*

  Provides basic board information.

- *Hardware Reference*

  Provides information about the hardware aspects of the board.

- *Bill of Materials*

  A companion file in PDF format that lists all of the components used on the board is available on the website at http://www.analog.com/ADZS-21569-EZKIT .

- *Schematic*

  A companion file in PDF format documenting all of the circuits used on the board is available on the website at http://www.analog.com/ADZS-21569-EZKIT .

Technical Support

Supported Integrated Circuit

This evaluation system supports the Analog Devices ADSP-21569 IC.

Supported Tools

Product Information

Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products - analog integrated circuits, amplifiers, converters, transceivers, and digital signal processors.

Also note, MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone

EngineerZone is a technical support forum from Analog Devices, Inc. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

2   Using the Board

This chapter provides information on the major components and peripherals on the board, along with instructions for installing and setting up the emulation software.

Product Overview

The board features:

- Analog Devices ADSP-21569 processor

  - 400 ball BGA

  - 25 MHz oscillator

- DDR3 Memory

  - 512Mx16 bit (8Gbit)

  - ISSI IS43TR16512BL-125KBL

  - 1.35V

- SPI Flash Quad (`SPI2`) Memory

  - 512Mbit

  - ISSI IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI

  - Single/Dual/Quad SPI

- SPI Flash Octal (`SPI2`) Memory

  - 1Gbit

  - Macronix MX66LM1G45G - 1G-bit Serial Flash Memory with Single and Octal SPI

  - Single/Octal SPI

- SPI EEPROM

  - Microchip 25LC010AT - 1K SPI Serial EEPROM

- Audio

- Analog Devices ADAU1962A - 12 Channel, High Performance, 192kHz, 24-Bit DAC
  - Analog Devices ADAU1977 - Quad ADC with Diagnostics
  - Analog Devices ADAU1979 - Quad Analog-to-Digital Converter
  - 12 RCA connectors. 12 outputs or 8 outputs/4 inputs
- Universal Asynchronous Receiver/Transmitter (UART0)
  - FTDI FT232R - USB to UART
  - USB micro-B
- A^2B
  - Analog Devices AD2428 - Automotive Audio Bus A^2B Transceiver
  - Two DuraClik connectors
- Debug Interface (JTAG and Trace)
  - ICE-1000 emulator
  - JTAG 10-pin 0.05" header
  - JTAG and Trace 38-pin Mictor connector
- LEDs
  - 11 LEDs: one power (green), one board reset (red), 3 general-purpose (amber), 3 A2B LEDs, one fault (red) and 2 UART leds (amber)
- Pushbuttons
  - Three pushbuttons: one reset and two IRQ/Flag
- EI3 connector
  - SMC
  - EPPI
  - SPORT
  - SPI
  - UART
  - TWI
  - TMR
  - GPIO
  - RESET

- GND/3.3V/5V output
- External power supply
  - CE compliant
  - 12V @1.6 Amps
- Power measurement
  - 0.051-ohm resistors for measuring current draw

Package Contents

Your *ADZS-21569-EZKIT* package contains the following items.

- *ADZS-21569-EZKIT* board
- Universal 12V DC power supply
- USB 2.0 type A to micro-B cable
- ICE-1000 emulator

Contact the vendor where you purchased your *ADZS-21569-EZKIT* evaluation board or contact Analog Devices, Inc. if any item is missing.

Default Configuration

The *ADZS-21569-EZKIT* board is designed to run as a standalone unit.

The *Default Hardware Setup* figure shows the default settings for jumpers and switches and the location of the jumpers, switches, connectors, and LEDs. Confirm that your board is in the default configuration before using the board.

Default Config
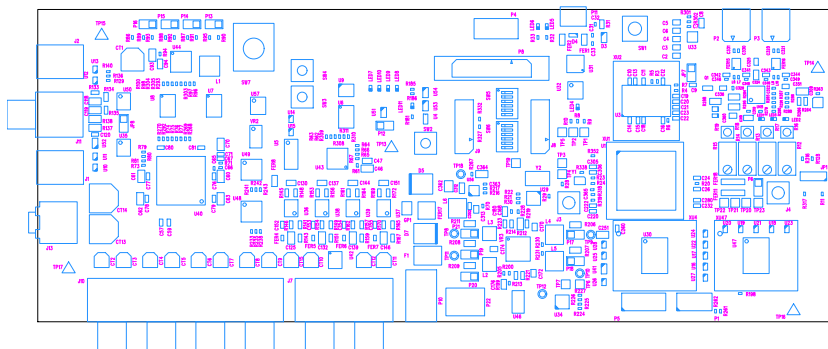
Figure 2-1: Default Hardware Setup

NOTE: Connectors on the back of the board are noted with dotted lines if applicable.

Debug Interface

The *ADZS-21569-EZKIT* provides a JTAG and Trace connection via `P4` or `P8`.

Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all EZ-KIT peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT is fully tested for an extended period of time with POST. All EZ-KIT boards are shipped with POST preloaded into flash memory. The POST is executed by resetting the board and connecting the USB To UART to your PC and open up a terminal window. The POST also can be used as a reference for a custom software design or hardware troubleshooting.

Note that the source code for the POST program is included in the Board Support Package (BSP) along with the readme file that describes how the board is configured to run POST.

Example Programs

Example programs are provided with the *ADZS-21569-EZKIT* Board Support Package (BSP) to demonstrate various capabilities of the product. The programs can be found in the `ADSP-21569_EZ-KIT\examples` installation folder. Refer to the readme file provided with each example for more information.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the schematic design, layout, fabrication, and assembly of the board.

The information can be found at:

http://www.analog.com/ADZS-21569-EZKIT

Expansion Interface 3

The Expansion Interface 3 (EI3) interface supports connecting with other EI3 daughterboards designed by Analog Devices, extending the evaluation system's capabilities. The connectors provide power, ground, reset, ADC, PPI, TWI, UART, SPORT, SMC and GPIO signals.

The expansion interface is architected to provide support for modularity with different expansion board types. These types fall into several categories including audio, video, converter, and asynchronous memory.

More information about available extender boards can be found at: http://www.analog.com/en/design-center/landing-pages/001/sharc-processors-software-and-tools.html

25LC010AT - 1K SPI Serial EEPROM

The Microchip Technology Inc. 25XX010A* is a 1 Kbit Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (CS) input.

AD2428 - Automotive Audio Bus A^{2}B Transceiver

The Automotive Audio Bus (A^{2}B$^®$) provides a multichannel, I2S/TDM link over distances of up to 15 m between nodes. It embeds bidirectional synchronous pulse-code modulation (PCM) data (for example, digital audio), clock, and synchronization signals onto a single differential wire pair. A^{2}B supports a direct point to point connection and allows multiple, daisy-chained nodes at different locations to contribute and/or consume time division multiplexed channel content.

A^{2}B is a single-master, multiple-slave system where the transceiver chip at the host controller is the master. The master generates clock, synchronization, and framing for all slave nodes. The master A^{2}B chip is programmable over a control bus (I^{2}C) for configuration and read back. An extension of this control bus is embedded in the A^{2}B data stream, which grants direct access of registers and status information on slave transceivers as well as I^{2}C to I^{2}C communication over distance.

The transceiver can connect directly to general-purpose digital signal processors (DSPs), field-programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), microphones, analog-to-digital converters (ADCs), digital-toanalog converters (DACs), and codecs through a multichannel I^{2}S/TDM interface. It also provides a pulse density modulation (PDM) interface for direct connection of up to four PDM digital microphones.

Finally, the transceiver also supports an A^{2}B bus powering feature, where the master node supplies voltage and current to the slave nodes over the same daisy-chained, twisted pair wire cable as used for the communication link.

ADAU1962A - 12 Channel, High Performance, 192kHz, 24-Bit DAC

The ADAU1962A is a high performance, single-chip digital-to-analog converter (DAC) that provides 12 DACs with differential or single-ended output using the Analog Devices, Inc., patented multibit sigma-delta (Σ-Δ) architecture. A serial peripheral interface (SPI)/I2C port is included, allowing a micro-controller to adjust volume and many other parameters. The ADAU1962A operates from 2.5 V digital and 3.3 V analog supplies. A linear regulator is included to generate the digital supply voltage from the analog supply voltage.

The ADAU1962A is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive the internal master clock from an external LRCLK, the ADAU1962A can eliminate the need for a separate high frequency master clock and can be used with or without a

bit clock. The DACs are designed using the latest Analog Devices continuous time architectures to further minimize EMI.

ADAU1977 - Quad ADC with Diagnostics

The ADAU1977 incorporates four high performance analog-todigital converters (ADCs) with direct-coupled inputs capable of 10 V rms. The ADC uses multibit sigma-delta (Σ-Δ) architecture with continuous time front end for low EMI. The ADCs can be connected to the electret microphone (ECM) directly and provide the bias for powering the microphone. Built-in diagnostic circuitry detects faults on input lines and includes comprehensive diagnostics for faults on microphone inputs. The faults reported are short to battery, short to microphone bias, short to ground, short between positive and negative input pins, and open input terminals. In addition, each diagnostic fault is available as an IRQ flag for ease in system design. An I2C/SPI control port is also included. The ADAU1977 uses only a single 3.3 V supply. The part internally generates the microphone bias voltage. The microphone bias is programmable in a few steps from 5 V to 9 V. The low power architecture reduces the power consumption. An on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with a frame clock, the PLL eliminates the need for a separate high frequency master clock in the system.

ADAU1979 - Quad Analog-to-Digital Converter

The ADAU1979 incorporates four high performance, analog-to-digital converters (ADCs) with 4.5 V rms capable ac-coupled inputs. The ADCs use a multibit sigma-delta (Σ-Δ) architecture with continuous time front end for low EMI. An I2C/serial peripheral interface (SPI) control port is included that allows a microcontroller to adjust volume and many other parameters. The ADAU1979 uses only a single 3.3 V supply. The device internally generates the required digital DVDD supply. The low power architecture reduces the power consumption. The on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with the frame clock, it eliminates the need for a separate high frequency master clock in the system.

FT232R - USB to UART

The FT232R is a USB-to-serial-UART interface with the following advanced features:

- Single chip USB to asynchronous serial data transfer interface

- Entire USB protocol handled on the chip. No USB specific firmware programming required

- Fully-integrated 1024 bit EEPROM storing device descriptors and CBUS I/O configuration

- Fully-integrated USB termination resistors

- Fully-integrated clock generation with no external crystal required, plus optional clock output selection enabling a glue-less interface to external MCU or FPGA

- Data transfer rates from 300 baud to 3 Mbaud (RS422, RS485, RS232) at TTL levels

- 128 byte receive buffer and 256 byte transmit buffer utilizing buffer smoothing technology to allow for high-data throughput

- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.

- Transmit and receive LED drive signals

- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity

- FIFO receives and transmits buffers for high-data throughput

- Device supplied pre-programmed with unique USB serial number

- Supports bus powered, self-powered and high-power bus powered USB configurations

- Integrated +3.3V level converter for USB I/O

- Integrated level converter on UART and CBUS for interfacing to between +1.8V and +5V logic

- True 5V/3.3V/2.8V/1.8V CMOS drive output and TTL input

- Configurable I/O pin output drive strength

- Integrated power-on-reset circuit

- Fully-integrated AVCC supply filtering - no external filtering required.

- UART signal inversion option

- +3.3V (using external oscillator) to +5.25V (internal oscillator) single supply operation

- Low-operating and USB suspend current

- Low USB bandwidth consumption

- UHCI/OHCI/EHCI host controller compatible

- USB 2.0 full speed compatible

INA3221 - Triple Channel, High Measurement, Shunt and Bus Voltage Monitor

The INA3221 is a three-channel, high-side current and bus voltage monitor with an I^2C- and SMBUS-compatible interface. The INA3221 monitors both shunt voltage drops and bus supply voltages, in addition to having programmable conversion times and averaging modes for these signals. The INA3221 offers both critical and warning alerts to detect multiple programmable out-of-range conditions for each channel.

IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI

The IS25LP512M and IS25WP512M Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems

that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 66.5Mbytes/sof data throughput. The IS25xE series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addressesand read data on both edges of the clock.These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (eXecute In Place) operation.

The memory array is organized into programmable pages of 256/512bytes. This family supports page program mode where 1 to 256/512bytes of data areprogrammed in a single command.

QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64K/256Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

MX66LM1G45G - 1G-bit Serial Flash Memory with Single and Octal SPI

MX66LM1G45G is 1Gbit Serial NOR Flash memory, which is configured as 134,217,728 x 8 internally. MX66LM1G45G feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

The MX66LM1G45G MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

3 Hardware Reference

This chapter describes the hardware design of the *ADZS-21569-EZKIT* .

System Architecture

The board's configuration is shown in the ***Block Diagram*** figure.
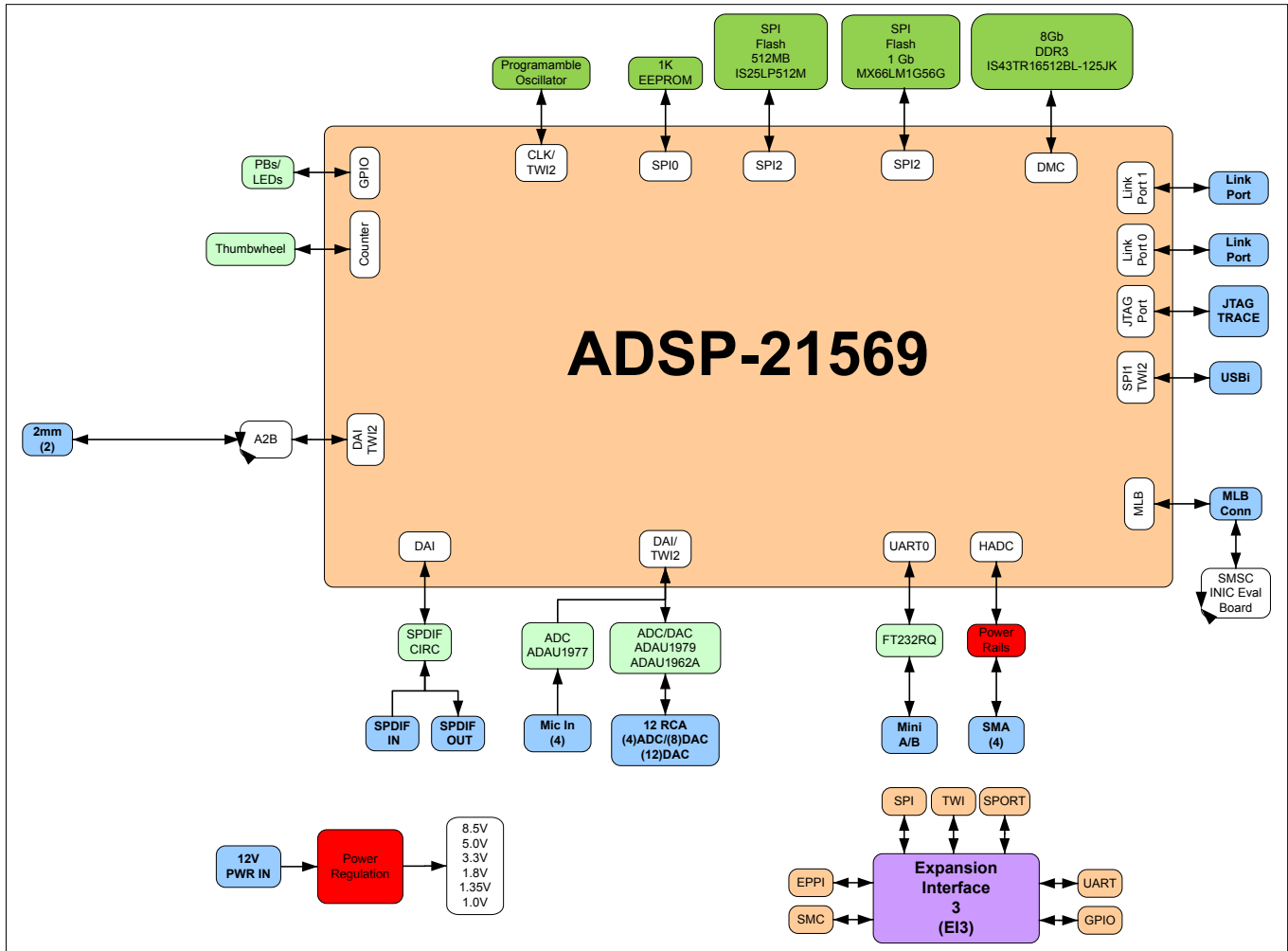
Figure 3-1: Block Diagram

This EZ-KIT is designed to demonstrate the ADSP-21569 processor's capabilities. The board has a 25 MHz input clock and runs at a max core clock frequency of 1GHz.

User I/O to the processor is provided in the form of two pushbuttons and three LEDs.

The software-controlled switches (SoftConfig) facilitate the switch multi-functionality by disconnecting the pushbuttons from their associated processor pins and reusing the pins elsewhere on the board.

Software-Controlled Switches (SoftConfig)

On the board, most of the traditional mechanical switches and jumpers have been replaced by I^2C software-controlled switches. The remaining mechanical switches are provided for the boot mode and pushbuttons. Reference any `SoftConfig*.c` file found in the installation directory for an example of how to set up the SoftConfig feature of

the board through software. The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided by ADI is used, there should be little need to reference this section.

NOTE: Care should be taken when changing SoftConfig settings not to create a conflict with interfaces. This is especially true when connecting extender cards.

Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses similar FET and bus switch components that are on the board.

After this generic discussion there is a detailed explanation of the SoftConfig interface specific to the *ADZS-21569-EZKIT* .

The *Example of Individual FET Switches* figure shows two individual FET switches (Pericom PI3A125CEX) with reference designators UA and UB. Net names ENABLE_A and ENABLE_B control UA and UB. The default FET switch enable settings in this example are controlled by resistors RA and RB which pull the enable pin 1 of UA and UB to ground (low). In a real example, these enable signals are controlled by the Microchip IO expander. The default pull-down resistors connects the signals EXAMPLE_SIGNAL_A and EXAMPLE_SIGNAL_B and also connects signals EXAMPLE_SIGNAL_C and EXAMPLE_SIGNAL_D. To disconnect EXAMPLE_SIGNAL_A from EXAMPLE_SIGNAL_B, the Microchip IO expander is used to change ENABLE_A to a logic 1 through software that interfaces with the Microchip. The same procedure for ENABLE_B disconnects EXAMPLE_SIGNAL_C from EXAMPLE_SIGNAL_D.

Figure 3-2: Example of Individual FET Switches

The following figure shows the equivalent circuit to the ***Example of Individual FET Switches*** figure but utilizes mechanical switches that are in the same package. Notice the default is shown by black boxes located closer to the ***ON*** label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.
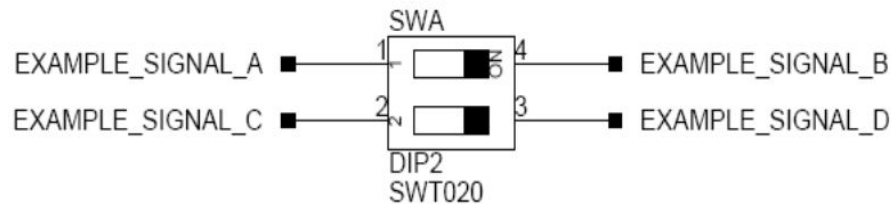
Figure 3-3: Example of a Mechanical Switch (Equivalent to Example of Individual FET Switches Figure)

The ***Example of Bus Switch*** figure shows a bus switch example, reference designator UC (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (0B1) and the letter on the upper group (0B2). The default setting is controlled by the signal CONTROL_LETTER_NUMBER which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the Microchip IO expander is not shown but controls the signal CONTROL_LETTER_NUMBER and allows the user to change the selection through software.
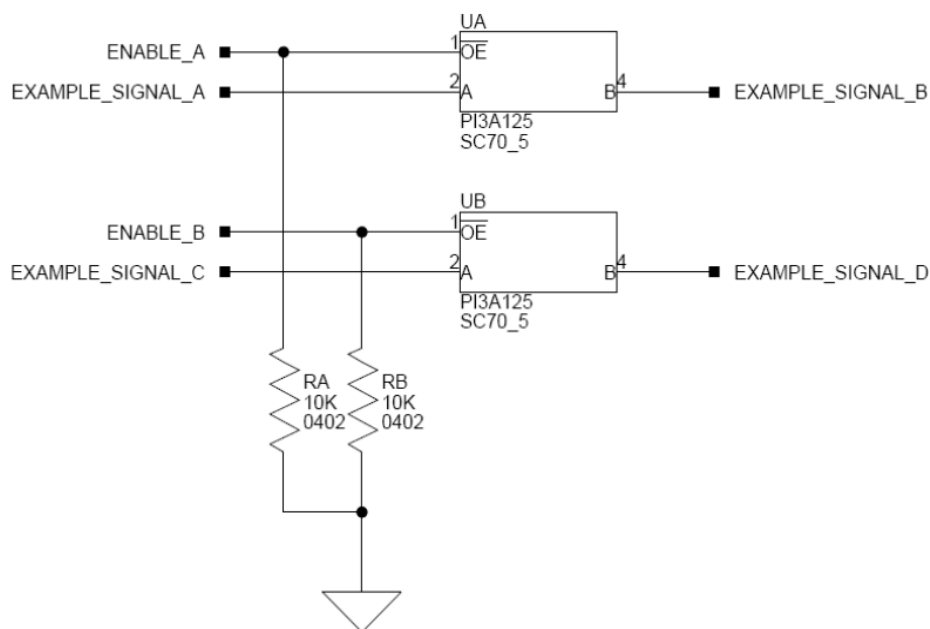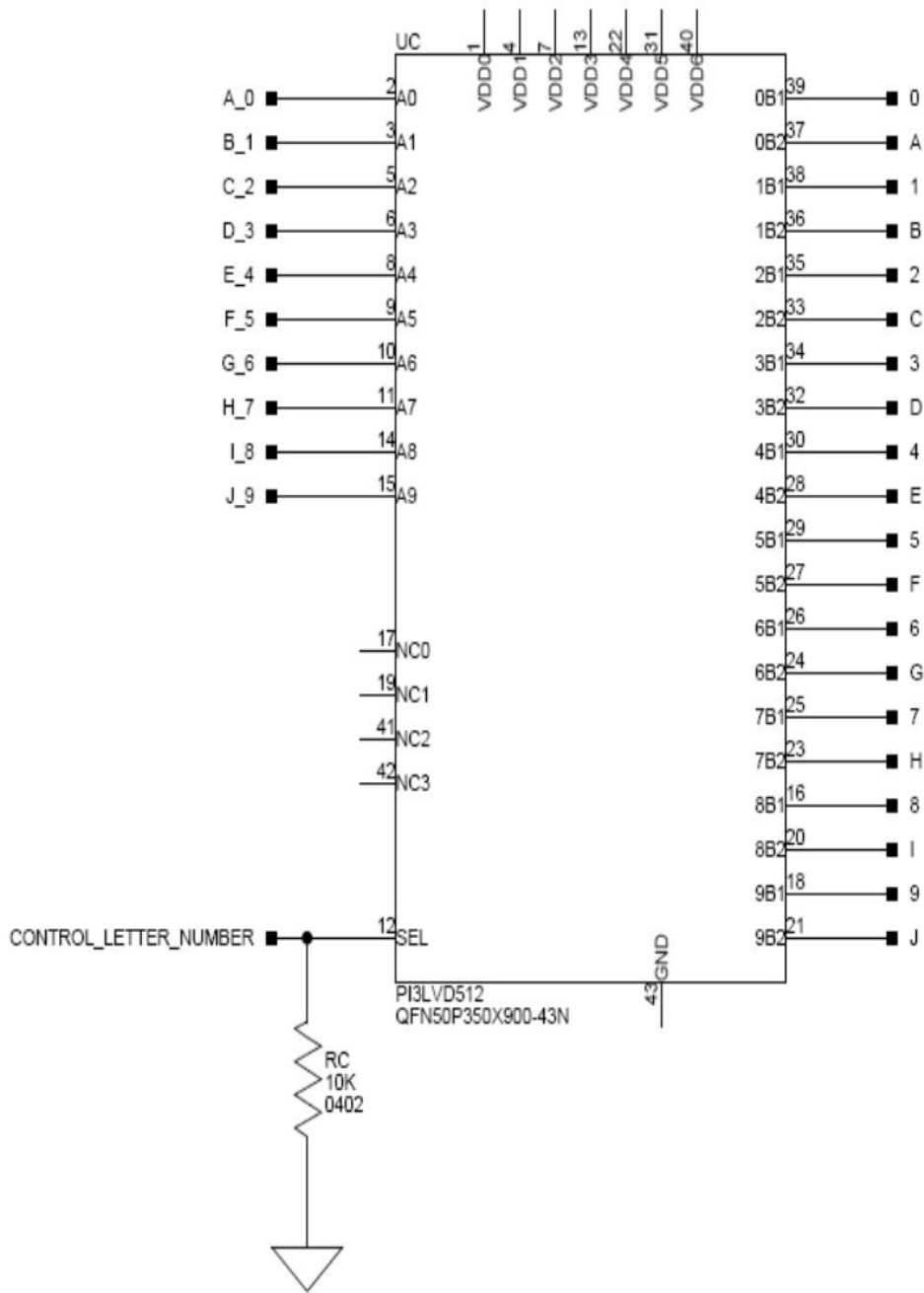
Figure 3-4: Example of a Bus Switch

The following figure shows the equivalent circuit to the *Example of Bus Switch* figure but utilizes mechanical switches. Notice the default for reference designators SWC and SWD is illustrated by black boxes located closer to the *ON* label of the switches to enable the number signals by default. Also notice the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.
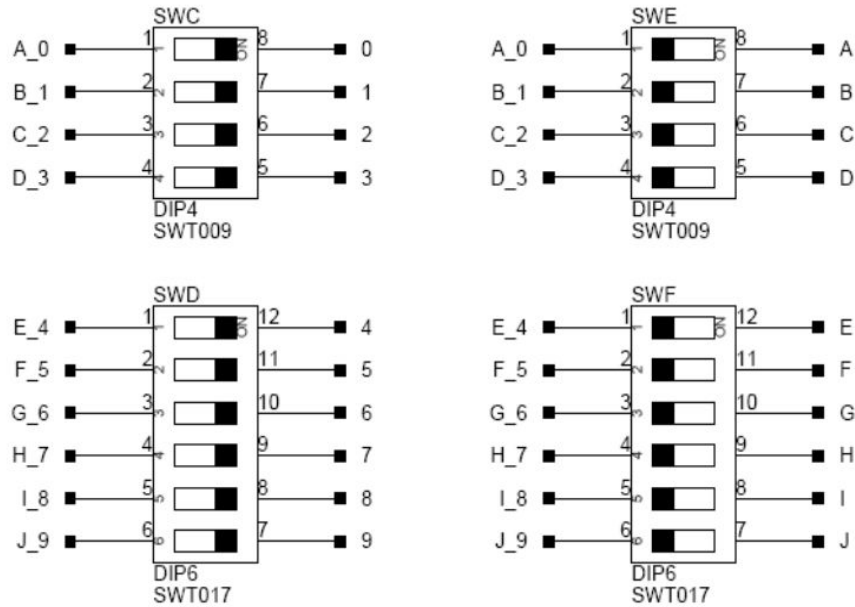
Figure 3-5: Example of a Mechanical Switch (Equivalent to Example of Bus Switch)

SoftConfig on the Board

Two Microchip MCP23017 GPIO expanders provide control for individual electronic switches. The TWI2 interface of the processor communicates with the Microchip devices. There are individual switches with default settings that enable basic board functionality.

The *Default Processor Interface Availability* table lists the processor and board interfaces that are available by default. Note that only interfaces affected by software switches are listed in the table.

Table 3-1: Default Processor Interface Availability

Interface	Availability by Default
UART0	USB to UART FTDI232RQ
SPI Flash	Quad mode enabled
Audio Connectors	4 inputs/8 outputs
S/PDIF Digital	S/PDIF RCA input and output connectors enabled
Pushbuttons	Enabled
LEDs	Enabled

Programming SoftConfig Switches

On the board, two Microchip MCP23017 devices exist. Each of these devices have the following programming characteristics:

- Each GPIO register controls eight signals (software switches).

GPIO Register	Register Address
GPIOA	0x12
GPIOB	0x13

- By default, the Microchip MCP23017 GPIO signals function as input signals.

  The signals must be programmed as output signals to override their default values. A zero is programmed into the register to enable the signal as an output. The following table shows the Microchip register addresses.

IODIR Register	IODIR Register Address
IODIRA	0x00
IODIRB	0x01

Each example in the Board Support Software (BSP) includes source files that program the soft switches, even if the default settings are being used. The README for each example identifies only the signals that are being changed from their default values. The code that programs the soft switches is located in the SoftConfig_XXX.c file in each example where XXX is the name of the baord.

The following tables (*I²C Hardware Address 0x21* and *I²C Hardware Address 0x22*) outline the default values for each of the two Microchip MCP23017 devices.

Table 3-2: I²C Hardware Address 0x21

GPIO	MCP23017 Register Address	Default Value
GPIOA	0x12	0x02
GPIOB	0x13	0xC4

Table 3-3: I²C Hardware Address 0x22

GPIO	MCP23017 Register Address	Default Value
GPIOA	0x12	0xE0
GPIOB	0x13	0xFF

The board schematic shows how the two Microchip GPIO expanders are connected to the board's ICs.

Tables *Output Signals of Microchip GPIO Expander (U47 Port A)* and *Output Signals of Microchip GPIO Expander (U47 Port B)* show the output signals of the Microchip GPIO expander (*U47*), with a TWI address of 0100 001X, where X represents the read or write bit. The signals that control an individual FET have an entry in the *FET* column. The *Component Connected* column shows the board IC that is connected if the FET is enabled. The Microchip (U47) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in **bold** font in the *Processor Signal* column.

Table 3-4: Output Signals of Microchip GPIO Expander (U48 Port A)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Connected	Default
0	EEPROM_EN	SPI EEPROM CS	U25	PA_09/SPI0_SEL1b/ UART0_CTSb/OSPI_D7/ SMC0_D09/SPI0_SSb	U41	High
1	UART0_FLOW_ EN	UART0 Flow Control	U32	PA_08/SPI0_MOSI/ UART0_RTSb/OSPI_D6/ SMC0_D08/TM0_ACLK2	U31	Low
2	UART0_EN	Enables UART0	U32	PA_06/SPI0_CLK/ UART0_TXb/OSPI_D4/ SMC0_D06/TM0_ACLK1	U31	Low
3	ADAU_RESET	Reset ADAU ICs	U6, U7, U8	None	U40, U43, U44	High
4	OCTAL_SPI_ CS_EN	Connects Octal CS to SPI port	U16	PA_05/SPI2_SEL1b/ OSPI_SEL1b/SMC0_D05/ SPI2_SSb	U47	High
5	OCTAL_SPI_ CONNECT	Connects Octal signals to SPI port	U17	PA_00/SPI2_MISO/ OSPI_MISO/SMC0_D00	U47	High
6	THUMBWHEEL_ OE	Enables Rotary Switch	U48	Counter signals	U57	High
7	NOT USED					

Table 3-5: Output Signals of Microchip GPIO Expander (U48 Port B)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Connected	Default
0	ADAU1962_EN	Enables ADAU1962	U7	DAI0_PIN02, DAI0_PIN04, DAI0_PIN0, DAI0_PIN05 and DAI0_PIN10	U40	High
1	ADAU1979_EN	Enables ADAU1979	U7	DAI0_PIN20, DAI0_PIN12, DAI0_PIN06 and DAI0_PIN07	U43	High
2	AUDIO_JACK_ SEL	Selects between connector being configured for input or output	U40	None	J3	High
3	NOT USED					
4	SPI2FLASH_ CS_EN	SPI2 FLASH CS	U26	PB_15/SPI2_SEL1b	U30	Low
5	SPI2D2_D3_ EN	Enables Quad mode for SPI2 Flash	U27 and U28	PB_12/SPI2_D2 and PB_13/ SPI2_D3	U30	Low
6	SPDIF_ OPTICAL	Enables S/PDIF optical connectors	U10 and U13	DAI0_PIN09, DAI0_PIN10	J1 and J2	Low

Table 3-5: Output Signals of Microchip GPIO Expander (U48 Port B) (Continued)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Connected	Default
7	SPDIF_ DIGITAL_EN	Enables S/PDIF digital connectors	U11 and U12	DAI0_PIN09, DAI0_PIN10	J11	High

Tables *Output Signals of Microchip GPIO Expander (U48 Port A)* and *Signals of Microchip GPIO Expander (U48 Port B)* show the output signals of the Microchip GPIO expander (*U48*), with a TWI address of `0100 010X`, where `X` represents the read or write bit. The signals that control an individual FET have an entry in the *FET* column. The *Component Connected* column shows the board IC that is connected if the FET is enabled. However, in most cases, the Microchip (`U48`) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in *bold* font in the *Processor Signal* column.

Table 3-6: Output Signals of Microchip GPIO Expander (U48 Port A)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Connected	Default
0	NOT USED					
1	PUSHBUTTON2 _EN	PC_07 is used as GPIO input for push button 2, enabled by default	U15	PC_07/LP1_CLK/ OSPI_SEL4b/TM0_TMR9/ SYS_FAULT	SW3	Low
2	PUSHBUTTON1 _EN	PB_03 is used as GPIO input for push button 1, enabled by default	U14	PB_03/TM0_TMR3/FLG2/ SPI2_SEL2b/SMC0_ADDR1/ CNT0_UD	SW4	Low
3	LEDS_EN	Px & DAI is used as GPIO output for LED7,9,10 enabled by default	U8	DAI0_PINI08, DAI0_PIN11, PB_03	LED7,9,10	Low
4	NOT USED					
5	NOT USED					
6	NOT USED					
7	NOT USED					

Table 3-7: Output Signals of Microchip GPIO Expander (U48 Port B)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Connected	Default
0	ADAU1977_EN	Enables ADAU1977	U8	DAI0_PIN08, DAI0_PIN09, DAI0_PIN11 and DAI0_PIN19	U44	High
1	ADAU1977_ FAULT_RST_ EN	Enables ADAU1977 FAULT and RESET	U7	PB_13/LP0_D6/SPI1_SEL3b/ UART2_RTSb and ADAU_RE-SET	U44	High

Table 3-7: Output Signals of Microchip GPIO Expander (U48 Port B) (Continued)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Connected	Default
2	NOT USED					
3	ENGINE_RPM_OE	PE_09 is used as an input for engine RPM, disabled by default	U52	PA_00/SMC0_A01	P12	High
4	NOT USED					
5	NOT USED					
6	NOT USED					
7	NOT USED					

Switches

This section describes operation of the switches. The switch locations are shown in the *Switch Locations* figure.
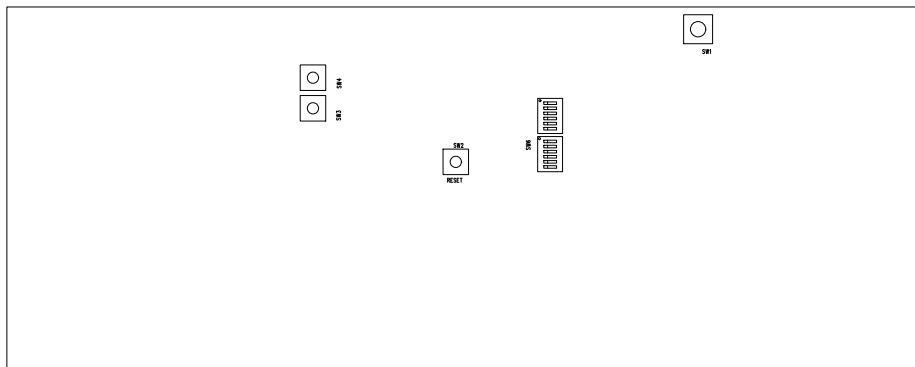
Figure 3-6: Switch Locations

Boot Mode Select (SW1)

The Boot Mode selection switch selects between the different boot modes of the processor. The *Boot Mode Switch* table shows the available boot mode settings. By default, the processor boots from SPI2 master boot which uses the on-board SPI flash memory.

Table 3-8: Boot Mode Switch

Position	Processor Boot Mode
0	No Boot
1	*SPI Master Boot*
2	SPI Slave Boot
3	UART Boot
4	Link Port Boot

Table 3-8: Boot Mode Switch (Continued)

Position	Processor Boot Mode
5	OSPI Master Boot
6	Reserved
7	Reserved

Reset Pushbutton (`SW2`)

The reset pushbutton resets the ADSP-21569 processor. The reset signal also is connected to the expansion connectors via the `SYS_HWRST`signal. Reset (`LED11`) is used to indicate when the board is in reset.

GPIO Pushbuttons (`SW4 and SW3`)

The GPIO pushbuttons are connected to the processor's signals `PB_03/TM0_TMR3/FLG2/SPI2_SEL2b/SMC0_ADDR1/CNT0_UD` and `PC_07/LP1_CLK/OSPI_SEL4b/TM0_TMR9/SYS_FAULT`, respectively.

The GPIO pushbuttons can be disconnected from the processor by setting SoftConfig, see Software-Controlled Switches (SoftConfig) for more information.

Rotary Encoder (`SW7`)

The rotary encoder can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch, activated by pushing the switch towards the center of the board, that can be used to set the counter to zero. The rotary encoder is a two-bit quadrature (Gray code) encoder.

The rotary encoder can be disconnected from the processor by setting SoftConfig, see Software-Controlled Switches (SoftConfig) for more information.

JTAG Interface (`SW5 and SW6`)

The JTAG Interface switches select between a single processor (one board) and multiprocessor (more than one board) configurations. By default, the switches are set up for a single EZ-KIT configuration.

Table 3-9: Single Processor Configuration

Location	Position
SW5.1	ON
SW5.2	OFF
SW5.3	ON
SW5.4	OFF
SW5.5	ON
SW5.6	OFF

Table 3-9: Single Processor Configuration (Continued)

Location	Position
SW6.1	ON
SW6.2	OFF
SW6.3	ON
SW6.4	OFF
SW6.5	OFF
SW6.6	OFF

To use an emulator and multiple EZ-KITs simultaneously set up the boards as shown below. Attach the boards to each other through connectors J8 and J9 . Connect using the Samtec cables described in Link Port/JTAG (J8 and J9).

Table 3-10: Multiple Processor Configuration

Location	EZ-KIT connected to emualtor	EZ-KIT not conencted to emulator
SW5.1	ON	OFF
SW5.2	ON	ON
SW5.3	ON	OFF
SW5.4	ON	ON
SW5.5	ON	OFF
SW5.6	ON	ON
SW6.1	ON	OFF
SW6.2	OFF	OFF
SW6.3	OFF	OFF
SW6.4	ON	ON
SW6.5	OFF	ON
SW6.6	ON	OFF

Jumpers

This section describes functionality of the configuration jumpers. The *Jumper Locations* figure shows the jumper locations.
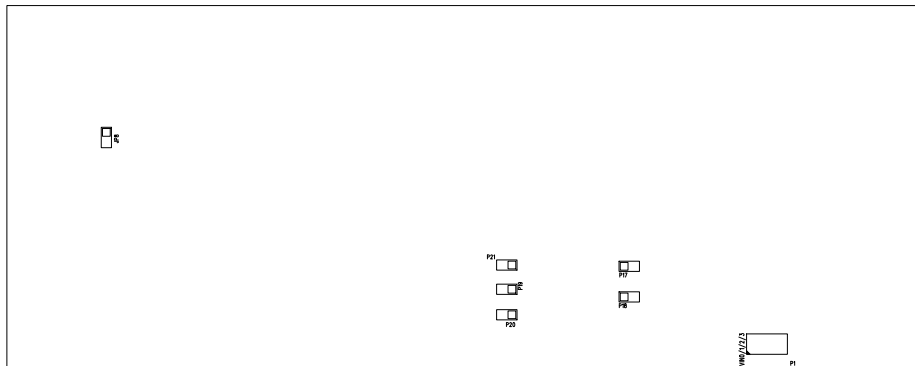
Figure 3-7: Jumper Locations

S/PDIF Loopback (`JP8`)

The S/PDIF loopback jumper is used to connect the S/PDIF input and output signals together and bypass the two RCA connectors.

Current Measurement (`P17, P18, P19, P20, and P21`)

The current measurement jumpers are used to measure the current draw of the `VDD_INT, 1.5V, 3.3V,` `VDD_EXT and USB0_VBUS` respectively. The default is for the jumpers to be installed. To measure the current draw, remove the jumper and measure the voltage across the precision resistor. The current can be calculated by dividing the measured voltage by the 0.051 ohm resistor. For best results a differential probe should be used to measure the voltage across the resistor.

HADC (`P1`)

The HADC jumper is used to connect the HADC of the processor to various voltages on the board for monitoring.

Jumper	Voltage
1 and 2	VDD_INT
3 and 4	1.8V
5 and 6	1.35V
7 and 8	MIC BIAS

LEDs

This section describes the on-board LEDs. The *LED Locations* figure shows the LED locations.
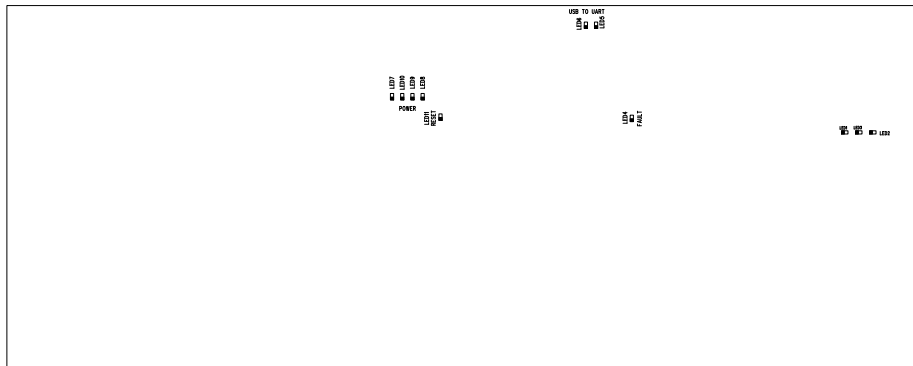
Figure 3-8: LED Locations

Fault (`LED4`)

When ON, it indicates a system fault. For more information, refer to the ADSP-2156xHardware Reference Manual.

USB to UART Activity (`LED5-6`)

The USB to UART activity LEDs are used to indicate the transmitting and receiving of data between a PC and the FT232R - USB to UART.

Table 3-11: USB to UART LEDs

LED	Function
LED2	Receive
LED3	Transmit

A^{2}B Interrupt (`LED1`)

The A^{2}B interrupt LED is driven by the AD2428 when it is configured as a master and driven by the ADSP-21569 when the AD2428 is configured as a slave.

Power (`LED8`)

When ON (green), it indicates that power is being supplied to the board properly.

GPIO (`LED7, LED10, LED9`)

Three LEDs are connected to the general-purpose I/O pins of the processor (see the **GPIO LEDs** table). The LEDs are active high and are turned ON (amber) by writing a 1 to the correct processor signal.

Table 3-12: GPIO LEDs

Reference Designator	Programmable Flag Pin
LED7	PB_03
LED9	DAI0_PIN08
LED10	DAI0_PIN11

Reset (`LED11`)

When ON (red), it indicates that the board is in reset. A master reset is asserted by pressing SW2 , which activates the LED. For more information, see Reset Pushbutton (SW2).

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in the *Connector Locations* figure.
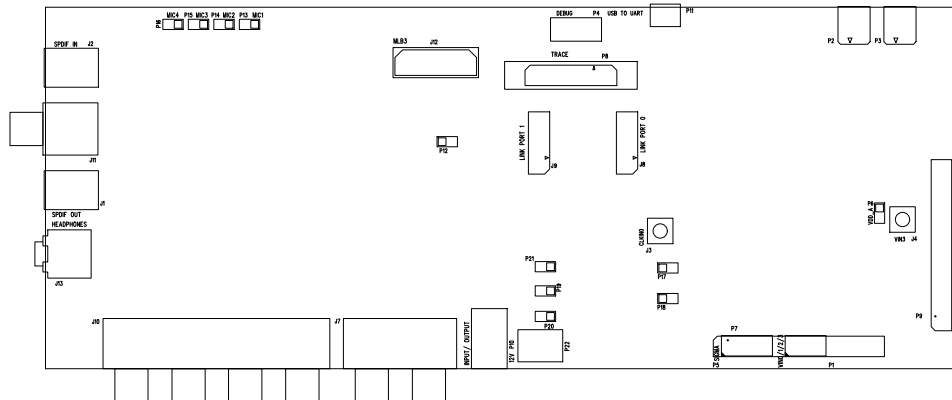

Figure 3-9: Connector Locations

NOTE: Connectors on the back of the board are noted with dotted lines.

S/PDIF Optical Tx (`J1`)

Part Description	Manufacturer	Part Number
Fiber optic transmitter	Everlight	PLT133/T10W
Mating Cable		
Standard TOSLINK optical digital cable		

Clock (`J2`)

Part Description	Manufacturer	Part Number
SMB jack	Emerson	131-3711-201
Mating Cable		
Standard SMB cable		

Audio Input/Output (`J3`)

Part Description	Manufacturer	Part Number
RCA 2x2 female	Switchcraft	PJRAS2X2S
Mating Cable		
Standard audio cable with RCA connectors		

Link Port/JTAG (`J8 and J9`)

Part Description	Manufacturer	Part Number
ERF8 10X2, female	Samtec	ERF8-010-05.0-D-DV-L
Mating Cable		
6" coax cable assembly	Samtec	ERCD-010-06.00-TED-TEU-1-D

S/PDIF Optical Rx (`J11`)

Part Description	Manufacturer	Part Number
Fiber optic receiver	Everlight	PLR135/T10
Mating Cable		
Standard TOSLINK optical digital cable		

Audio Output (`J10`)

Part Description	Manufacturer	Part Number
RCA 4x2 female	Switchcraft	PJRAS4X2U
Mating Cable		
Standard audio cable with RCA connectors		

S/PDIF Digital (`J11`)

Part Description	Manufacturer	Part Number
RCA 1x2 female	Switchcraft	PJRAS1X2S02X
Mating Cable		
Standard S/PDIF cable with RCA connectors		

MLB (`J12`)

Part Description	Manufacturer	Part Number
40-pin high speed socket	Samtec	QSH-020-01-L-D-DP-A
Mating Connector		
40-pin high speed header	Samtec	QTH-0202-01-L-D-DP-A

Headphone (`J13`)

Part Description	Manufacturer	Part Number
3.5mm headphone connector	CUI	SJ1-3525NG
Mating Cable		
Standard audio cable with 3.5mm connector		

HADC (`P1 and J4`)

Part Description	Manufacturer	Part Number
SMB jack	Emerson	131-3711-201
Mating Cable		
Standard SMB cable		

JTAG (`P4`)

The JTAG header provides debug connectivity for the processor. This is a 0.05" shrouded through-hole connector from SAMTEC (SHF-105-01-L-D-SM-K). This connector mates with ICE- 1000, ICE-2000, and any newer Analog Devices emulators. For more information, see Debug Interface

Sigma Studio (`P5`)

This connector interfaces with SigmaStudio® through the EVAL-ADUSB2EBZ board. The connector is a 0.1" header. The pinout can be found in the schematic.

Trace and JTAG (`P8`)

The Trace and JTAG connector provides connectivity to the processor's trace interface. This is a MICTOR connector from TYCO (2-5767004-2). At this time, there are no trace pods available.

USB to UART(`P11`)

Part Description	Manufacturer	Part Number
USB Micro-AB	Hirose	ZX62D-AB-5P8
Mating Cable		
USB Micro-B to Standard-A cable		

A^{2}B (`P10 and P11`)

Part Description	Manufacturer	Part Number
2-pin DuraClik	Molex	5023520200
Mating Cable		
DuraClik cable assembly		

Engine RPM (`P12`)

Part Description	Manufacturer	Part Number
IDC 2x1 0.1"	Samtec	HTSW-102-07-T-S
Mating Cable		
Custom cable assembly		

Microphone (`P13-P16`)

Part Description	Manufacturer	Part Number
IDC 2x1 0.1"	Samtec	HTSW-102-07-T-S
Mating Cable		
Custom cable assembly		

Power Plug (`P10`)

Part Description	Manufacturer	Part Number
2.1 mm power jack	CUI	PJ-102AH
Mating Cable		

Part Description	Manufacturer	Part Number
12.0VDC@1.5A power supply	CUI	EMSA120150-P5RP-SZ

Power Terminal Block (`P22`)

Part Description	Manufacturer	Part Number
5.08mm power jack	Weidmuller	1760510000
Mating Cable		
12.0VDC discrete wires		

Expansion Interface 3 (`P9` and `P7`)

Part Description	Manufacturer	Part Number
120-pin, 0.6 mm	Hirose	FX8-120P-SV1(91)
Mating Connector		
120-pin, 0.6 mm	Hirose	FX8-120S-SV(21)