ANALOG DEVICES

DSP Microcomputer

ADSP-2171/ADSP-2172/ADSP-2173

OBSOLETE

FEATURES

30 ns Instruction Cycle Time (33 MIPS) from 16.67 MHz Crystal at 5.0 V
50 ns Instruction Cycle Time (20 MIPS) from 10 MHz Crystal at 3.3 V
ADSP-2100 Family Code & Function Compatible with New Instruction Set Enhancements for Bit Manipulation Instructions, Multiplication Instructions, Biased Rounding, and Global Interrupt Masking
Bus Grant Hang Logic
2K Words of On-Chip Program Memory RAM
2K Words of On-Chip Data Memory RAM
8K Words of On-Chip Program Memory ROM (ADSP-2172)
8- or 16-Bit Parallel Host Interface Port
300 mW Typical Power Dissipation at 5.0 V at 30 ns
70 mW Typical Power Dissipation at 3.3 V at 50 ns
Powerdown Mode Featuring Less than 0.55 mW (ADSP-2171/ADSP-2172) or 0.36 mW (ADSP-2173) CMOS Standby Power Dissipation with 100 Cycle Recovery from Powerdown
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides
Zero Overhead Looping
Conditional Instruction Execution
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Host Interface Port
Stand-Alone ROM Execution (Optional)
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
128-Lead TQFP and 128-Lead PQFP

GENERAL DESCRIPTION

The ADSP-2171, ADSP-2172, and ADSP-2173 are single-chip microcomputers optimized for digital signal processing (DSP) and other high-speed numeric processing applications. The ADSP-2171 and ADSP-2172 are designed for 5.0 V applications. The ADSP-2173 is designed for 3.3 V applications. The ADSP-2172 also has 8K words (24-bit) of program ROM.

REV. A

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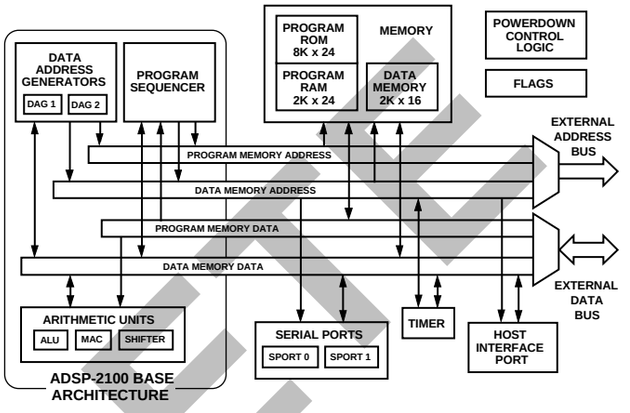
FUNCTIONAL BLOCK DIAGRAM



The ADSP-217x combines the ADSP-2100 base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a host interface port, a programmable timer, extensive interrupt capabilities, and on-chip program and data memory.

In addition, the ADSP-217x supports new instructions, which include bit manipulations–bit set, bit clear, bit toggle, bit test–new ALU constants, new multiplication instruction (x squared), biased rounding, and global interrupt masking, for increased flexibility. The ADSP-217x also has a Bus Grant Hang Logic ($\overline{BGH}$) feature.

The ADSP-217x provides 2K words (24-bit) of program RAM and 2K words (16-bit) of data memory. The ADSP-2172 provides an additional 8K words (24-bit) of program ROM. Powerdown circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-217x is available in 128-pin TQFP and 128-pin PQFP packages.

Fabricated in a high-speed, double metal, low power, CMOS process, the ADSP-217X operates with a 30 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-217x's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-217x can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- receive and transmit data through the two serial ports
- receive and/or transmit data through the host interface port
- decrement timer

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-217x. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-217x assembly source code. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

EZ-Tools, low cost, easy-to-use hardware tools, also support the ADSP-217x.

The ADSP-217x EZ-ICE® Emulator aids in the hardware debugging of ADSP-217x systems. The emulator consists of hardware, host computer resident software, the emulator probe, and the pin adaptor. The emulator performs a full range of emulation functions including stand-alone operation or operation in the target, setting up to 20 breakpoints, single-step or full-speed operation in the target, examining and altering registers and memory values, and PC upload/download functions. If you plan to use the emulator, you should consider the emulator's restrictions (differences between emulator and processor operation).

The EZ-LAB® Evaluation Board is a PC plug-in card, but it can operate in stand-alone mode. The evaluation board/system development board executes EPROM-based or downloaded programs. Modular Analog Front End daughter cards with different codecs will be made available.

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Additional Information

This data sheet provides a general overview of ADSP-217x functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*. For more information about the Development System and ADSP-217x programmer's reference information, refer to the *ADSP-2100 Family Assembler Tools & Simulator Manual*.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-217x. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-217x executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

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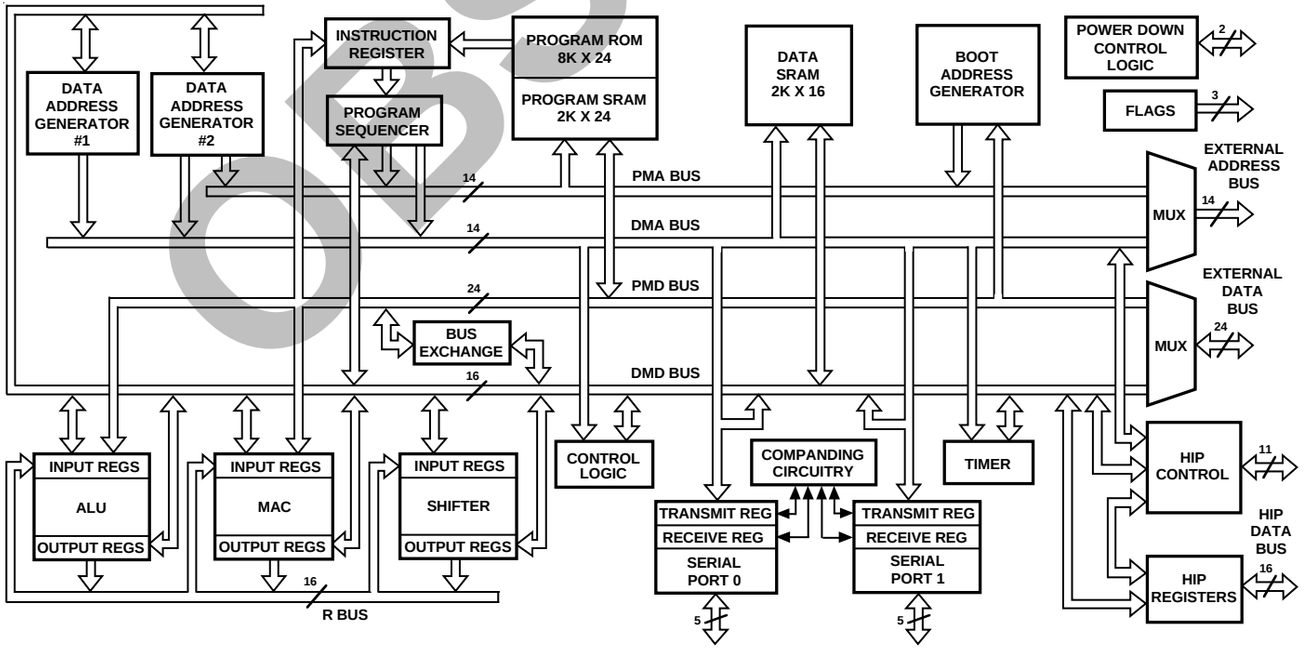

Figure 1. ADSP-217x Block Diagram

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus.

Program memory can store both instructions and data, permitting the ADSP-217x to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-217x can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-217x to continue running from internal memory. Normal execution mode requires the processor to halt while buses are granted.

In addition to the address and data bus for external memory connection, the ADSP-217x has a configurable 8- or 16-bit Host Interface Port (HIP) for easy connection to a host processor. The HIP is made up of 16 data/address pins and 11 control pins. The HIP is extremely flexible and provides a simple interface to a variety of host processors. For example, the Motorola 68000 series, the Intel 80C51 series and the Analog Devices' ADSP-2101 can be easily connected to the HIP. The host processor can initialize the ASDP-217x's on-chip memory through the HIP.

The ADSP-217x can respond to eleven interrupts. There can be up to three external interrupts, configured as edge or level sensitive, and eight internal interrupts generated by the Timer, the Serial Ports ("SPORTs"), the HIP, the powerdown circuitry, and software. There is also a master RESET signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, seven wait states are automatically generated. This allows, for example, a 30 ns ADSP-217x to use an external 200 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware. The on-chip program memory can also be initialized through the HIP.

The ADSP-217x features three general-purpose flag outputs whose states can be simultaneously changed through software. You can use these outputs to signal an event to an external device. In addition, the data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where *n-l* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-217x instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-217x assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Serial Ports

The ADSP-217x incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-217x SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

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Pin Description

The ADSP-217x is available in 128-lead TQFP and 128-lead PQFP packages. Table I contains the pin descriptions.

Table I. ADSP-217x Pin List

Pin Group Name	# of Pins	Input/ Output	Function
Address	14	O	Address output for program, data and boot memory spaces
Data	24	I/O	Data I/O pins for program and data memories. Input only for boot memory space, with two MSBs used as boot space addresses.
$\overline{\text{RESET}}$	1	I	Processor reset input
$\overline{\text{IRQ2}}$	1	I	External interrupt request #2
$\overline{\text{BR}}$	1	I	External bus request input
$\overline{\text{BG}}$	1	O	External bus grant output
$\overline{\text{BGH}}$	1	O	External bus grant hang output
$\overline{\text{PMS}}$	1	O	External program memory select
$\overline{\text{DMS}}$	1	O	External data memory select
$\overline{\text{BMS}}$	1	O	Boot memory select
$\overline{\text{RD}}$	1	O	External memory read enable
$\overline{\text{WR}}$	1	O	External memory write enable
MMAP	1	I	Memory map select
CLKIN, XTAL	2	I	External clock or quartz crystal input
CLKOUT	1	O	Processor clock output
$\overline{\text{HSEL}}$	1	I	HIP select input
$\overline{\text{HACK}}$	1	O	HIP acknowledge output
HSIZE	1		8/16 bit host select input 0 = 16-bit; 1 = 8-bit
BMODE	1	I	Boot mode select input 0 = EPROM/data bus; 1 = HIP
HMD0	1	I	Bus strobe select input 0 = RD, WR; 1 = RW, DS
HMD1	1	I	HIP address/data mode select input 0 = separate; 1 = multiplexed
$\overline{\text{HRD}}$/HRW	1	I	HIP read strobe/read/write select input
$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	1	I	HIP write strobe/host data strobe select input
HD15–0/ HAD15-0	16	I/O	HIP data/data and address
HA2/ALE	1	I	Host address 2/Address latch enable input
HA1–0/ Unused	2	I	Host addresses 1 and 0 inputs
SPORT0	5	I/O	Serial port 0 I/O pins (TFS0, RFS0, DT0, DR0, SCLK0)
SPORT1 or $\overline{\text{IRQ1}}$ (TFS1)	5	I/O	Serial port 1 I/O pins
$\overline{\text{IRQ0}}$ (RFS1)	1	I	External interrupt request #1
SCLK1	1	O	External interrupt request #0
FO (DT1)	1	O	Programmable clock output
FI (DR1)	1	I	Flag Output pin
FL2–0	3	O	Flag Input pin
V_{DD}	6		General purpose flag output pins
GND	11		Power supply pins
$\overline{\text{PWD}}$	1	I	Ground pins
PWDACK	1	O	Powerdown pin
			Powerdown acknowledge pin

Host Interface Port

The ADSP-217x host interface port is a parallel I/O port that allows for an easy connection to a host processor. Through the HIP, the ADSP-217x can be used as a memory-mapped peripheral to a host computer. The HIP can be thought of as an area of dual-ported memory, or mailbox registers, that allow communication between the computational core of the ADSP-217x and the host computer.

The HIP is completely asynchronous. The host processor can write data into the HIP while the ADSP-217x is operating at full speed.

The HIP can be configured with the following pins:

- HSIZE configures HIP for 8-bit or 16-bit communication with the host processor.
- BMODE (when MMAP = 0) determines whether the ADSP-217x boots from the host processor (through the HIP) or external EPROM (through the data bus).
- HMD0 configures the bus strobes as separate read and write strobes, or a single read/write select and a host data strobe.
- HMD1 selects separate address (3-bit) and data (16-bit) buses, or a multiplexed, 16-bit address/data bus with address latch enable.

Tying these pins to appropriate values configures the ADSP-217x for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

In 8-bit reads, the ADSP-217x three-states the upper eight bits of the bus. When the host processor writes an 8-bit value to the HIP, the upper eight bits are all zeros. For additional information refer to the *ADSP-2100 Family User's Manual.*

HIP Operation

The HIP contains six data registers (HDR5–0) and two status registers (HSR7–6) with an associated HMASK register for masking interrupts from individual HIP data registers. All HIP data registers are memory-mapped into the internal data memory of the ADSP-217x. HIP transfers can be managed using either interrupts or a polling scheme. These registers are shown in the section "ADSP-217x Registers."

The HIP allows a software reset to be performed by the host processor. The internal software reset signal is asserted for five ADSP-217x processor cycles.

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Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-217x provides up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$. $\overline{IRQ2}$ is always available as a dedicated pin; SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, and the flags. The ADSP-217x also supports internal interrupts from the timer, the host interface port, the two serial ports, software, and the powerdown control circuit. The interrupt levels are internally prioritized and individually maskable (except powerdown and reset). The input pins can be programmed to be either level- or edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table II, and the interrupt registers are shown in Figure 2.

Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected.The powerdown interrupt is nonmaskable.

The ADSP-217x masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect autobuffering.

The interrupt control register, ICNTL, allows the external interrupts to be either edge- or level-sensitive. Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially.

The IFC register is a write-only register used to force and clear interrupts generated from software.

Table II. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (*Highest Priority*)
Powerdown (Nonmaskable)	002C
$\overline{IRQ2}$	0004
HIP Write	0008
HIP Read	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
Software Interrupt 1	0018
Software Interrupt 0	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (*Lowest Priority*)

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling.

The stacks are twelve levels deep to allow interrupt nesting.

The following instructions allow global enable or disable servicing of the interrupts (including powerdown), regardless of the state of IMASK. Disabling the interrupts does not affect autobuffering.

ENA INTS;
DIS INTS;

When you reset the processor, the interrupt servicing is enabled.

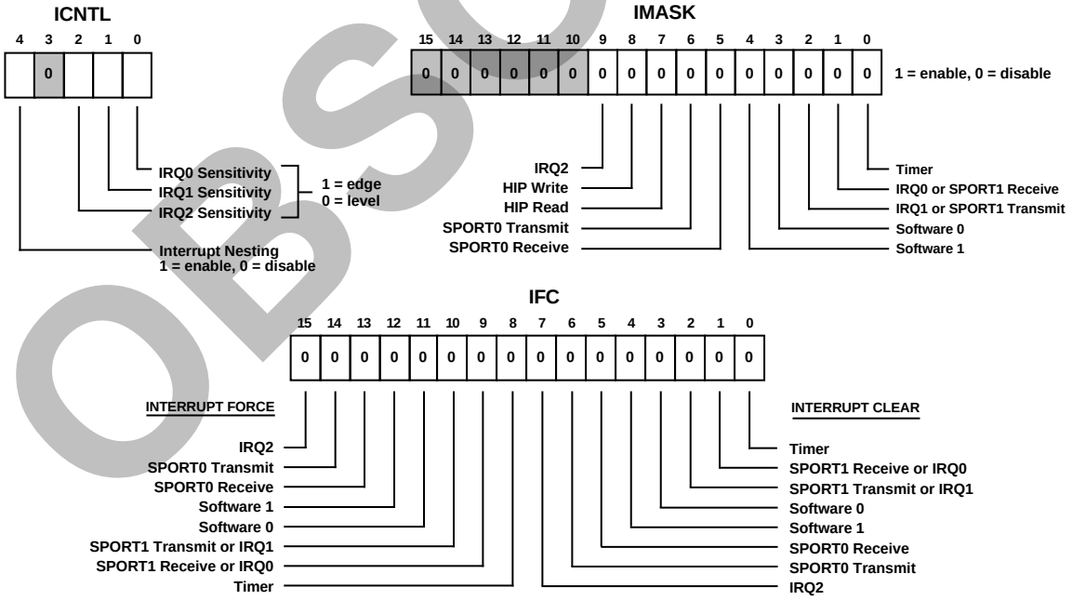

Figure 2. Interrupt Registers

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LOW POWER OPERATION

The ADSP-217x has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Powerdown
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation. The CLKOUT pin is controlled by Bit 14 of SPORT0 Autobuffer Control Register, DM[0x3FF3].

Powerdown

The ADSP-217x processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of powerdown features. Refer to the *ADSP-2100 Family User's Manual*, Chapter 9 "System Interface" for detailed information about the powerdown feature.

- Powerdown mode holds the processor in CMOS standby with a maximum current of less than 100 µA in some modes.
- Quick recovery from powerdown. The processor begins executing instructions in as few as 100 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during powerdown without affecting the lowest power rating and 100 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 100 CLKIN cycle startup.
- Powerdown is initiated by either the powerdown pin ($\overline{\text{PWD}}$) or the software powerdown force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The powerdown interrupt also can be used as a non-maskable, edge sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the powerdown state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate powerdown, and the host software reset feature can be used to terminate powerdown under certain conditions.
- Powerdown acknowledge pin indicates when the processor has entered powerdown.

Idle

When the ADSP-217x is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the *IDLE* instruction.

Slow Idle

The *IDLE* instruction is enhanced on the ADSP-217x to let the processor's internal clock signal be slowed during *IDLE*, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the *IDLE* instruction. The format of the instruction is

IDLE (n);

where *n* = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts—the 1-cycle response time of the standard idle state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-217x will remain in the idle state for up to a maximum of *n* processor cycles (*n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of *n* processor cycles).

SYSTEM INTERFACE

Figure 3 shows a basic system configuration with the ADSP-217x, two serial devices, a host processor, a boot EPROM, and optional external program and data memories. Up to 14K words of data memory and 16K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories. The ADSP-217x also provides one external interrupt and two serial ports or three external interrupts and one serial port.

Clock Signals

The ADSP-217x can be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the Powerdown State. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual* for detailed information on this powerdown feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

The ADSP-217x uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock yields a 30 ns processor cycle (which is equivalent to 33 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

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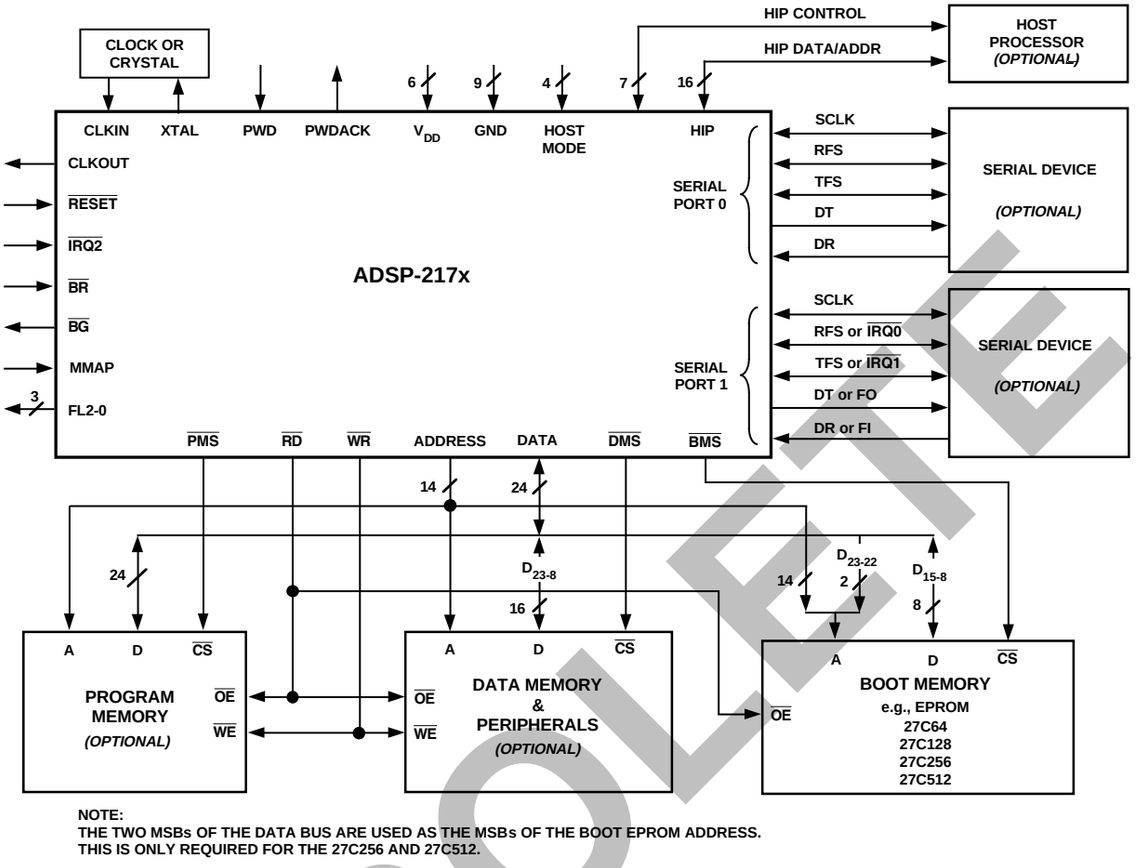

NOTE:
THE TWO MSBs OF THE DATA BUS ARE USED AS THE MSBs OF THE BOOT EPROM ADDRESS.
THIS IS ONLY REQUIRED FOR THE 27C256 AND 27C512.

Figure 3. ADSP-217x Basic System Configuration

Because the ADSP-217x includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

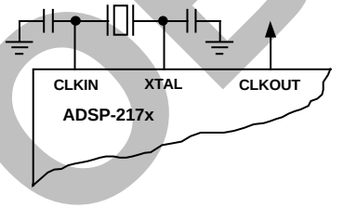

Figure 4. External Crystal Connections

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register, DM[0x3FF3].

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-217x. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000.

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Program Memory Interface

The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip DMA and DMD buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 16K words. 10K words of memory for ADSP-217x with optional 8K ROM and 2K words of memory for the non-ROM version are on-chip. The data bus is bidirectional and 24 bits wide to external program memory. Program memory may contain code and data.

The program memory data lines are bidirectional. The program memory select ($\overline{PMS}$) signal indicates access to the program memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and is used as a write strobe.

The read ($\overline{RD}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-217x writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps

ADSP-217x

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 5 shows the different configurations. When MMAP = 0, internal RAM occupies 2K words beginning at address 0x0000. In this configuration, the boot loading sequence (described in "Boot Memory Interface") is automatically initiated when $\overline{RESET}$ is released.

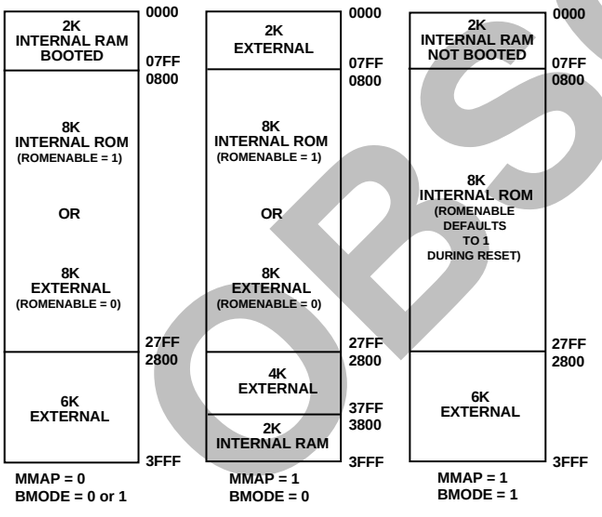


Figure 5. ADSP-217x Memory Maps

When MMAP = 1, words of external program memory begin at address 0x0000 and internal RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, program memory is not loaded although it can be written to and read from under program control.

The optional ROM always resides at locations PM[0x0800] through PM[0x27FF] regardless of the state of the MMAP pin. The ROM is enabled by setting the ROMENABLE bit in the Data Memory Wait State control register, DM[0x3FFE]. When the ROMENABLE bit is set to 1, addressing program memory in this range will access the on-chip ROM. When set to zero, addressing program memory in this range will access external program memory. The ROMENABLE bit is set to 0 on chip reset unless MMAP *and* BMODE = 1.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{RESET}$.

Boot Memory Interface

The ADSP-217x can load on-chip memory from external boot memory space. The boot memory space consists of 64K by 8-bit space, divided into eight separate 8K by 8-bit pages. Three bits in the system control register select which page is loaded by the boot memory interface. Another bit in the system control register allows the user to force a boot loading sequence under software control. Boot loading from page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate 0 to 7 wait states; it defaults to 7 wait states after $\overline{RESET}$. This allows the ADSP-217x to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8–D15. To accommodate addressing up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot space address.

The ADSP-2100 Family Assembler and Linker support the creation of programs and data structures requiring multiple boot pages during execution.

$\overline{RD}$ and $\overline{WR}$ must always be qualified by $\overline{PMS}$, $\overline{DMS}$, or $\overline{BMS}$ to ensure the correct program, data, or boot memory accessing.

HIP Booting

The ADSP-217x can also boot programs through its Host Interface Port. If BMODE = 1 and MMAP = 0, the ADSP-217x boots from the HIP. If BMODE = 0, the ADSP-217x boots through the data bus (in the same way as the ADSP-2101), as described above in "Boot Memory Interface." For additional information about HIP booting, refer to the *ADSP-2100 Family User's Manual*, Chapter 7, "Host Interface Port."

The ADSP-2100 Family Development Software includes a utility program called the HIP Splitter. This utility allows the creation of programs that can be booted via the ADSP-217x's HIP, in a similar fashion as EPROM-bootable programs generated by the PROM Splitter utility.

OBSOLETE

Stand-Alone ROM Execution
When the MMAP and BMODE pins both are set to 1, the ROM is automatically enabled and execution commences from program memory location 0x0800 at the start of ROM. This feature lets an embedded design operate without external memory components. To operate in this mode, the ROM coded program must copy an interrupt vector table to the appropriate locations in program memory RAM. In this mode, the ROM enable bit defaults to 1 during reset.

Table III. Boot Summary Table

	BMODE = 0	BMODE = 1
MMAP = 0	Boot from EPROM, then execution starts at internal RAM location 0x0000	Boot from HIP, then execution starts at internal RAM location 0x0000
MMAP = 1	No booting, execution starts at external memory location 0x0000	Stand-Alone Mode, execution starts at internal ROM location 0x0800

Ordering Procedure for ADSP-2172 Processors
To place an order for a custom ROM-coded ADSP-2172 processor, you must:

1. Complete the following forms contained in the *ADSP ROM Ordering Package*, available from your Analog Devices sales representative:

   ADSP-2172 ROM Specification Form
   ROM Release Agreement
   ROM NRE Agreement & Minimum Quantity Order (MQO) Acceptance Agreement for Pre-production ROM Products.
2. Return the forms to Analog Devices along with two copies of the Memory Image File (.EXE file) of your ROM code. The files must be supplied on two 3.5" or 5.25" floppy disks for IBM PC (DOS 2.01 or higher).
3. Place a purchase order with Analog Devices for nonrecurring engineering charges (NRE) associated with ROM product development.

After this information is received, it is entered into Analog Devices' ROM Manager System which assigns a custom ROM model number to the product. This model number will be branded on all prototype and production units manufactured to these specifications.

To minimize the risk of code being altered during this process, Analog Devices verifies that the .EXE files on both floppy disks are identical, and recalculates the checksums for the .EXE file entered into the ROM Manager System. The checksum data, in the form of a ROM memory map, a hard copy of the .EXE file, and a ROM Data Verification Form are returned to you for inspection.

A signed ROM Verification Form and a purchase order for production units are required prior to any product being manufactured. Prototype units may be applied toward the minimum order quantity.

Upon completion of the prototype manufacture, Analog Devices will ship prototype units and a delivery schedule update for production units. An invoice against your purchase order for the NRE charges is issued at this time.

There is a charge for each ROM mask generated and a minimum order quantity. Consult your sales representative for details. A separate order must be placed for parts of a specific package type, temperature range, and speed grade.

Data Memory Interface
The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits (D8–D23) used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to the data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-217x supports memory-mapped I/O, with the peripherals memory mapped into the data or program memory address spaces and accessed by the processor in the same manner.

Data Memory Map
The on-chip data memory RAM resides in the 2K words of data memory beginning at address 0x3000, as shown in Figure 6. In addition, data memory locations from 0x3800 to the end of data memory at 0x3FFF are reserved. Control registers for the system, timer, wait state configuration, host interface port, and serial port operations are located in this region of memory.

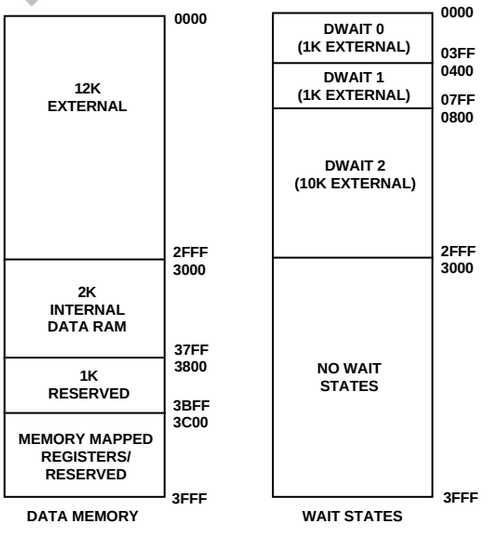


Figure 6. ADSP-217x Data Memory Map

The remaining 12K of data memory is external. External data memory is divided into three zones, each associated with its own wait state generator. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{RESET}$. For compatibility with other ADSP-2100 Family processors, bit definitions for DWAIT 3 and DWAIT4 are shown in the Data Memory Wait State Control Register, but they are not used by the ADSP-217x.

OBSOLETE

Bus Request & Bus Grant

The ADSP-217x can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-217x is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If the Go Mode is enabled, the ADSP-217x will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-217x is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes, which can be up to eight cycles later depending on the number of wait states. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The new Bus Grant Hang logic and associated $\overline{BGH}$ pin allow the ADSP-217x to operate in a multiprocessor environment with a minimal number of "wasted" processor cycles. The bus grant hang pin is asserted when the ADSP-217x desires a cycle, but cannot execute it because the bus is granted to some other processor. With the $\overline{BGH}$ signal, the other processor(s) in the system can be alerted that the ADSP-217x is hung and release the bus by deasserting bus request. Once the bus is released the ADSP-217x executes the external access and deasserts $\overline{BGH}$. This is a signal to the other processors that external memory is now available.

ADSP-217X REGISTERS

Figure 7 summarizes all the registers in the ADSP-217x. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

A secondary set of registers in all computational units allows a single-cycle context switch.

The bit and field definitions for control and status registers are given in the rest of this section, except for IMASK, ICNTL and IFC, which are defined earlier in this data sheet. The system control register, DWAIT register, timer registers, HIP control registers, HIP data registers, and SPORT control registers are all mapped into data memory; that is, registers are accessed by reading and writing data memory locations rather than register names. The particular data memory address is shown with each memory-mapped register.

Register bit values shown on the following pages are the default bit values after reset. If no values are shown, the bits are indeterminate at reset. Reserved bits are shown in gray; these bits should always be written with zeros.

OBSOLETE

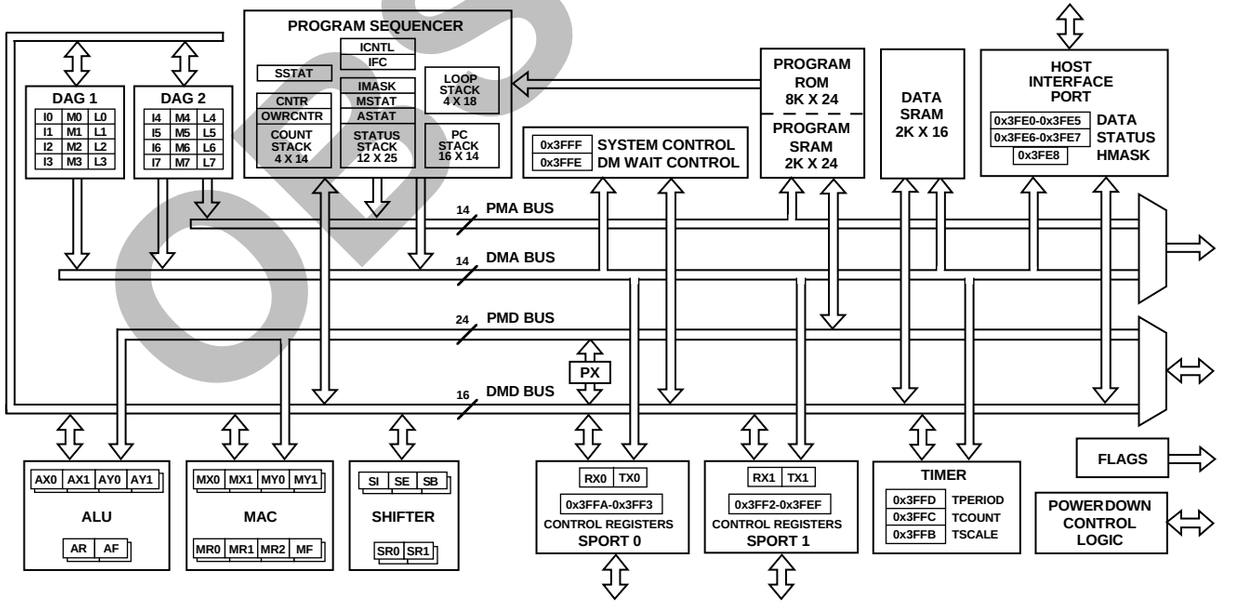
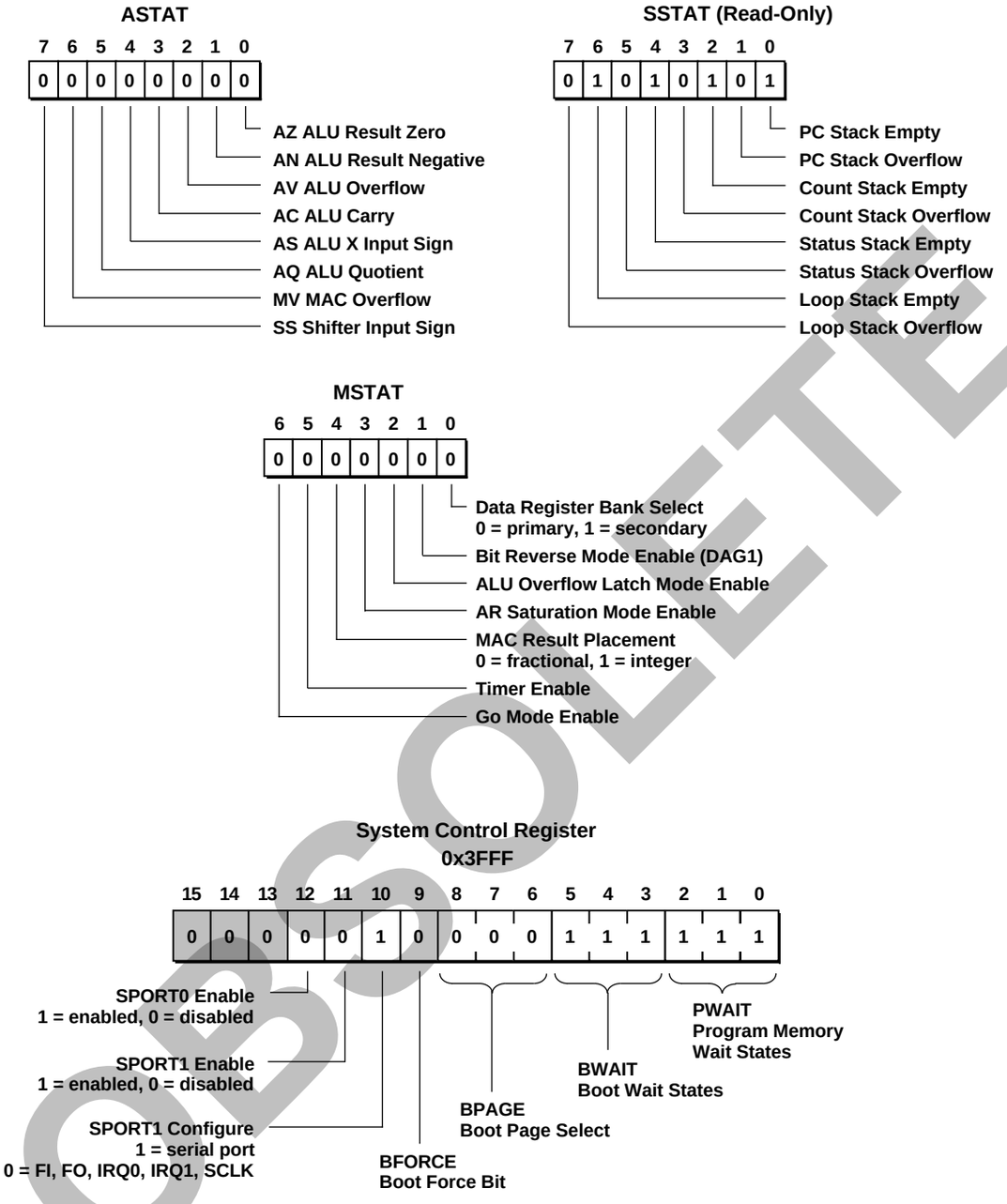
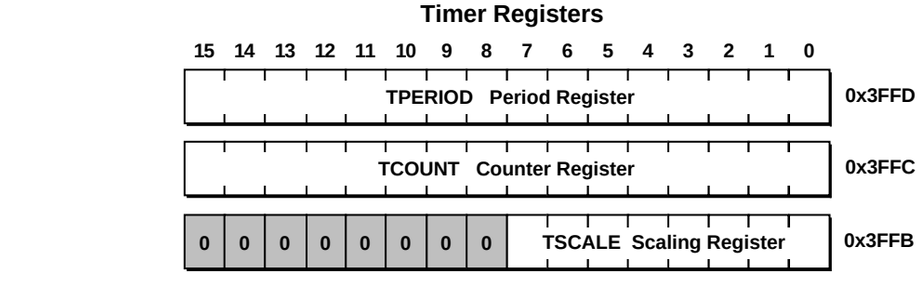


Figure 7. ADSP-217x Registers Control Register

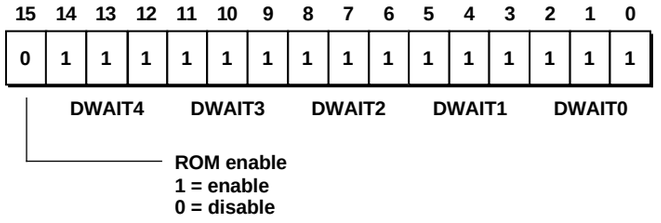




Control Registers

OBSOLETE

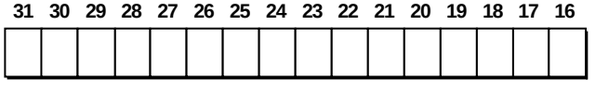
ROM Enable/Data Memory Wait State Control Register
0x3FFE



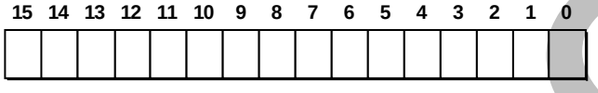
SPORT0 Multichannel Receive Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FFA



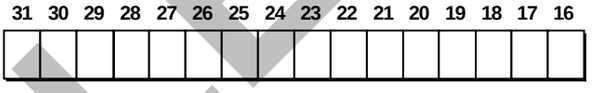
0x3FF9



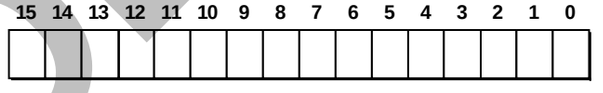
SPORT0 Multichannel Transmit Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

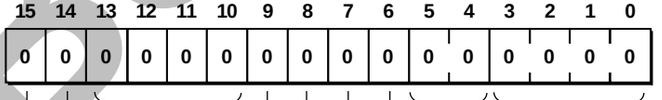
0x3FF8



0x3FF7



SPORT0 Control Register
0x3FF6



Multichannel Enable MCE

Internal Serial Clock Generation ISCLK

Receive Frame Sync Required RFSR

Receive Frame Sync Width RFSW

Multichannel Frame Delay MFD
Only If Multichannel Mode Enabled

Transmit Frame Sync Required TFSR

Transmit Frame Sync Width TFSW

ITFS Internal Transmit Frame Sync Enable
(or MCL Multichannel Length; 1 = 32 words, 0 = 24 words
Only If Multichannel Mode Enabled)

SLEN Serial Word Length

DTYPE Data Format
00 = right justify, zero-fill unused MSBs
01 = right justify, sign extend into unused MSBs
10 = compand using μ-law
11 = compand using A-law

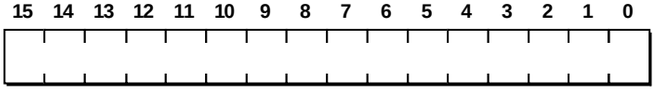
INVRFS Invert Receive Frame Sync

INVTFS Invert Transmit Frame Sync
(or INVTDV Invert Transmit Data Valid
Only If Multichannel Mode Enabled)

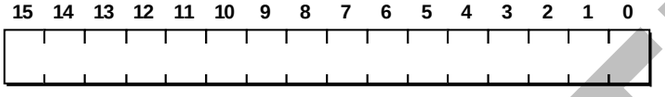
IRFS Internal Receive Frame Sync Enable

OBSOLETE

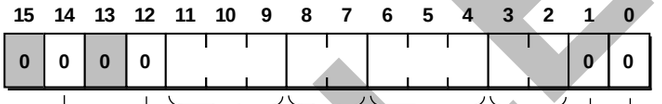
SPORT0 SCLKDIV
Serial Clock Divide Modulus
0x3FF5



SPORT0 RFSDIV
Receive Frame Sync Divide Modulus
0x3FF4



SPORT0 Autobuffer Control Register
0x3FF3



CLKODIS
CLKOUT Disable Control Bit

BIASRND
MAC Biased Rounding Control Bit

TIREG
Transmit Autobuffer I Register

TMREG
Transmit Autobuffer M Register

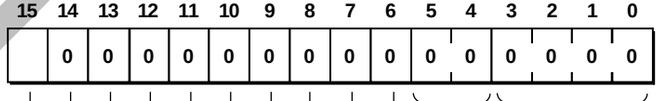
RBUF
Receive Autobuffering Enable

TBUF
Transmit Autobuffering Enable

RMREG
Receive Autobuffer M Register

RIREG
Receive Autobuffer I Register

SPORT1 Control Register
0x3FF2



Flag Out (Read Only)

Internal Serial Clock Generation ISCLK

Receive Frame Sync Required RFSR

Receive Frame Sync Width RFSW

Transmit Frame Sync Required TFSR

Transmit Frame Sync Width TFSW

ITFS Internal Transmit Frame Sync Enable

SLEN Serial Word Length

DTYPE Data Format
00 = right justify, zero-fill unused MSBs
01 = right justify, sign extend into unused MSBs
10 = compand using μ-law
11 = compand using A-law

INVRFS Invert Receive Frame Sync

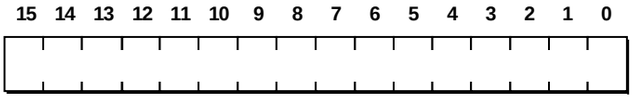
INVTFS Invert Transmit Frame Sync

IRFS Internal Receive Frame Sync Enable

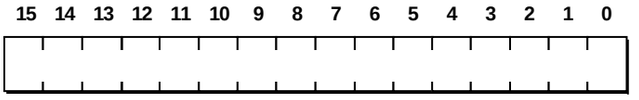
OBSOLETE

Control Registers

SPORT1 SCLKDIV
Serial Clock Divide Modulus
0x3FF1



SPORT1 RFSDIV
Receive Frame Sync Divide Modulus
0x3FF0



SPORT1 Autobuffer Control Register
0x3FEF

XTALDIS
XTAL Pin Drive Disable during Powerdown
1 = disabled, 0 = enabled
(disable XTAL pin when no external crystal connected)

XTALDELAY
4096 Cycle Delay Enable
1 = delay, 0 = no delay

PDFORCE
Powerdown Force

PUCR
Powerup Context Reset Enable
1 = soft reset (context clear),
0 = resume execution

RBUF
Receive Autobuffer Enable

TBUF
Transmit Autobuffer Enable

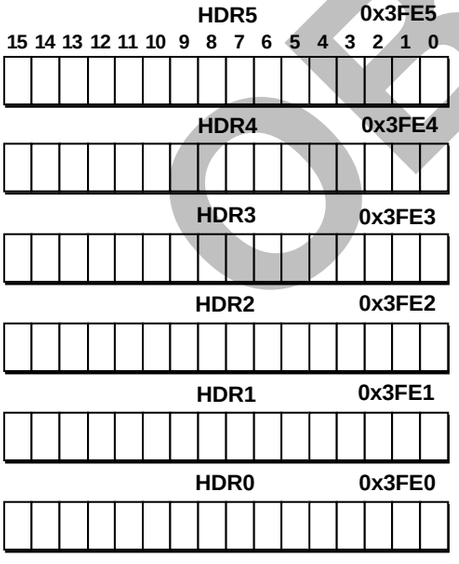
RMREG
Receive M Register

RIREG
Receive I Register

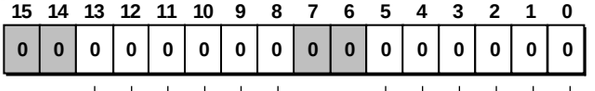
TMREG
Transmit M Register

TIREG
Transmit I Register

HIP Data Registers



HMASK Register
0x3FE8



Host HDR5 Read

Host HDR4 Read

Host HDR3 Read

Host HDR2 Read

Host HDR1 Read

Host HDR0 Read

Interrupt Enables
1 = Enable
0 = Disable

Host HDR0 Write

Host HDR1 Write

Host HDR2 Write

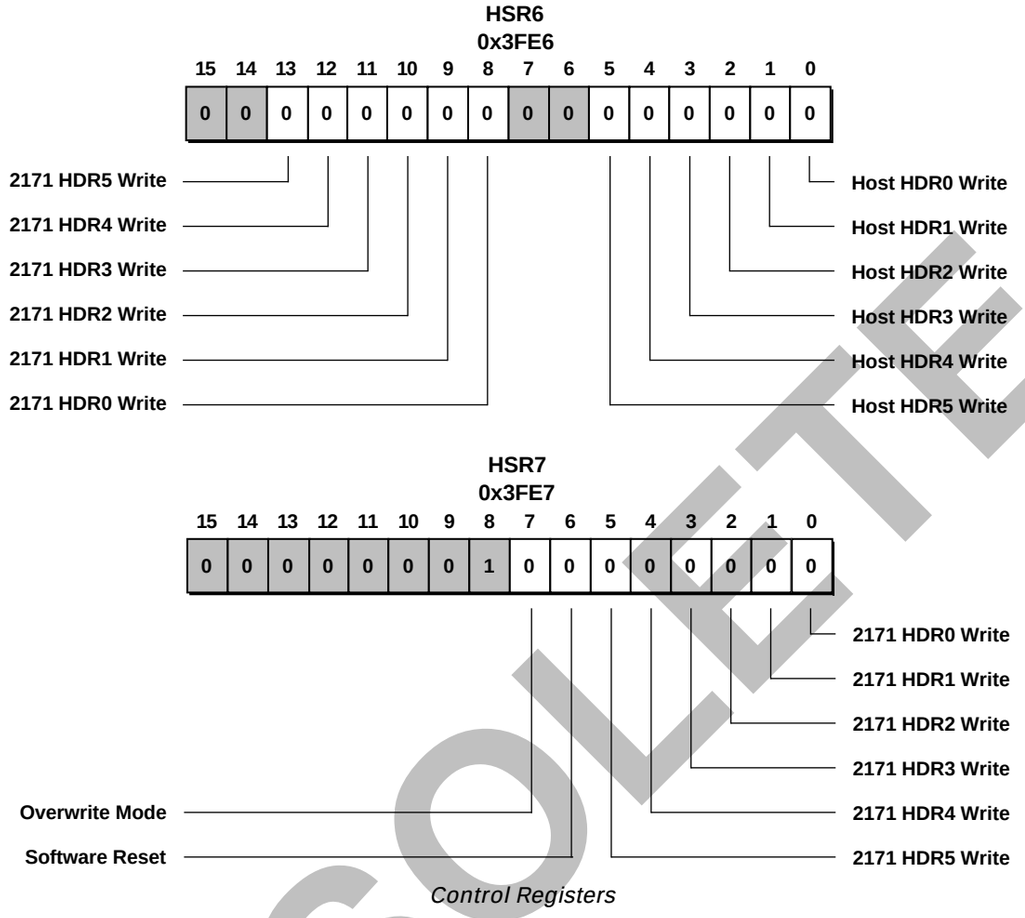
Host HDR3 Write

Host HDR4 Write

Host HDR5 Write

OBSOLETE

Control Registers



Control Registers

Biased Rounding

A new mode allows biased rounding in addition to the normal unbiased rounding. When the BIASRND bit is set to 0, the normal unbiased rounding operations occur. When the BIASRND bit is set to 1, biased rounding occurs instead of the normal unbiased rounding. When operating in biased rounding mode all rounding operations with MR0 set to 0x8000 will round up, rather than only rounding odd MR1 values up. For example:

MR value before RND	biased RND result	unbiased RND result
00-0000-8000	00-0001-8000	00-0000-8000
00-0001-8000	00-0002-8000	00-0002-8000
00-0000-8001	00-0001-8001	00-0001-8001
00-0001-8001	00-0002-8001	00-0002-8001
00-0000-7FFF	00-0000-7FFF	00-0000-7FFF
00-0001-7FFF	00-0001-7FFF	00-0001-7FFF

This mode only has an effect when the MR0 register contains 0x8000, all other rounding operation work normally. This mode was added to allow more efficient implementation of bit specified algorithms which specify biased rounding such as the GSM speech compression routines. Unbiased rounding is preferred for most algorithms.

Note: BIASRND bit is Bit 12 of the SPORT0 Autobuffer Control register.

INSTRUCTION SET DESCRIPTION

The ADSP-217x assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize internal memory and conform to the ADSP-217x's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

Consult the *ADSP-2100 Family User's Manual* for a complete description of the syntax and an instruction set reference.

OBSOLETE

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
  MF=MX0*MY1 (RND), MX0=DM (I2,M1);   /* MF=error*beta */
  MR=MX0*MF (RND), AY0=PM (I6,MS);
DO adapt UNTIL CE;
  AR=MR1 + AY0, MX0=DM (I2,M1), AY0=PM (I6,M7);
adapt:  PM(I6,M6) =AR, MR=MX0*MF (RND);
        MODIFY (I2, M3);            /* Point to oldest data */
        MODIFY (I6, M7);            /* Point to start of data */
```

Interrupt Enable

The ADSP-217x supports an interrupt enable instruction. Interrupts are enabled by default at reset. The instruction source code is specified as follows:

Syntax: ENA INTS;

Description: Executing the ENA INTS instruction allows all unmasked interrupts to be serviced again.

Interrupt Disable

The ADSP-217x supports an interrupt disable instruction. The instruction source code is specified as follows:

Syntax: DIS INTS;

Description: Reset enables interrupt servicing. Executing the DIS INTS instruction causes all interrupts to be masked without changing the contents of the IMASK register. Disabling interrupts does not affect the autobuffer circuitry, which will operate normally whether or not interrupts are enabled. The disable interrupt instruction masks all user interrupts including the powerdown interrupt.

OBSOLETE

ADSP-2171/ADSP-2172–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	4.5	5.5	4.5	5.5	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IH}	Hi-Level RESET Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[6]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = V_{DD} max[8]		10	µA
I_{OZL}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V[8]		10	µA
I_{DD}	Supply Current (Idle)[9, 10]	@ V_{DD} = max		18	mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DD} = max, t_{CK} = 30 ns[11]		75	mA
I_{DD}	Supply Current (Powerdown)[10]	Lowest Power Mode[12]		100	µA
C_I	Input Pin Capacitance[3, 6, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[6, 7, 13, 14]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES

[1]Bidirectional pins: D0-D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, HD0-HD15/HAD0-HAD15.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, $\overline{\text{PWD}}$, HA2/ALE, HA1-0.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, $\overline{\text{PWD}}$, HA2/ALE, HA1-0.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0-A13, DT0, DT1, CLKOUT, $\overline{\text{HACK}}$, FL2-0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2171/ADSP-2172 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0-A13, D0-D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RSF1, HD0-HD15/HAD0-HAD15.

[8]0 V on $\overline{\text{BR}}$, CLKIN Active (to force three-state condition).

[9]Idle refers to ADSP-2171/ADSP-2172 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND. Current reflects device operation with CLKOUT disabled.

[10]Current reflects device operating with no output loads.

[11]V_{IN} = 0.4 V and 2.4 V. For typical figures for supply currents, refer to "Power Dissipation" section.

[12]See Chapter 9, of the *ADSP-2100 Family User's Manual* for details.

[13]Applies to TQFP and PQFP package types.

[14]Output pin capacitance is the capacitive load for any three-state output pin.

Specifications subject to change without notice.

OBSOLETE

ADSP-2171/ADSP-2172

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) TQFP . . . . . +280°C
Lead Temperature (5 sec) PQFP . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-217x is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-217x features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-217x has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

OBSOLETE

ADSP-2171/ADSP-2172 TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also, use the switching characteristics to ensure any timing requirement of a device connected to the processor (such as memory) is satisfied.

ADSP-2171/ADSP-2172

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2171/ADSP-2172 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ before $\overline{WR}$ Deasserted	Setup Address Setup to Write End
t_{WRA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Clock Signals				
t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2171/ADSP-2172 uses an input clock with a frequency equal to half the instruction rate; a clock (which is equivalent to 60 ns) yields a 30 ns processor cycle 16.67 MHz input (equivalent to 33 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CKH} = 0.5t_{CK} – 7$ ns = 0.5 (30 ns) – 7 ns = 8 ns.				
Timing Requirement:				
t_{CKI}	CLKIN Period	60	150	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} – 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} – 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	RESET Width Low	$5t_{CK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

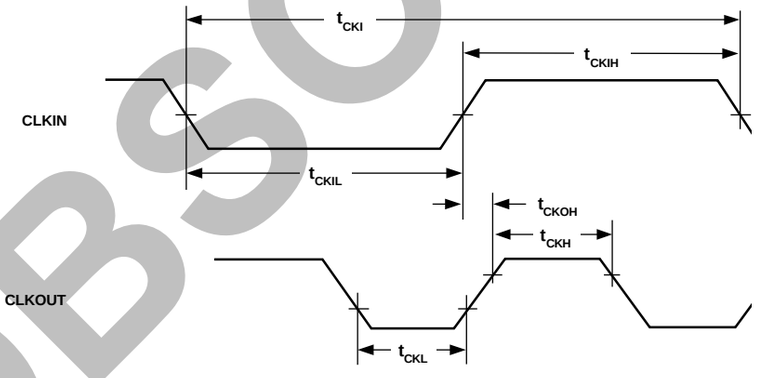


Figure 8. Clock Signals

OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	$\overline{IRQx}$ or FI Setup before CLKOUT Low[1, 2, 3]	$0.25t_{CK}$ + 15		ns
t_{IFH}	$\overline{IRQx}$ or FI Hold after CLKOUT High[1, 2, 3]	$0.25t_{CK}$		ns
Switching Characteristic:				
t_{FOH}	Flag Output Hold after CLKOUT Low[4]	$0.5t_{CK}$ – 7		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[4]		$0.5t_{CK}$ + 5	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[4]Flag Output = FL0, FL1, FL2, and FO.

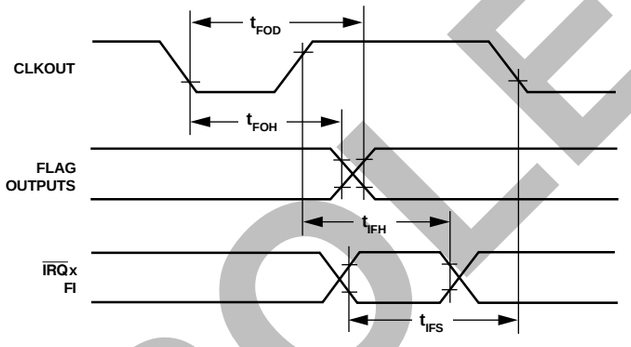


Figure 9. Interrupts and Flags

OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 2		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 17		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 16	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ – 7		ns
t_{SDBH}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

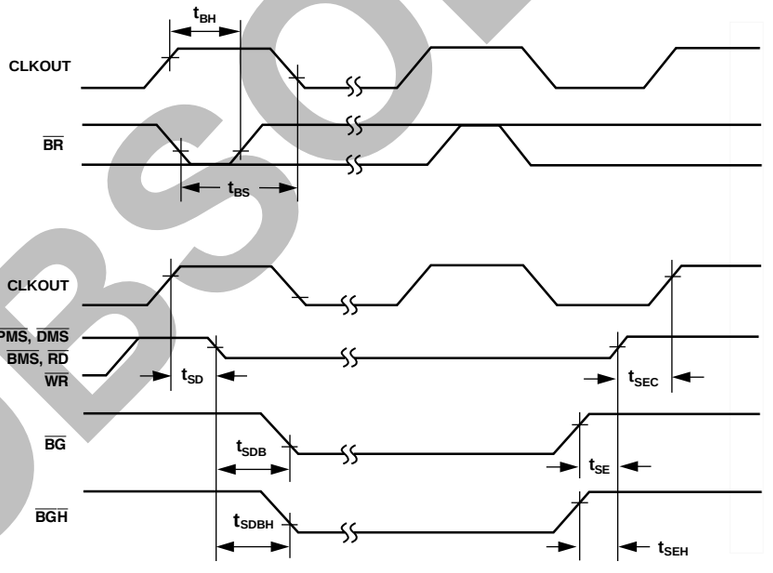


Figure 10. Bus Request–Bus Grant

OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 9 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 10.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}.

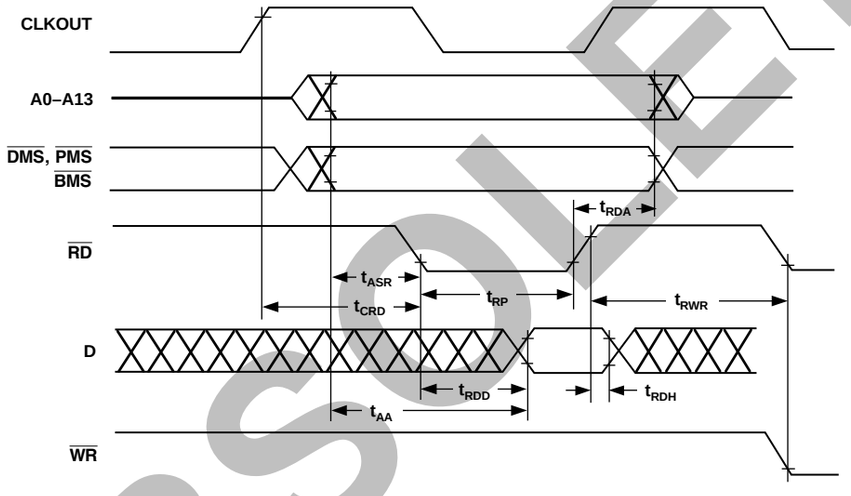


Figure 11. Memory Read

OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	0.5 t_{CK} – 7 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	0.25t_{CK} – 2		ns
t_{WP}	$\overline{WR}$ Pulse Width	0.5t_{CK} – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	0.25t_{CK} – 6		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	0.25t_{CK} – 7		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	0.25t_{CK} – 5	0.25 t_{CK} + 7	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	0.75t_{CK} – 9 + w		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	0.25t_{CK} – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5t_{CK} – 5		ns

w = wait states x t_{CK}.

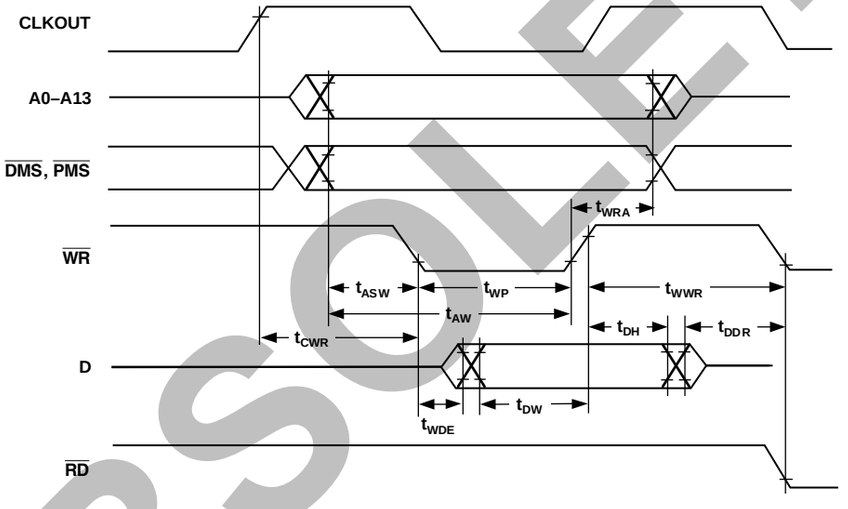


Figure 12. Memory Write

OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	50		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	20		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK}$ + 10	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS(Alt) to DT Enable	0		ns
t_{TDV}	TFS(Alt) to DT Valid		15	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

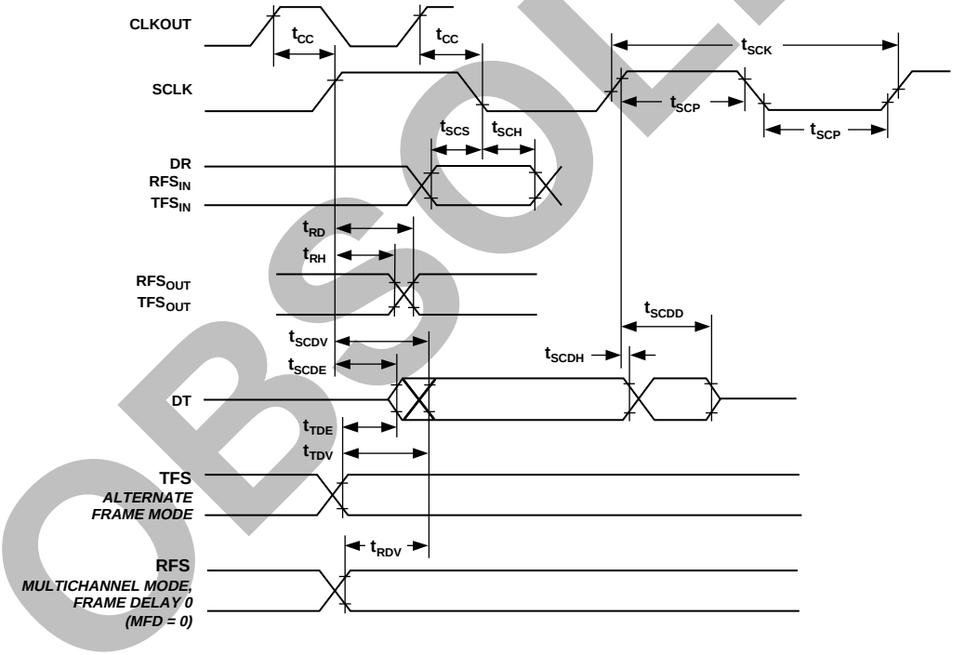


Figure 13. Serial Ports

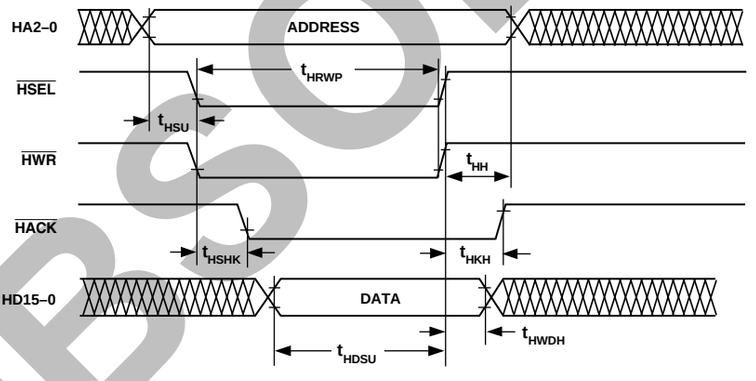
OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HSU}	HA2–0 Setup before Start of Write or Read[1, 2]	5		ns
t_{HDSU}	Data Setup before End of Write[3]	5		ns
t_{HWDH}	Data Hold after End of Write[3]	3		ns
t_{HH}	HA2–0 Hold after End of Write or Read[3, 4]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	15	ns
t_{HDE}	Data Enabled after Start of Read[2]	0		ns
t_{HDD}	Data Valid after Start of Read[2]		18	ns
t_{HRDH}	Data Hold after End of Read[4]	0		ns
t_{HRDD}	Data Disabled after End of Read[4]		7	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

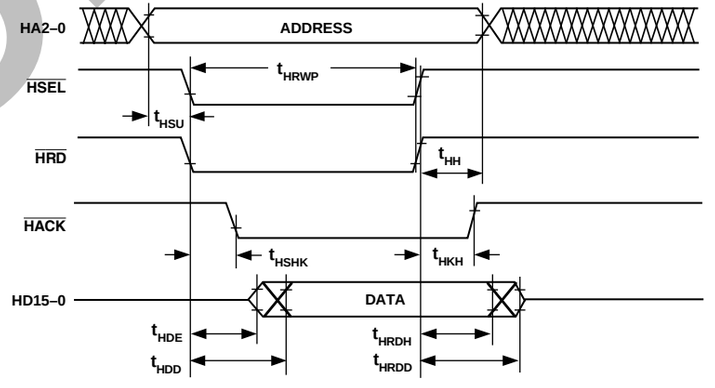


Figure 14. Host Interface Port (HMD1 = 0, HMD0 = 0)

OBSOLETE

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HSU}	HA2–0, HRW Setup before Start of Write or Read[1]	5		ns
t_{HDSU}	Data Setup before End of Write[2]	5		ns
t_{HWDH}	Data Hold after End of Write[2]	3		ns
t_{HH}	HA2–0, HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	15	ns
t_{HDE}	Data Enabled after Start of Read[1]	0		ns
t_{HDD}	Data Valid after Start of Read[1]		18	ns
t_{HRDH}	Data Hold after End of Read[2]	0		ns
t_{HRDD}	Data Disabled after End of Read[2]		7	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

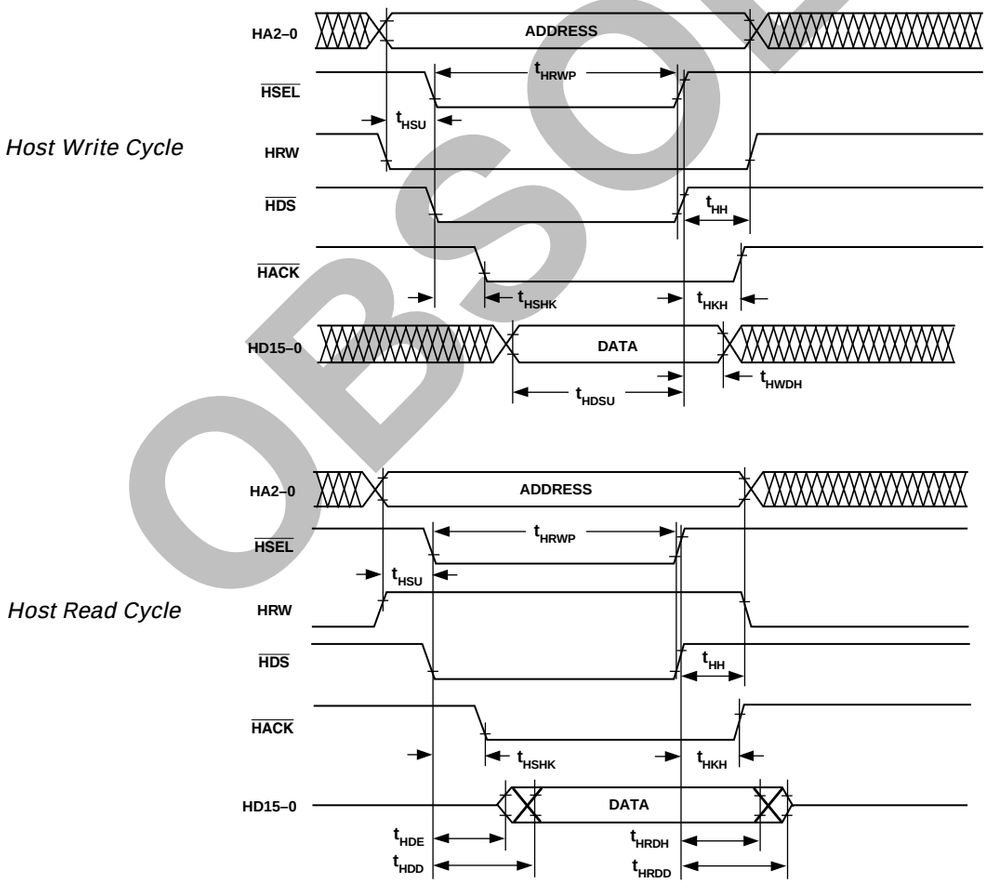


Figure 15. Host Interface Port (HMD1 = 0, HMD0 = 1)

OBSOLETE

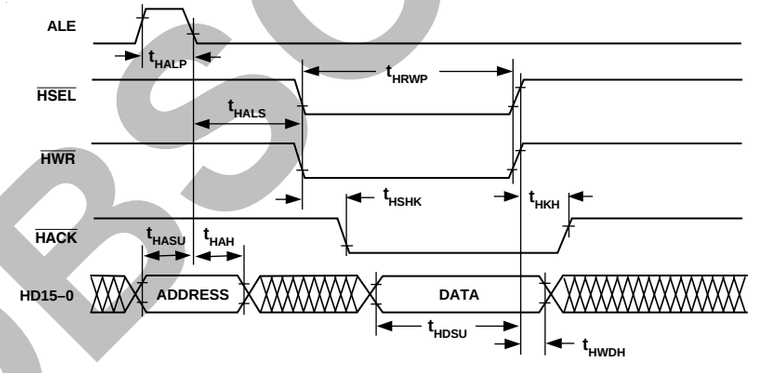
ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	10		ns
t_{HASU}	HAD15–0 Address Setup, before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1, 2]	10		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[3]	5		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[3]	3		ns
t_{HRWP}	Read or Write Pulse Width[4]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 5]	0	15	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[2]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[2]		18	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[5]		7	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[5]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.

OBSOLETE

Host Write Cycle



Host Read Cycle

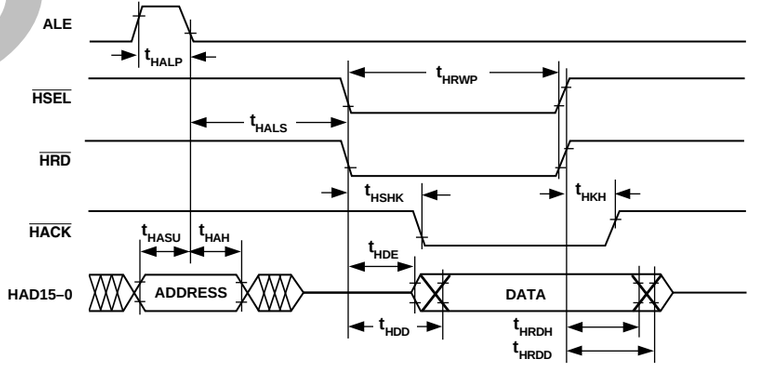


Figure 16. Host Interface Port (HMD1 = 1, HMD0 = 0)

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	10		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1]	10		ns
t_{HSU}	HRW Setup before Start of Write or Read[1]	5		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[2]	5		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[2]	3		ns
t_{HH}	HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	15	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[1]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[1]		18	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[2]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[2]		7	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

OBSOLETE

Host Write Cycle

Host Read Cycle

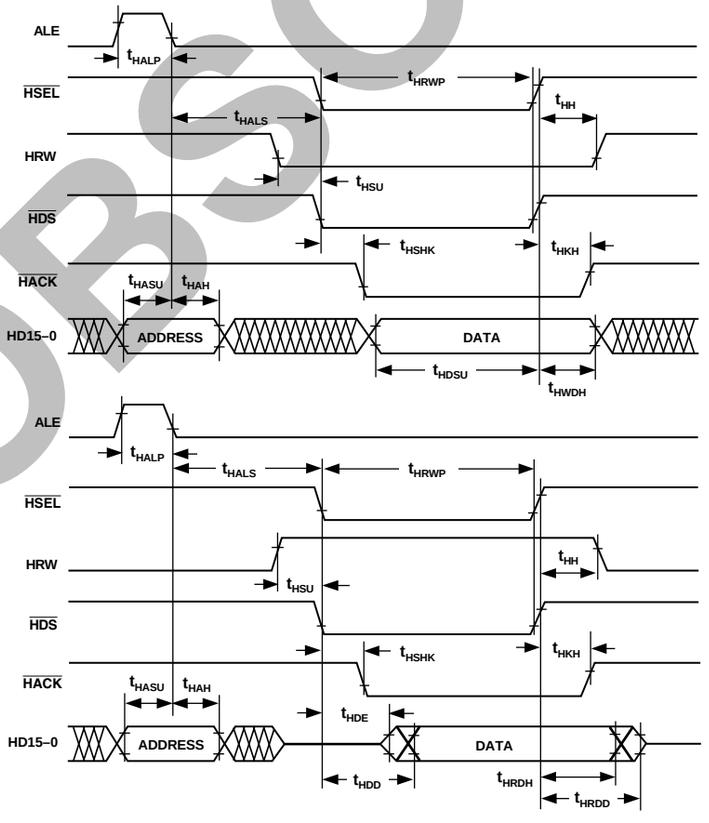


Figure 17. Host Interface Port (HMD1 = 1, HMD0 = 1)

ADSP-2171/ADSP-2172

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	50°C/W	2°C/W	48°C/W
PQFP	41°C/W	10°C/W	31°C/W

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 30 ns.

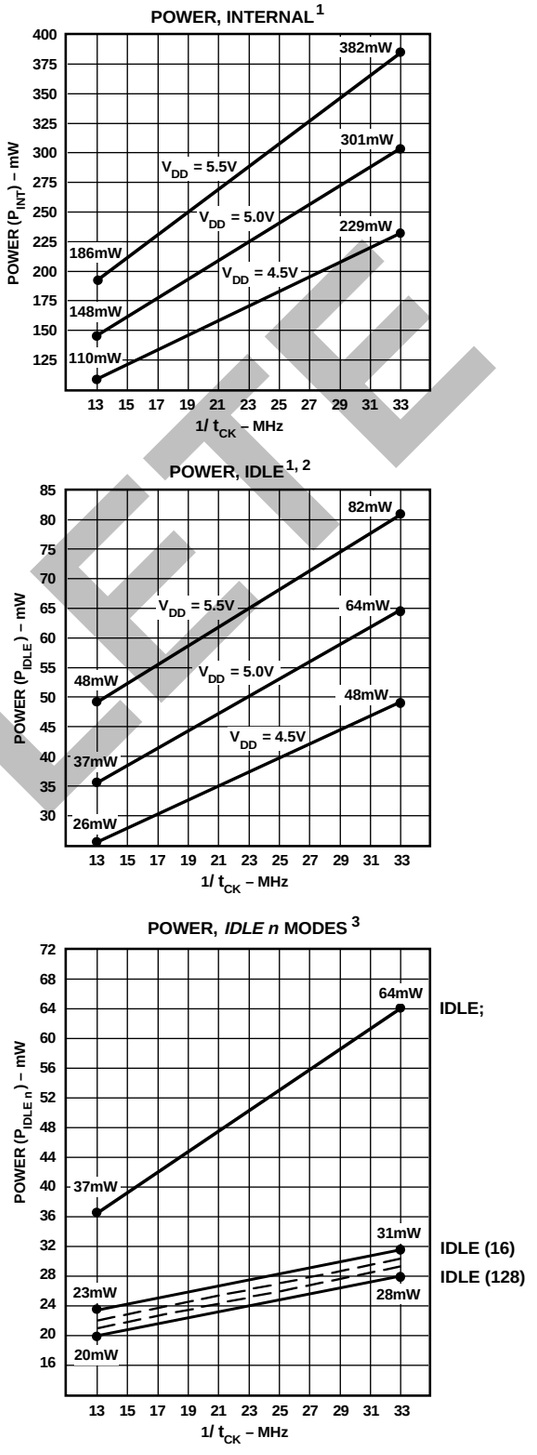
Total Power Dissipation = $P_{INT} + (C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 18).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

	# of Pins	× C	× V_{DD}^2	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 33.3 MHz	=	66.6 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 16.67 MHz	=	37.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 16.67 MHz	=	4.2 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 33.3 MHz	=	8.3 mW
						116.6 mW

Total power dissipation for this example is P_{INT} + 116.6 mW.



VALID FOR ALL TEMPERATURE GRADES.

[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.

[2] IDLE REFERS TO ADSP-2171 STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND. POWER REFLECTS DEVICE OPERATING WITH CLKOUT DISABLED.

[3] TYPICAL POWER DISSIPATION AT 5.0V V_{DD} DURING EXECUTION OF *IDLE N* INSTRUCTION (CLOCK FREQUENCY REDUCTION). POWER REFLECTS DEVICE OPERATING WITH CLKOUT DISABLED.

Figure 18. Power vs. Frequency

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ADSP-2171/ADSP-2172

CAPACITIVE LOADING

Figures 19 and 20 show the capacitive loading characteristics of the ADSP-2171/ADSP-2172.

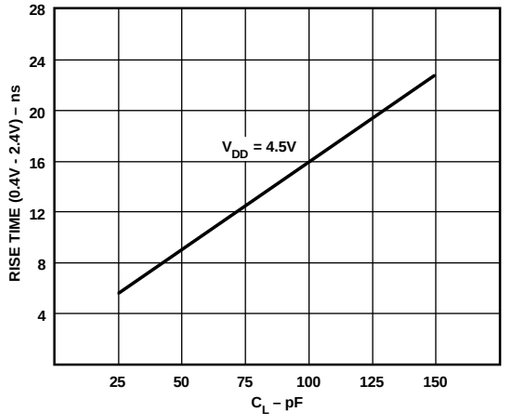

Figure 19. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

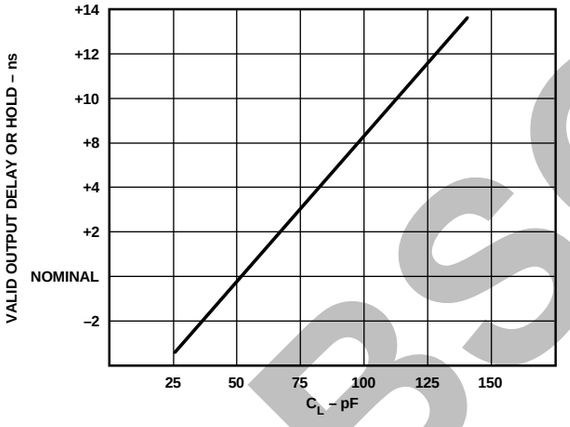

Figure 20. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

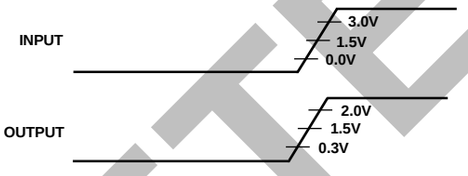

Figure 21. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when that have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

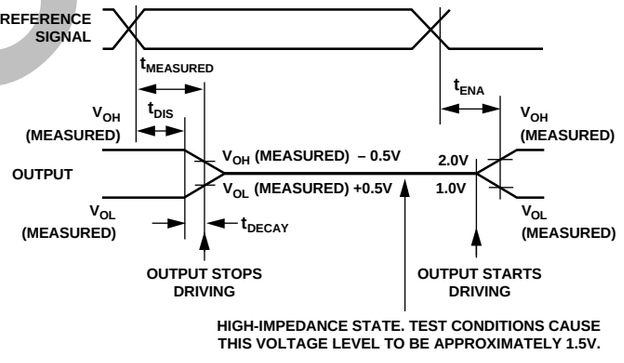

Figure 22. Output Enable/Disable

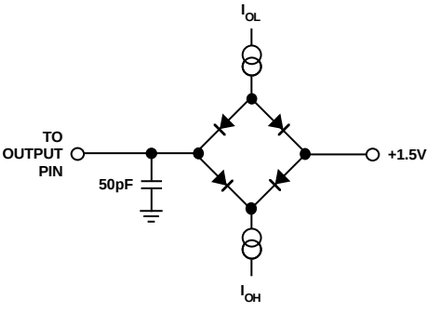

Figure 23. Equivalent Device Loading for AC Measurements (Including All Fixtures)

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ADSP-2173–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	3.0	3.6	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level RESET Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.4	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 mA[6]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = V_{DD} max[8]		10	µA
I_{OZL}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V[8]		10	µA
I_{DD}	Supply Current (Idle)[9, 10]	@ V_{DD} = max		7	mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DD} = max, t_{CK} = 50 ns[11]		27	mA
I_{DD}	Supply Current (Powerdown)[10]	Lowest Power Mode[12]		100	µA
C_I	Input Pin Capacitance[3, 6, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[6, 7, 13, 14]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

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NOTES

[1]Bidirectional pins: D0-D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, HD0-HD15/HAD0-HAD15.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}/\overline{\text{HDS}}$, $\overline{\text{PWD}}$, HA2/ALE, HA1-0.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}/\overline{\text{HDS}}$, $\overline{\text{PWD}}$, HA2/ALE, HA1-0.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0-A13, DT0, DT1, CLKOUT, $\overline{\text{HACK}}$, FL2-0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2173 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0-A13, D0-D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RSF1, HD0-HD15/HAD0-HAD15.

[8]0 V on $\overline{\text{BR}}$, CLKIN Active (to force three-state condition).

[9]Idle refers to ADSP-2173 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND. Current reflects device operation with CLKOUT disabled.

[10]Current reflects device operating with no output loads.

[11]V_{IN} = 0.4 V and 2.4 V. For typical figures for supply currents, refer to "Power Dissipation" section.

[12]See Chapter 9, of the *ADSP-2100 Family User's Manual* for details.

[13]Applies to TQFP and PQFP package types.

[14]Output pin capacitance is the capacitve load for any three-state output pin.

Specifications subject to change without notice.

ADSP-2173 TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also, use the switching characteristics to ensure any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2173 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ before $\overline{WR}$ Deasserted	Setup Address Setup to Write End
t_{WRA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

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ADSP-2173

Parameter		Min	Max	Unit
Clock Signals				
t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2173 uses an input clock with a frequency equal to half the instruction rate; a 10.0 MHz input clock (which is equivalent to 100 ns) yields a 50 ns processor cycle (equivalent to 20 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CKH} = 0.5t_{CK} – 10$ ns = 0.5 (50 ns) – 10 ns = 15 ns.				
Timing Requirement:				
t_{CKI}	CLKIN Period	100	160	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} – 10$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} – 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	25	ns
Control Signals				
Timing Requirement:				
t_{RSP}	RESET Width Low	$5t_{CK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

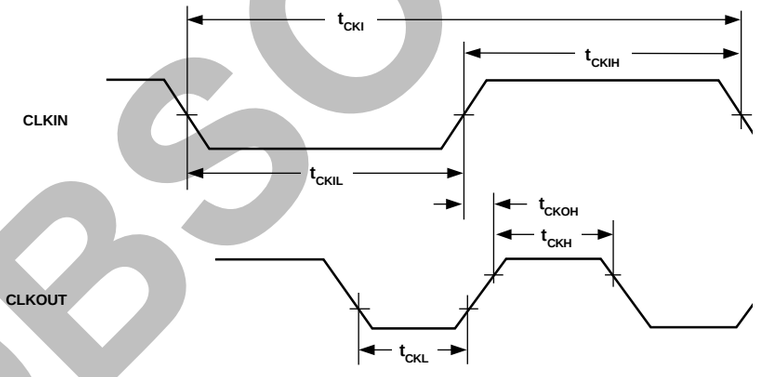

Figure 24. Clock Signals

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ADSP-2173

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	$\overline{IRQx}$ or FI Setup before CLKOUT Low[1, 2, 3]	$0.25t_{CK}$ + 23		ns
t_{IFH}	$\overline{IRQx}$ or FI Hold after CLKOUT High[1, 2, 3]	$0.25t_{CK}$		ns
Switching Characteristic:				
t_{FOH}	Flag Output Hold after CLKOUT Low[4]	$0.5t_{CK}$ – 10		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[4]		$0.5t_{CK}$ + 5	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[4]Flag Output = FL0, FL1, FL2, and FO.

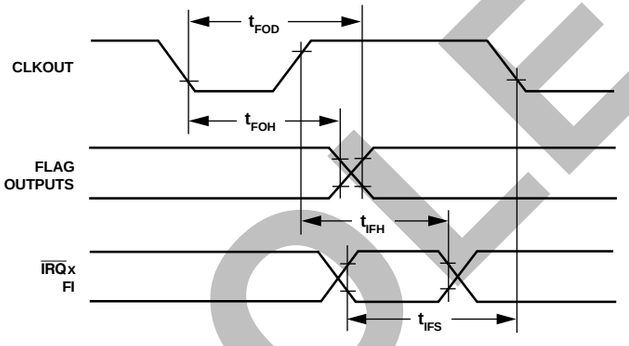

Figure 25. Interrupts and Flags

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ADSP-2173

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 2		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 22		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 16	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ – 10		ns
t_{SDBH}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

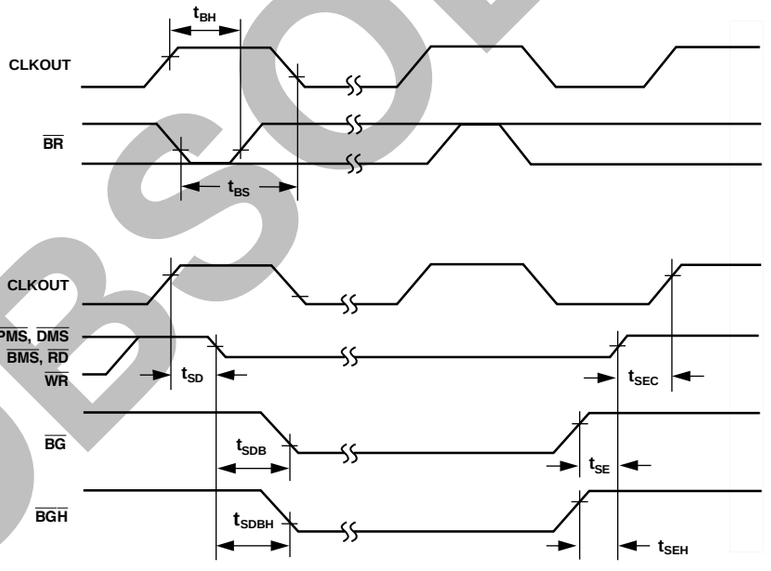

Figure 26. Bus Request–Bus Grant

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ADSP-2173

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 7$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}.

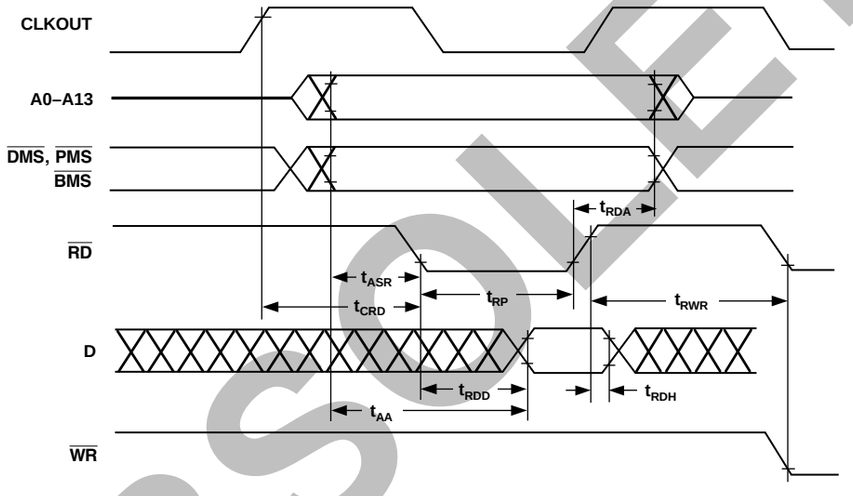

Figure 27. Memory Read

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ADSP-2173

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	0.5 t_{CK} – 7 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	0.25t_{CK} – 2		ns
t_{WP}	$\overline{WR}$ Pulse Width	0.5t_{CK} – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	0.25t_{CK} – 7		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	0.25t_{CK} – 7		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	0.25t_{CK} – 5	0.25 t_{CK} + 10	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	0.75t_{CK} – 11.5 + w		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	0.25t_{CK} – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5t_{CK} – 5		ns

w = wait states x t_{CK}.

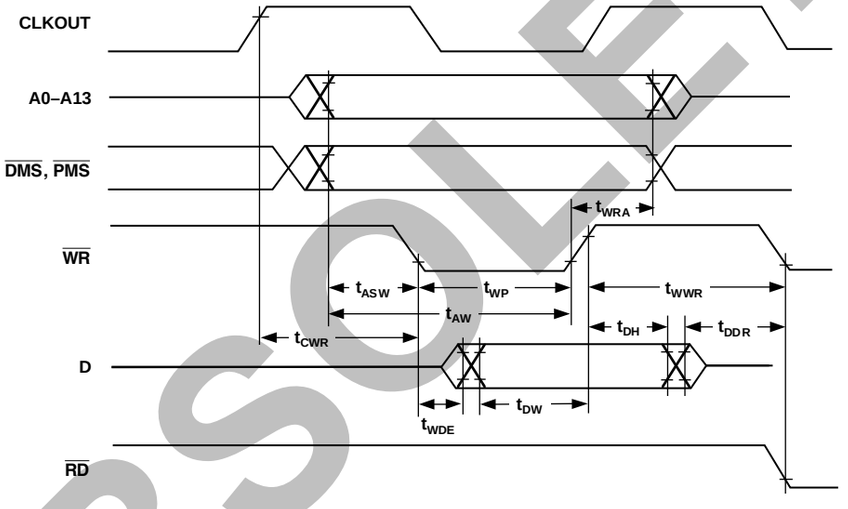

Figure 28. Memory Write

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ADSP-2173

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	76.9		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		ns
t_{SCP}	$SCLK_{IN}$ Width	28		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		20	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		20	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS(Alt) to DT Enable	0		ns
t_{TDV}	TFS(Alt) to DT Valid		19	ns
t_{SCDD}	SCLK High to DT Disable		25	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20	ns

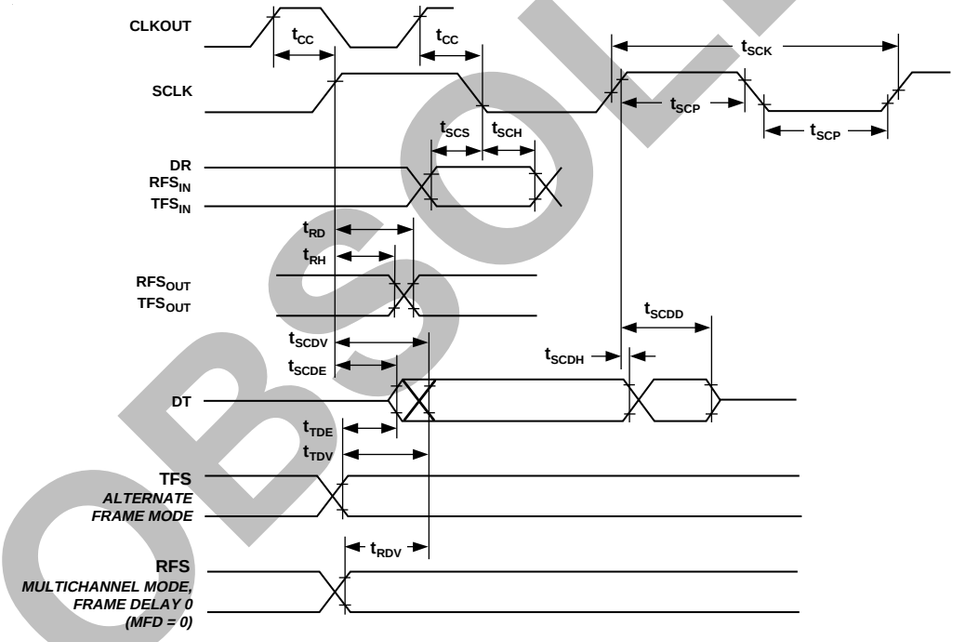

Figure 29. Serial Ports

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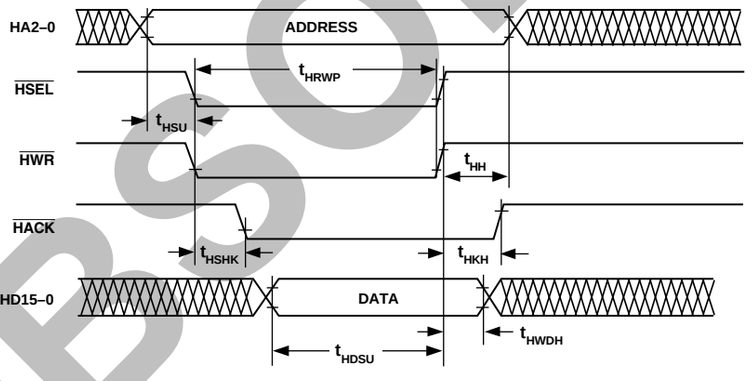
ADSP-2173

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HSU}	HA2–0 Setup before Start of Write or Read[1, 2]	8		ns
t_{HDSU}	Data Setup before End of Write[3]	8		ns
t_{HWDH}	Data Hold after End of Write[3]	3		ns
t_{HH}	HA2–0 Hold after End of Write or Read[3, 4]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	ns
t_{HDE}	Data Enabled after Start of Read[2]	0		ns
t_{HDD}	Data Valid after Start of Read[2]		23	ns
t_{HRDH}	Data Hold after End of Read[4]	0		ns
t_{HRDD}	Data Disabled after End of Read[4]		15	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

OBSOLETE

Host Write Cycle



Host Read Cycle

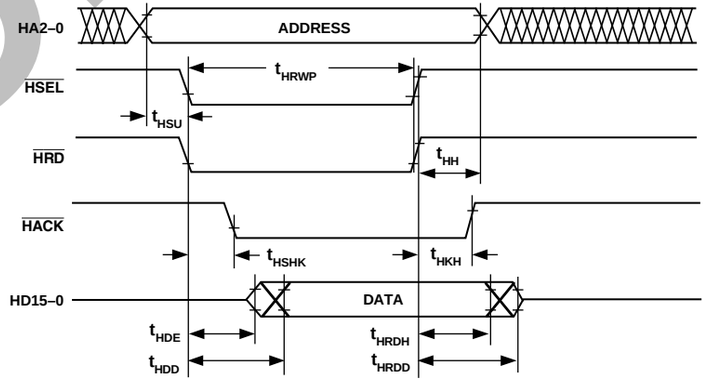


Figure 30. Host Interface Port (HMD1 = 0, HMD0 = 0)

ADSP-2173

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HSU}	HA2–0, HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	Data Setup before End of Write[2]	8		ns
t_{HWDH}	Data Hold after End of Write[2]	3		ns
t_{HH}	HA2–0, HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	Data Enabled after Start of Read[1]	0		ns
t_{HDD}	Data Valid after Start of Read[1]		23	ns
t_{HRDH}	Data Hold after End of Read[2]	0		ns
t_{HRDD}	Data Disabled after End of Read[2]		15	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

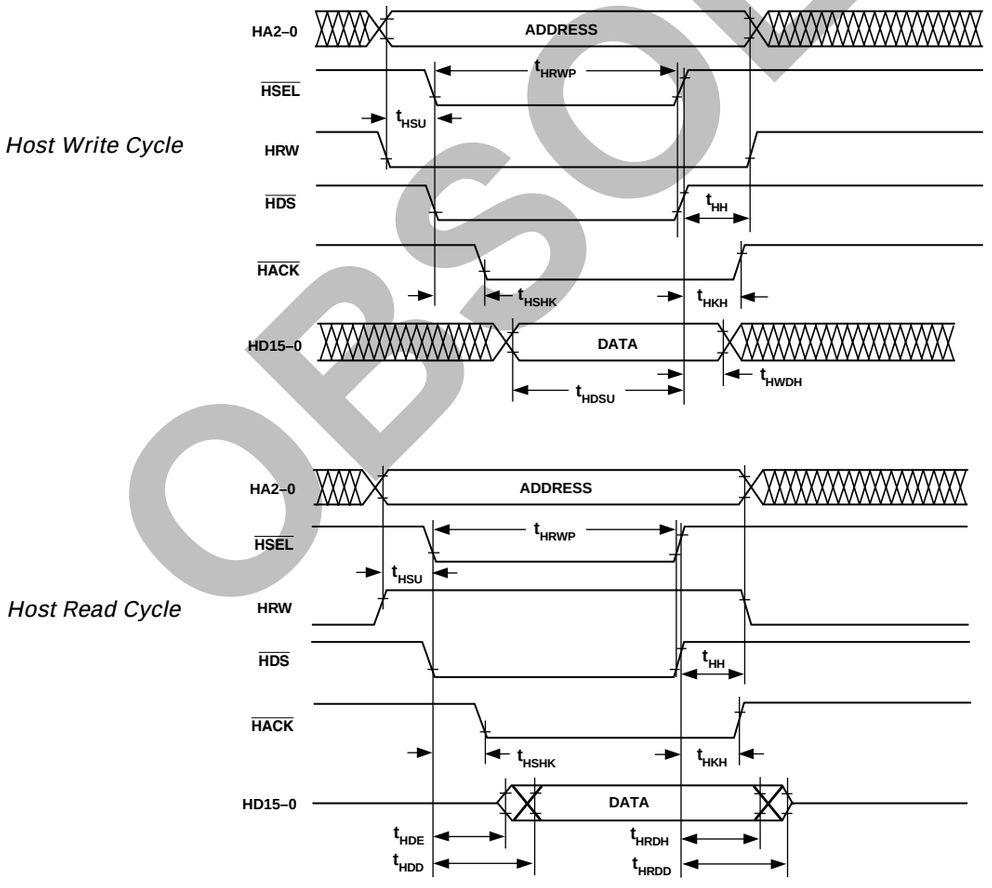


Figure 31. Host Interface Port (HMD1 = 0, HMD0 = 1)

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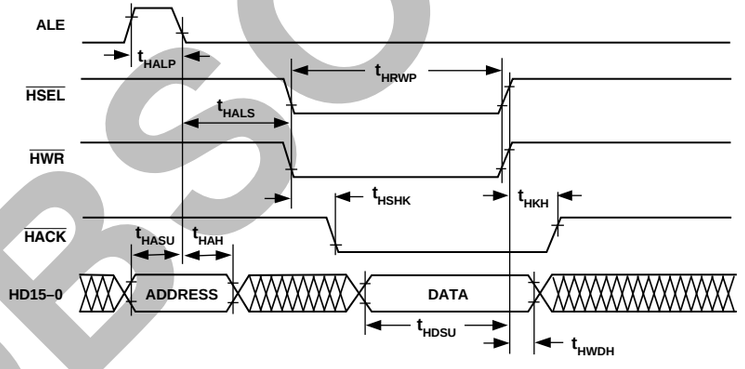
ADSP-2173

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup, before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1, 2]	15		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[3]	8		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[3]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[2]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[2]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[4]		15	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

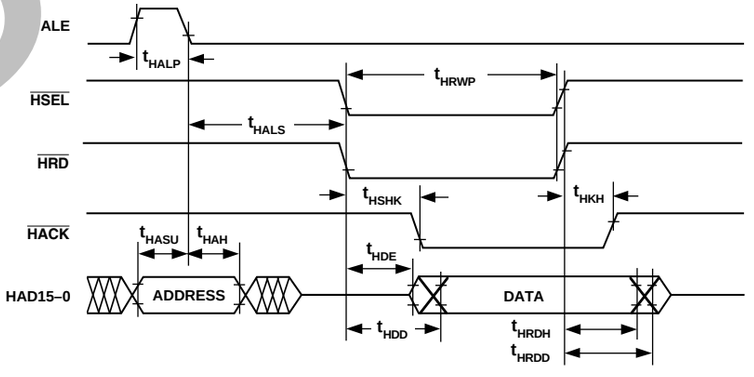


Figure 32. Host Interface Port (HMD1 = 1, HMD0 = 0)

OBSOLETE

ADSP-2173

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1]	15		ns
t_{HSU}	HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[2]	8		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[2]	3		ns
t_{HH}	HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[1]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[1]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[2]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[2]		15	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle

Host Read Cycle

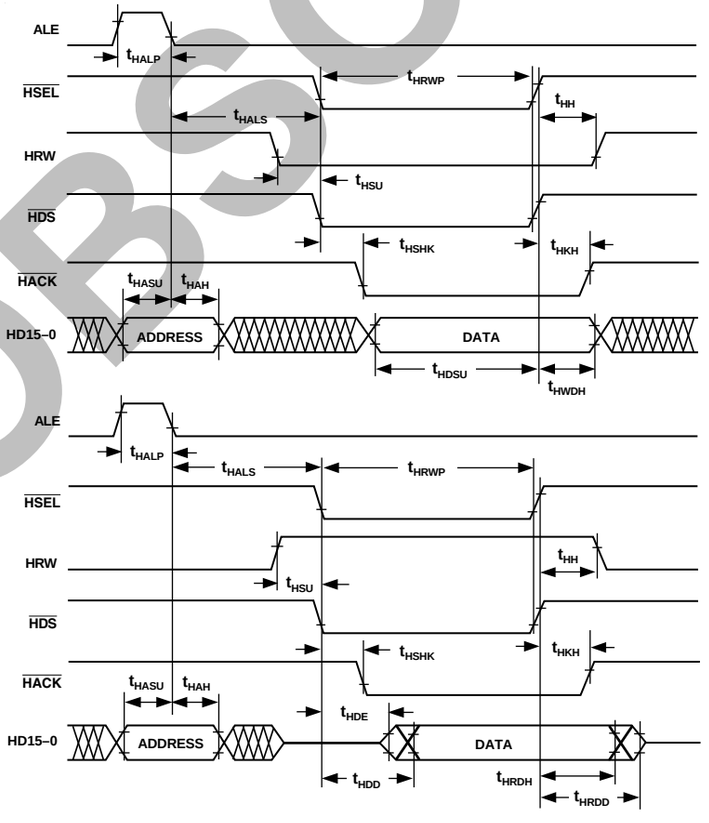


Figure 33. Host Interface Port (HMD1 = 1, HMD0 = 1)

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ADSP-2173

ENVIRONMENTAL CONDITIONS
Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	50°C/W	2°C/W	48°C/W
PQFP	41°C/W	10°C/W	31°C/W

POWER DISSIPATION
To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 50 ns.

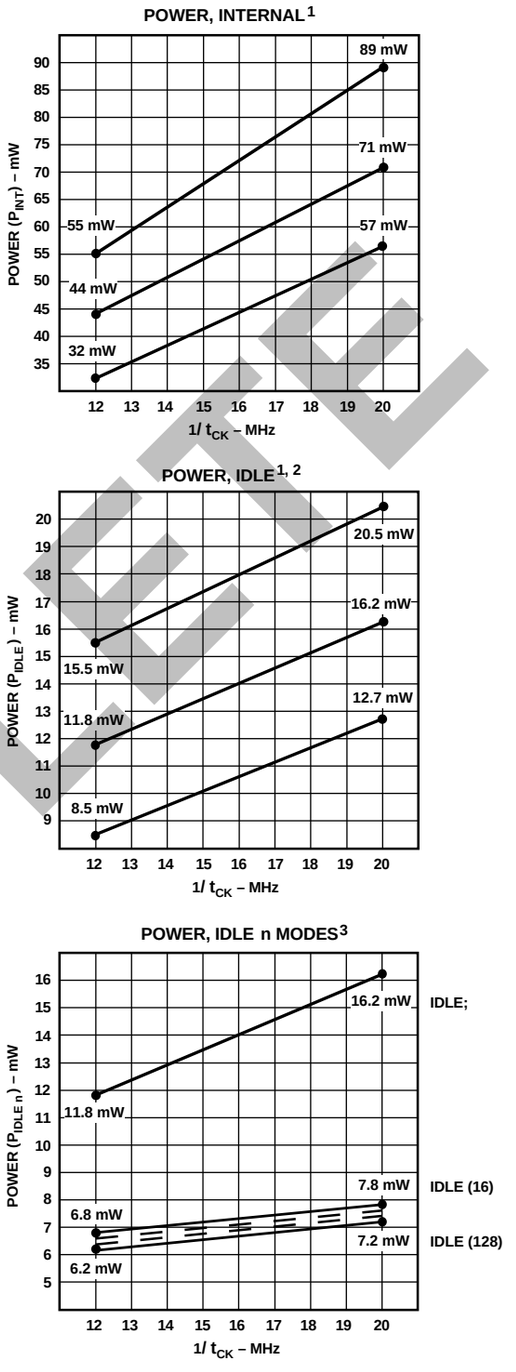
Total Power Dissipation = P_{INT} + ($C \times V_{DD}^2 \times f$)

P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 18).

($C \times V_{DD}^2 \times f$) is calculated for each output:

	# of Pins	× C	× V_{DD}^2	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 3.3^2 V	× 20 MHz	=	17.4 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 3.3^2 V	× 10 MHz	=	9.8 mW
$\overline{RD}$	1	× 10 pF	× 3.3^2 V	× 10 MHz	=	1.1 mW
CLKOUT	1	× 10 pF	× 3.3^2 V	× 20 MHz	=	2.2 mW
						30.5 mW

Total power dissipation for this example is P_{INT} + 30.5 mW.



VALID FOR ALL TEMPERATURE GRADES.

[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
[2] IDLE REFERS TO ADSP-2173 STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND. POWER REFLECTS DEVICE OPERATING WITH CLKOUT DISABLED.
[3] TYPICAL POWER DISSIPATION AT 3.3V V_{DD} DURING EXECUTION OF IDLE n INSTRUCTION (CLOCK FREQUENCY REDUCTION). POWER REFLECTS DEVICE OPERATING WITH CLKOUT DISABLED.

Figure 34. Power vs. Frequency

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ADSP-2173

CAPACITIVE LOADING

Figures 35 and 36 show the capacitive loading characteristics of the ADSP-2173.

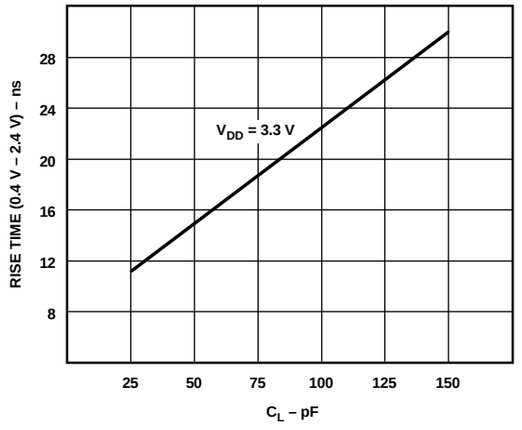

Figure 35. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

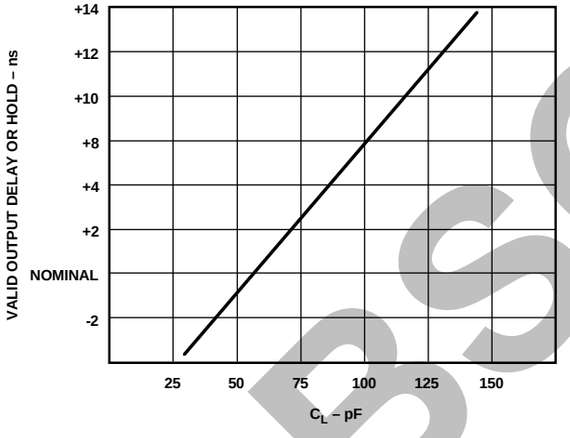

Figure 36. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

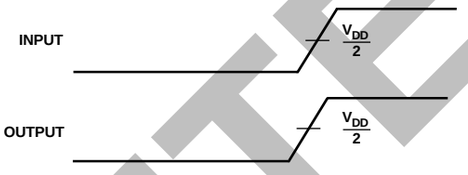

Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when that have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

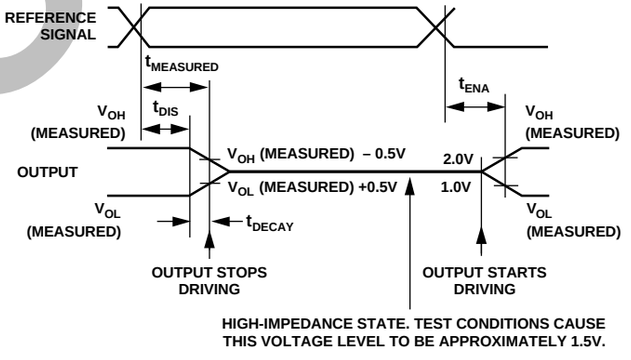

Figure 38. Output Enable/Disable

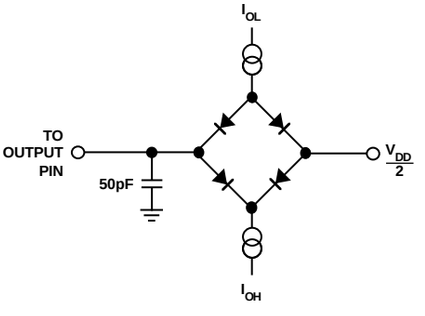

Figure 39. Equivalent Device Loading for AC Measurements (Including All Fixtures)

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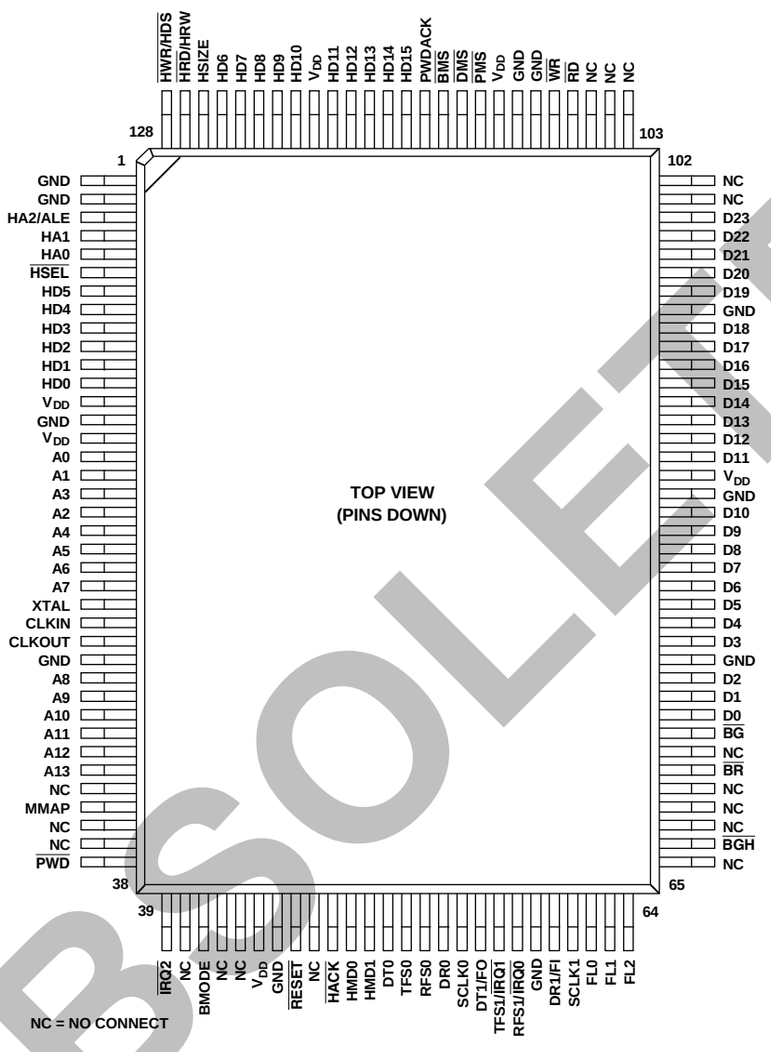
128-Lead TQFP Package Pinout



OBSOLETE

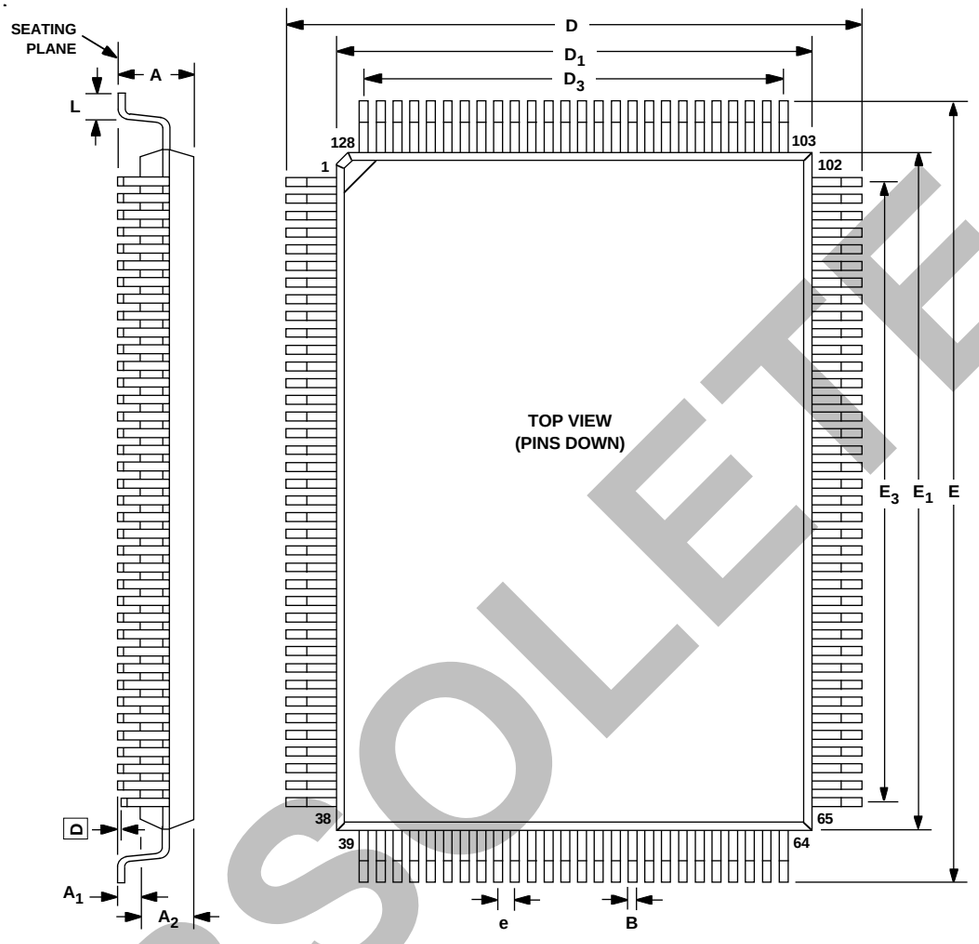
TQFP Pin Configurations

TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name
1	GND	33	A13	65	NC	97	D20
2	GND	34	NC	66	$\overline{BGH}$	98	D21
3	HA2/ALE	35	MMAP	67	NC	99	D22
4	HA1	36	NC	68	NC	100	D23
5	HA0	37	NC	69	NC	101	NC
6	$\overline{HSEL}$	38	$\overline{PWD}$	70	$\overline{BR}$	102	NC
7	HD5	39	$\overline{IRQ2}$	71	NC	103	NC
8	HD4	40	NC	72	$\overline{BG}$	104	NC
9	HD3	41	BMODE	73	D0	105	NC
10	HD2	42	NC	74	D1	106	$\overline{RD}$
11	HD1	43	NC	75	D2	107	$\overline{WR}$
12	HD0	44	V_{DD}	76	GND	108	GND
13	V_{DD}	45	GND	77	D3	109	GND
14	GND	46	$\overline{RESET}$	78	D4	110	V_{DD}
15	V_{DD}	47	NC	79	D5	111	$\overline{PMS}$
16	A0	48	$\overline{HACK}$	80	D6	112	$\overline{DMS}$
17	A1	49	HMD0	81	D7	113	$\overline{BMS}$
18	A2	50	HMD1	82	D8	114	PWDACK
19	A3	51	DT0	83	D9	115	HD15
20	A4	52	TFS0	84	D10	116	HD14
21	A5	53	RFS0	85	GND	117	HD13
22	A6	54	DR0	86	V_{DD}	118	HD12
23	A7	55	SCLK0	87	D11	119	HD11
24	XTAL	56	DT1/FO	88	D12	120	V_{DD}
25	CLKIN	57	TFS1/$\overline{IRQ1}$	89	D13	121	HD10
26	CLKOUT	58	RFS1/$\overline{IRQ0}$	90	D14	122	HD9
27	GND	59	GND	91	D15	123	HD8
28	A8	60	DR1/F1	92	D16	124	HD7
29	A9	61	SCLK1	93	D17	125	HD6
30	A10	62	FL0	94	D18	126	HSIZE
31	A11	63	FL1	95	GND	127	$\overline{HRD}$/HRW
32	A12	64	FL2	96	D19	128	$\overline{HWR}$/$\overline{HDS}$

NC = These pins MUST remain unconnected.

OBSOLETE

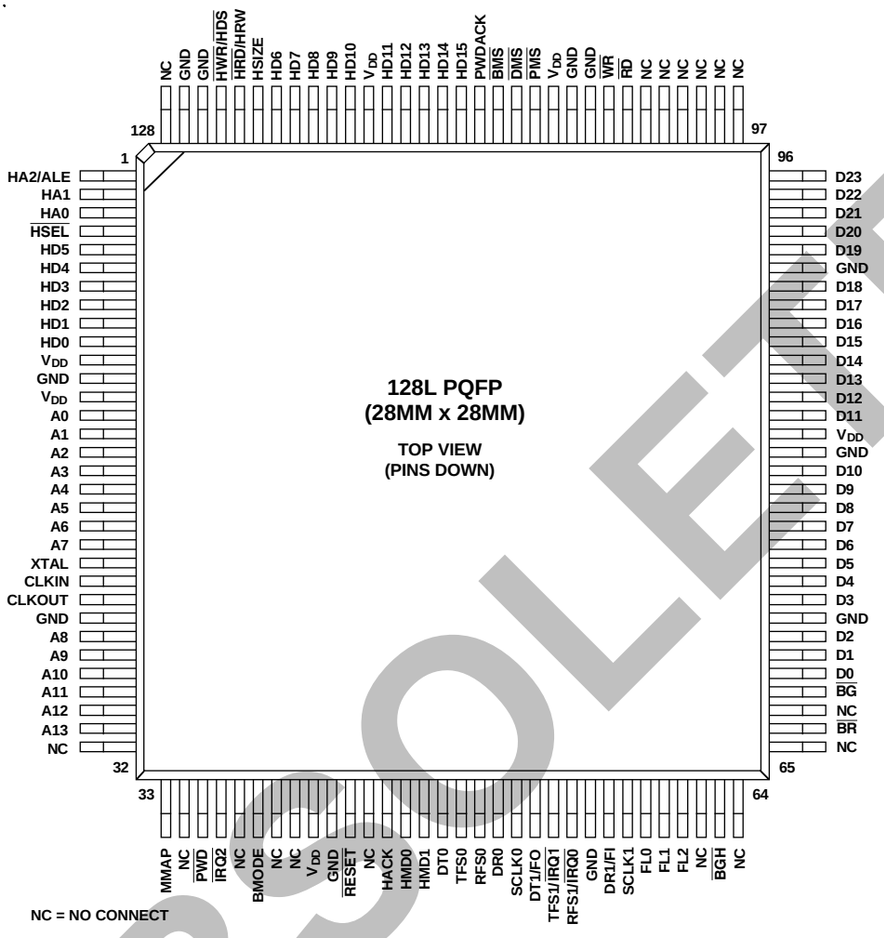
OUTLINE DIMENSIONS
128-Lead Metric Thin Plastic Quad Flatpack (TQFP)



	MILLIMETERS			INCHES		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A			1.60		0.063	
A_1	0.05		0.15	0.002		0.006
A_2	1.30	1.40	1.50	0.051	0.055	0.059
D	15.75	16.00	16.25	0.620	0.630	0.640
D_1	13.90	14.00	14.10	0.547	0.551	0.555
D_3		12.50	12.58		0.492	0.495
E	21.75	22.00	22.25	0.856	0.866	0.876
E_1	19.90	20.00	20.10	0.783	0.787	0.792
E_3		18.50	18.58		0.728	0.731
L	0.45	0.60	0.75	0.018	0.024	0.030
e	0.42	0.50	0.58	0.017	0.019	0.023
B	0.17	0.22	0.27	0.007	0.009	0.011
⊐			0.10			0.004

OBSOLETE

128-Lead PQFP Package Pinout



OBSOLETE

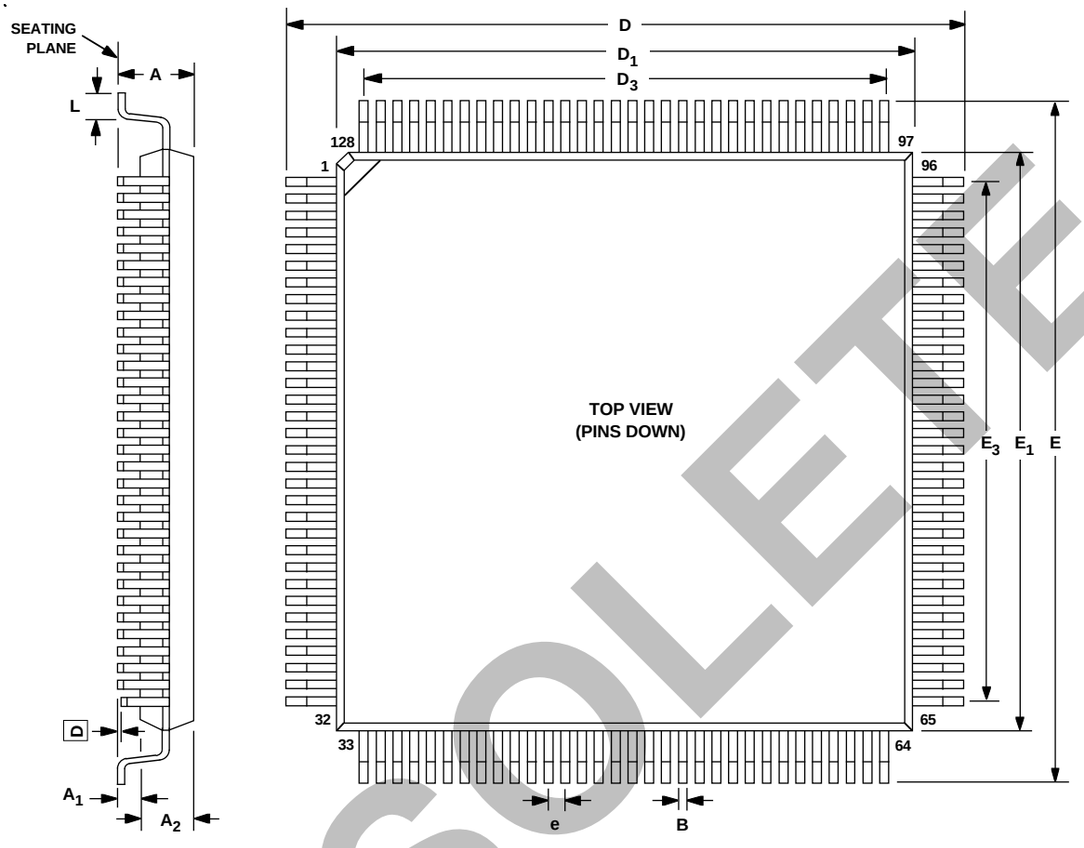
PQFP Pin Configurations

PQFP Number	Pin Name	PQFP Number	Pin Name	PQFP Number	Pin Name	PQFP Number	Pin Name
1	HA2/ALE	33	MMAP	65	NC	97	NC
2	HA1	34	NC	66	$\overline{BR}$	98	NC
3	HA0	35	$\overline{PWD}$	67	NC	99	NC
4	$\overline{HSEL}$	36	$\overline{IRQ2}$	68	$\overline{BG}$	100	NC
5	HD5	37	NC	69	D0	101	NC
6	HD4	38	BMODE	70	D1	102	NC
7	HD3	39	NC	71	D2	103	$\overline{RD}$
8	HD2	40	NC	72	GND	104	$\overline{WR}$
9	HD1	41	V_{DD}	73	D3	105	GND
10	HD0	42	GND	74	D4	106	GND
11	V_{DD}	43	$\overline{RESET}$	75	D5	107	V_{DD}
12	GND	44	NC	76	D6	108	$\overline{PMS}$
13	V_{DD}	45	$\overline{HACK}$	77	D7	109	$\overline{DMS}$
14	A0	46	HMD0	78	D8	110	$\overline{BMS}$
15	A1	47	HMD1	79	D9	111	PWDACK
16	A2	48	DT0	80	D10	112	HD15
17	A3	49	TFS0	81	GND	113	HD14
18	A4	50	RFS0	82	V_{DD}	114	HD13
19	A5	51	DR0	83	D11	115	HD12
20	A6	52	SCLK0	84	D12	116	HD11
21	A7	53	DT1/FO	85	D13	117	V_{DD}
22	XTAL	54	TFS1/$\overline{IRQ1}$	86	D14	118	HD10
23	CLKIN	55	RFS1/$\overline{IRQ0}$	87	D15	119	HD9
24	CLKOUT	56	GND	88	D16	120	HD8
25	GND	57	DR1/F1	89	D17	121	HD7
26	A8	58	SCLK1	90	D18	122	HD6
27	A9	59	FL0	91	GND	123	HSIZE
28	A10	60	FL1	92	D19	124	$\overline{HRD}$/HRW
29	A11	61	FL2	93	D20	125	$\overline{HWR}$/$\overline{HDS}$
30	A12	62	NC	94	D21	126	GND
31	A13	63	$\overline{BGH}$	95	D22	127	GND
32	NC	64	NC	96	D23	128	$\overline{NC}$

NC = These pins MUST remain unconnected.

OBSOLETE

OUTLINE DIMENSIONS
128-Lead Metric Thin Plastic Quad Flatpack (PQFP)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			4.07			0.160
A_1	0.25			0.010		
A_2	3.17	3.49	3.67	0.125	0.137	0.144
D, E	30.95	31.20	31.45	1.219	1.228	1.238
D_1, E_1	27.90	28.00	28.10	1.098	1.102	1.106
D_3, E_3	24.73	24.80	24.87	0.974	0.976	0.979
L	0.65	0.88	1.03	0.031	0.035	0.041
e	0.73	0.80	0.87	0.029	0.031	0.034
B	0.30	0.35	0.45	0.012	0.014	0.018
D			0.10			0.004

OBSOLETE

ORDERING GUIDE*

Part Number**	Ambient Temperature Range	Instruction Rate (MHz)	Package Description
ADSP-2171KST-133	0°C to +70°C	33.33	128-Lead TQFP
ADSP-2171BST-133	–40°C to +85°C	33.33	128-Lead TQFP
ADSP-2171KS-133	0°C to +70°C	33.33	128-Lead PQFP
ADSP-2171BS-133	–40°C to +85°C	33.33	128-Lead PQFP
ADSP-2171KST-104	0°C to +70°C	26	128-Lead TQFP
ADSP-2171BST-104	–40°C to +85°C	26	128-Lead TQFP
ADSP-2171KS-104	0°C to +70°C	26	128-Lead PQFP
ADSP-2171BS-104	–40°C to +85°C	26	128-Lead PQFP
ADSP-2173BST-80	–40°C to +85°C	20	128-Lead TQFP
ADSP-2173BS-80	–40°C to +85°C	20	128 Lead PQFP

*Refer to section titled “Ordering Procedure for ADSP-2172 ROM Processors” for information about ordering ROM-coded parts.
**S = Plastic Quad Flatpack, ST = Plastic Thin Quad Flatpack.

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