Using Third Overtone Crystals with the ADSP-218x DSP

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Introduction

DSPs frequently require an input clock frequency (CLKIN) that is over 35MHz. Unfortunately fundamental mode crystals over 35MHz are not popular and tend to be expensive and fragile. Packaged clock oscillators cost considerably more than a crystal so, for some applications, using a 3rd overtone (3rd OT) crystal may be a sensible choice.

While the current trend is to incorporate PLL frequency multiplication into the DSP, using a low frequency input clock to generate internal core clocks of several hundred MHz, there are still occasions when it might be useful to consider using a 3rd OT crystal.

This note discusses using readily available 3rd overtone crystals, at frequencies over 35MHz, with the ADSP-218x family of DSPs. A design procedure is developed for calculating the optimum values for the support components. This procedure can be extended to CODECs and other applications requiring input clocks over 35MHz.

Cautionary Note

There are a number of cautions that should be noted when deciding to use a 3rd OT crystal oscillator.

First, a 3rd OT crystal normally has a higher ESR, typically more than twice that of a fundamental mode crystal at the same frequency. Second, a 3rd OT crystal has a lower activity, (i.e. requires a higher minimum drive level to start reliably).

For these reasons, extra care should be taken when designing 3rd OT crystal oscillators and careful testing should be performed over temperature, voltage and with a representative batch of crystals to ensure that all parts operate reliably.

Note that there is often no indication, marked on the crystal package, to show that a crystal is intended for 3rd OT operation verses fundamental mode operation. Care should be taken to determine this information. If a crystal is used in a traditional (two capacitor fundamental mode circuit) appears to be oscillating at approximately one third of the frequency marked on it's package, it is very likely that it is intended for 3rd OT operation.

Design Method

When a 3rd OT crystal is chosen, two additional circuit components must be added to the traditional parallel, or fundamental mode circuit, to force oscillation at the overtone frequency marked on the crystal. The added components consist of a series inductor and capacitor as shown in Figure 1. If L_1 and C_3 are not added to the circuit, the crystal will oscillate at its fundamental frequency, which is approximately one third of the desired overtone frequency.

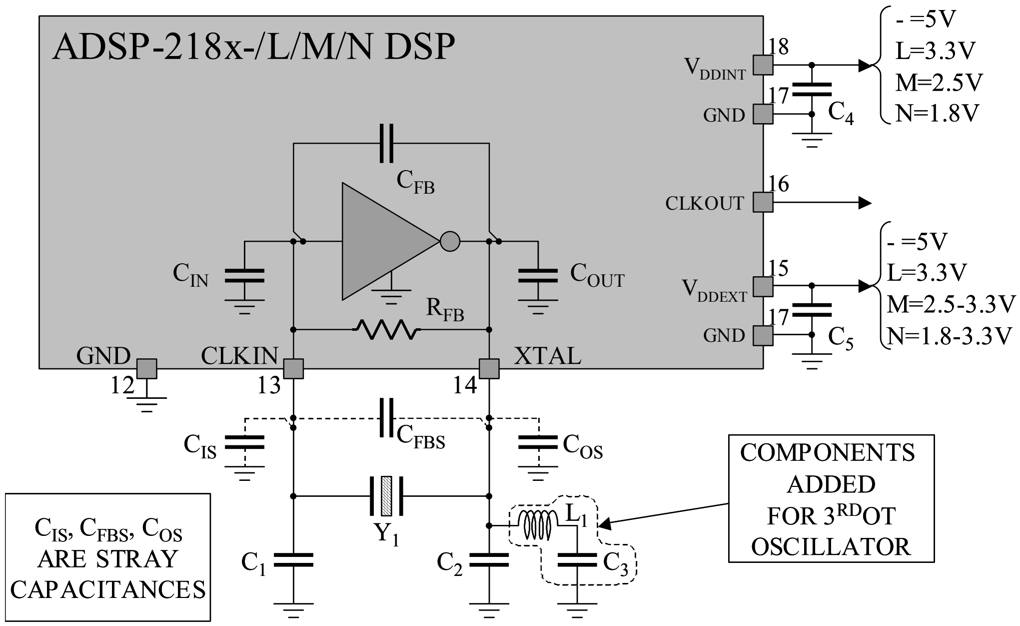

Figure 1: Schematic of 3rd Overtone Crystal Oscillator

Note that the three capacitors, C_1, C_2 and C_3, must be 'RF' types with low loss dielectrics at the frequencies being used. Examples of capacitors with suitable dielectrics include silver mica, polystyrene and ceramic NP0.

The inductor, L_1, must also be chosen for low RF losses (i.e. high 'Q'). At these frequencies and inductance values this usually means an air core type, although there are some inductors that use special formulations of iron dust and/or ferrites that result in high Q. As a guide, look for an inductor with a Q greater than 30, DC resistance less than 1.0Ω and a self-resonant frequency (SRF) greater than 120MHz.

The crystal's load capacitance (C_L) is required to ensure the crystal operates at the labeled frequency and will be specified by the crystal manufacturer. This is usually a 'standard' value and 18pF is very common. It is up to the engineer to choose the correct values for C_1, C_2, C_3 and L_1 in conjunction with the amplifier and stray PCB capacitance, to provide the correct load capacitance, C_L. C_1 and C_2 will usually be between 20pF and 70pF.

C_3 is only required for blocking DC current that would otherwise load the output of the oscillator. Its value is not critical and a value of 1nF NP0 should be satisfactory.

The inductor, L_1, is chosen to resonate with C_2 and the stray output capacitance at a frequency $f_R \approx ⅔$ of the 3^{rd} OT frequency, f_{OT}. This provides the correct loading reactance for the crystal and closed loop phase relationship to start and maintain oscillation. In addition, the parallel combination of L_1 and C_2 must provide an effective capacitance, C_{2EFF} at the 3^{rd}OT frequency, f_{OT}, to correctly load the crystal.

We have the following two equations with two unknown values, L_1 and C_2 …

$$f_R = \frac{2f_{OT}}{3} = \frac{1}{2\pi\sqrt{(C_2 + C_{OUT} + C_{OS})L_1}} \qquad \textit{Equation 1}$$

$$@f_{OT},\quad \frac{X_{C_2} \times X_{L_1}}{X_{C_2} + X_{L_1}} = X_{C_{2EFF}} = \frac{1}{2\pi f_{OT} C_{2EFF}} \qquad \textit{Equation 2}$$

where f_R is the actual resonant frequency of L_1 combined with the total output capacitance, C_2, C_{OUT} and C_{OS}. Note that C_2 is the actual capacitor value used while C_{2EFF} is the effective capacitance at f_{OT} due to the parallel combination of C_2 and L_1.

The reactance of C_3 is small enough to be ignored. Similarly the contributions of the feedback capacitances, C_{FB} and C_{FBS}, are very small and can be ignored in determining the required values of C_2 and L_1.

With some simple arithmetic manipulation we have the resulting design equations for C_2 and L_1 …

$$\boxed{C_2 = \frac{9C_{2EFF} + 4(C_{OUT} + C_{OS})}{5}}$$

Equation 3

$$\boxed{L_1 = \frac{5}{4\omega_{OT}^2(C_{2EFF} + C_{OUT} + C_{OS})}}$$

Equation 4

where: $\omega_{OT} = 2\pi f_{OT}$

Summarizing, the crystal manufacturer will specify a total load capacitance for the crystal. This is the TOTAL value of capacitance that must appear across the two terminals of the crystal for the operating frequency to be within the specified tolerance of the value stamped on the package. The total capacitance is usually called the load capacitance, C_L, and will consist of the amplifier input capacitance, C_{IN}, feedback capacitance, C_{FB} and output capacitance, C_{OUT}.

Added to these is the PCB stray capacitances, C_{IS}, C_{FBS} and C_{OS}. Finally we have to add the external capacitors C_1 and the parallel combination of C_2 and L_1.

Example: Determining External Load Capacitors, C_1, C_2 and Inductor L_1

Assume a manufacturer specifies a 37.5MHz 3rd OT crystal with a load capacitance, C_L=18pF. For the ADSP-218xM/N oscillator amplifier, typical values are C_{IN} = 5pF, C_{OUT} = 7pF and C_{FB} = 1pF. For the PCB stray capacitances, assume C_{IS}=2pF, C_{OS}=3pF and C_{FBS}=1pF. These are all reasonable approximations and, in practice, a couple of pF either way will not make much difference.

To calculate the equivalent capacitance <u>across the crystal</u>, first note that the input and output capacitances are effectively in series.

Therefore, the amplifier total capacitance, C_{AT}:

$$C_{AT} = C_{FB} + C_{IN}C_{OUT}/(C_{IN} + C_{OUT})$$
$$= [1 + 5\times 7/(5 + 7)]$$
$$\approx \underline{4\text{pF}}$$

For the PCB total capacitance, C_{PCBT}:

$$C_{PCBT} = C_{FBS} + C_{IS}C_{OS}/(C_{IS} + C_{OS})$$
$$= [1 + 2\times 3/(2 + 3)]$$
$$\approx \underline{2\text{pF}}$$

Therefore, total Amplifier and PCB stray capacitance, C_{ST}:

$$C_{ST} = C_{AT} + C_{PCBT}$$
$$\approx \underline{6\text{pF}}$$

The total load capacitance is specified by the crystal manufacturer. In this case, C_L = 18pF. We have 6pF provided by the amplifier in the DSP and stray PCB capacitance, as noted above. Hence we have to add another 12pF in parallel to make a total of 18pF. This capacitance is provided by C_1 and the combination of C_2 in parallel with L_1.

NOTE: It is most common to make C_1 and C_2 equal, and, since they are in series across the crystal, the resulting values for C_1 and C_{2EFF} will each be 24pF, the series combination making the 12pf required to make-up the specified total load capacitance.

NOTE that this 'sleight of hand' introduction of capacitance C_{2EFF} in place of C_2 which is the effective capacitance of the parallel combination of C_2 and L_1 required to make 24pF at the 3rd OT frequency.

At this point we have determined the value of C_1 - in this example,

$$\underline{C_1 = 24pF}$$

From the design equations, 3 & 4, we can determine the values of C_2 & L_1,

$$\boxed{C_2 = \frac{9C_{2EFF} + 4(C_{OUT} + C_{OS})}{5}}$$

$$C_2 = [9*24 + 4(7+3)]/5 = 51.2pF$$

$$\underline{\therefore C_2 = 51.2pF}$$

Also, knowing the required crystal overtone frequency, $\omega_{OT} = 2\pi f_{OT} = 2\pi \times 37.5MHz$;

$$\boxed{L_1 = \frac{5}{4\omega_{OT}^2(C_{2EFF} + C_{OUT} + C_{OS})}}$$

$$L_1 = 5/[4(2\pi 37.5\times 10E6)^2(24+7+5)10E\text{-}12]$$

$$= 662.2\times 10^{-9}H$$

$$\therefore \underline{L_1 = 662.2nH}$$

Checking Calculated Values

To check the effective capacitance of the $C_2//L_1$ combination at f_{OT}, we can use the expression;

$$C_{2EFF} = \frac{\frac{1}{j\omega C_2} + j\omega L_1}{j\omega\left(\frac{1}{j\omega C_2} \times j\omega L_1\right)}$$

which simplifies to;

$$\boxed{C_{2EFF} = C_2 - \frac{1}{\omega^2 \times L_1}}$$

Substituting values;

$$C_{2EFF} = 51.2pF - 1/(2\pi 37.5E6)^2 \times 662.2E\text{-}9$$

$$\underline{\therefore C_{2EFF} = 24pF} \checkmark$$

Also, to confirm the frequency of resonance, from equation 1;

$$f_r = 1/[2\pi\sqrt{\{(51.2pF + 7pF + 5pF)662.2nH\}}]$$

$$\underline{\therefore f_r = 25.0MHz = 2f_{OT}/3} \checkmark$$

So all the calculations look good. Using preferred values, we can complete our design as shown in Figure 2. (See Appendix A for a detailed component list)

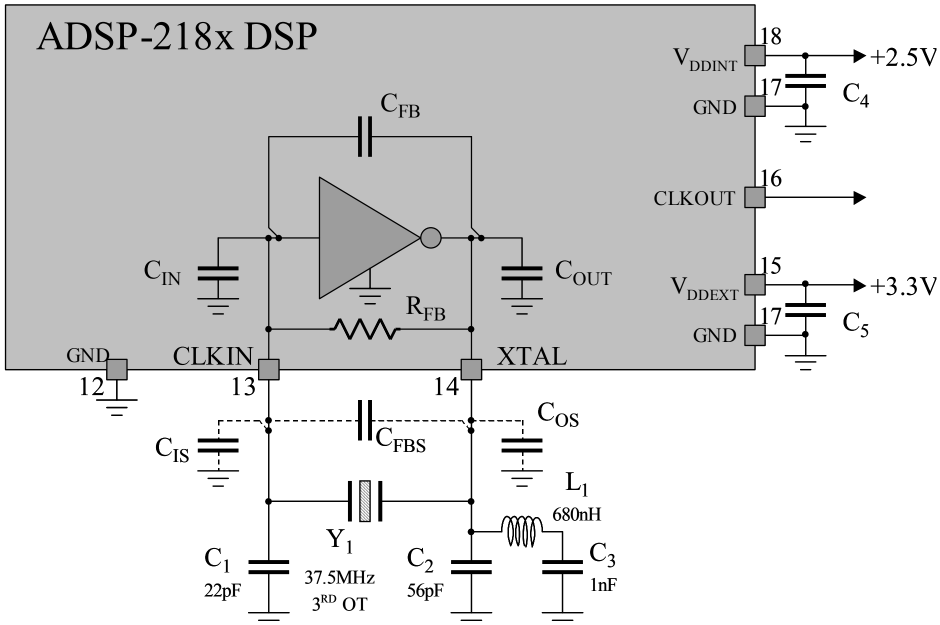

Figure 2: 37.5MHz, 3rd Overtone Crystal Oscillator

Test Results

A total of 15, 37.5MHz 3rd OT crystals were tested from three different batches. A second test of three different batches of five, 40MHz 3rd OT crystals were tested using the same circuit component values as for the 37.5MHz crystals. Finally, a third test of three 34MHz 3rd OT crystals were tested. All tests were performed on an ADSP-2189M EZ-KIT LITE evaluation board. The results are tabulated in Appendix B.

Note especially that all crystals are oscillating within the ±50ppm (±1875Hz for 37.5MHz) frequency tolerance specified by the crystal manufacturer. The worst-case deviation is within 25ppm. The manufacturer's test sheet shows the <u>average</u> operating frequency is above 37.5MHz by +29.8Hz. Checking the average for our application shows the frequency to be high by 292Hz. This error would normally be considered insignificant and could be ignored. The difference between the manufacturer's measured average frequency and our application is 262Hz.

If it is desired to trim (reduce) the operating frequency, we could increase the load capacitance using the "Pullability Equation" to estimate the additional load capacitance required.

This equation is given by …

$$\Delta f = f \times \frac{\Delta C_L C_1}{2(C_0 + C_L)^2} \quad Hz$$

where

C_L = Crystal Load Capacitance

C_0, C_1 = Crystal Capacitance Parameters

Using the average crystal parameters from Appendix C, the average pullability of the 37.5MHz crystals is ≈30Hz/pF. Hence by increasing the load capacitance C_L by 262Hz/30Hz/pF = 8.75pF, the mean frequency should be close to the manufacturer's quoted measurements. No attempt was made to verify this measurement as the operating frequency was already well within the manufacturer's specifications for all parts.

A check of voltage at the input to the crystal network shows the drive voltage to be approximately 2.5Vpp or just under 1Vrms. Lacking the instruments to measure crystal current, a Spice simulation was run, using the typical crystal parameters at the operating frequency. This showed a current through R_1 (approximating the crystal ESR) of approximately 1.2mA.

From the relation I^2R_1, where the crystal resistance is taken to be 65Ω, the crystal drive power is estimated to be greater than 93µW, which is considered sufficient to ensure oscillation.

Startup times for several 37.5 and 40MHz crystals were checked and ranged from a minimum of ≈12ms up to a maximum of ≈35ms.

Design Omissions

At this point it is useful to consider what has been ignored. The most important design considerations, ignored up till now, are the loop gain and the crystal drive level. The design process should aim for an overall loop gain (at zero degrees) of at least +10dB. While an amplifier gain of +30dB may seem sufficient, the crystal feedback network (including the source resistance of the amplifier) may have an attenuation of more than +20dB, thus reducing the gain margin. The loop gain is determined, in part, by the internal amplifier and is not something we have control over. We can minimize losses in the external feedback network by using high-Q RF capacitors and inductors and keeping all lead lengths and PCB traces very short. Using crystals with the lowest possible equivalent series resistance (ESR) is also a good idea.

The crystal drive level is usually measured in microwatts (µW) and third overtone crystals require a higher minimum drive level than fundamental mode crystals at the same frequency. This is a parameter that is difficult to measure and outside the scope of this paper. While the manufacturer specifies the maximum crystal drive level, typically 500µW to 1mW, the minimum drive level is usually not mentioned. This is unfortunate as it is one of the reasons why some 3rd OT crystal oscillators fail intermittently. Below a certain minimum drive level, a crystal may not start, or will start and then stop intermittently. The problem has been exacerbated with the trend to lower operating voltages for the amplifier. At V_{DDEXT} = 3.3V, the available ac signal is about half the amplitude obtained with a 5V supply. This reduces the crystal drive to level to 25% of a 5V system.

The crystal drive level should be measured and confirmed, if the facility is available. If possible, crystals should be selected with an ESR less than 50Ω. Extensive testing for startup reliability should be done to ensure operation for the limits of temperature, voltage and production tolerances.

Application Notes

At RF frequencies, care must be taken to absolutely minimize trace and lead lengths. Also, a ground plane is strongly recommended to ensure stability and reduce EMI. All DSP power pins should be bypassed to the ground plane with 10nF and/or 100nF surface mount capacitors, right at the pins.

Other oscillators on the same PCB should be physically separated and carefully decoupled to prevent mutual interaction via common power supply impedances. Failure to do this can also increase clock jitter.

The ground connections for capacitors $C_{1..5}$ should be connected to the ground plane with the shortest possible traces. The amplifier's ground pin(s) should be connected directly to the ground plane via without a trace.

The actual frequency of oscillation should be within the manufacturer's specified tolerance of the frequency marked on the crystal package. This is usually quoted by the manufacturer, in ppm. Typical tolerances are ±50 or ±100ppm. At 37.5MHz a tolerance of ±50ppm is ±1875Hz. If an accurate frequency counter is available, this should be confirmed, however, allowance should be made for the extra load impedance of the counter probe, unless the DSP has a buffered measurement point (e.g. CLKOUT).

If the operating frequency were outside this tolerance band it would indicate that the total load capacitance is in error or there is some other serious problem. Some crystal manufacturers will quote a figure called the 'pullability' of the crystal, usually in ppm/pF or Hz/pF. A typical figure is about 30Hz/pF (see Appendix C, parameter 'P'). This shows that an error of a few pF has only a small effect on the operating frequency.

It was mentioned earlier that the two external load capacitors, C_1 and C_{2EFF}, are normally equal values. It is possible to change the ratio of these two capacitors while maintaining the same total load capacitance. This is sometimes done to increase or decrease the feedback ratio and change the behavior of the oscillator. The objective might be to increase start-up speed with a low gain amplifier or improve stability if the amplifier gain is too high. These are not common requirements and are beyond the scope of this paper.

5th and Higher Overtone Crystals

The same principles described in this note apply to using 5th overtone and higher-order crystals. The parallel circuit consisting of C_2, L_1 and the stray output capacitance should be chosen to resonate halfway between the chosen overtone frequency and the next lowest overtone. For a 5th OT crystal, this would require $f_R \approx ⅘$ of the 5th OT frequency, f_{OT}.

It is still necessary to provide the manufacturer's specified load capacitance across the crystal and provide the correct network phase and gain conditions to initiate and support oscillation only at the chosen overtone. Note that the circuit becomes more critical of component tolerances as the overtone order increases, and 5th order operation, and higher, is not recommended for production applications. For clock frequencies up to 75MHz, it should not be necessary to use 5th OT mode crystals.

Appendix A

Components for the Example 37.5MHz 3rd Overtone Test Circuit

Ref Designator	Description	Package	Manufacturer	Part Number
C1	22pF, ±5%, 50V, NP0	SMD 0603	Panasonic	ECJ-1VC1H220J
C2	56pF, ±5%, 50V, NP0	SMD 0603	Panasonic	ECJ-1VC1H560J
C3	1nF, ±5%, 50V, NP0	SMD 0603	Panasonic	ECJ-1VC1H102J
L1	680nH, ±10%, Q_{min}=40, DCR<0.26Ω, SRF_{min}=175MHz	SMD 1008	API Delevan	1008-681K
Y1	37.5MHz, 3rdOT Crystal		Cardinal	CSM1-A1B2C2-100-37.5D18-3

Appendix B: 3rd OT Crystal Test Results

ADSP-2189M EZ-KIT. 3rd OT Crystal Oscillator Frequency Measurements

Tests on a selection of 3rd OT Crystals

Frequency Counter: HP Model 5328A

Approx 2min allowed for oscillator frequency to stabilize (typically drifts up about 200Hz)

FL = 37.50000 MHz Tolerance 50 ppm 1875 Hz

CL = 18 pF

		FL		Measured Frequency		
	Xtal	ppm	Hz	CLKOUT(kHz)	Xtal(kHz)	Error-Hz
CLP	1	-5.1	-191.3	75000.62	37500.31	310.0
(ThruHole)	2	4.8	180.0	75001.24	37500.62	620.0
	3	-3.54	-132.8	75000.67	37500.34	335.0
	4	4.23	158.6	75001.14	37500.57	570.0
	5	-3.19	-119.6	75001.08	37500.54	540.0
CSM1	6	11.31	424.1	75001.08	37500.54	540.0
(SMD)	7	9.46	354.8	75000.47	37500.24	235.0
	8	3.03	113.6	75000.32	37500.16	160.0
	9	4.23	158.6	75000.35	37500.18	175.0
	10	9.5	356.3	75001.02	37500.51	510.0
CX5	1	-6.91	-259.1	75000.03	37500.02	15.0
(SMD)	2	-3.72	-139.5	75000.19	37500.10	95.0
	3	-4.19	-157.1	75000.18	37500.09	90.0
	4	-4.33	-162.4	75000.15	37500.08	75.0
	5	-3.66	-137.3	75000.22	37500.11	110.0
Avg		0.79	29.8	75000.58	37500.29	292.0

FL = 40.00000 MHz Tolerance 50 ppm 2000 Hz

CL = 18 pF

NOTE: Same 3rd OT LC circuit values as used for 37.5MHz circuit.

This crystal frequency over clocks the 2189M DSP and is not recommended

		FL		Measured Frequency (Hz)		
	Xtal	ppm	Hz	CLKOUT (kHz)	Xtal(kHz)	Error-Hz
CLP	11	6.72	268.8	80000.91	40000.46	455.0
(ThruHole)	12	10.72	428.8	80000.69	40000.35	345.0
	13	7.35	294.0	80001.40	40000.70	700.0
	14	-0.67	-26.8	80000.73	40000.37	365.0
	15	5.39	215.6	80000.34	40000.17	170.0
CSM1	16	0.72	28.8	80000.98	40000.49	490.0
(SMD)	17	9.68	387.2	80000.36	40000.18	180.0
	18	2.05	82.0	80000.44	40000.22	220.0
	19	-0.17	-6.8	80000.34	40000.17	170.0
	20	1.72	68.8	80000.47	40000.24	235.0
CX5	1	-4.12	-16.5	80000.12	40000.06	60.0
(SMD)	2	-5.06	-20.2	79999.98	39999.99	-10.0
	3	-4.12	-16.5	80000.07	40000.04	35.0
	4	-7.36	-29.4	79999.80	39999.90	-100.0
	5	-9.41	-37.6	79999.22	39999.61	-390.0
Avg		0.896	108.0	80000.39	40000.20	195.0

FL = 34.0000 MHz Tolerance 50 ppm 1700 Hz

CL = 20 pF

NOTE: Same 3rd OT LC circuit values as used for 37.5MHz circuit.

		FL		Measured Frequency (Hz)		
	Xtal	ppm	Hz	CLKOUT	Xtal (/2)	Error-Hz
CLP	21	6.72	228.5	68000.21	34000.11	105.0
(ThruHole)	22	10.72	364.5	67999.68	33999.84	-160.0
	23	7.35	249.9	68002.05	34001.03	1025.0
		-0.67	-22.8			
		5.39	183.3			

Appendix C: Manufacturer's Sample Crystal Parameters

Ref Freq 37.50000 MHz (3rd OT)

CL = 18 pF

		FL		**Ts**	**Rs**	**Fs**		**C0**	**C1**	**L1**	**P**
	Xtal	ppm	Hz	ppm/pF	Ohm	ppm	Hz	pF	fF	mH	Hz/pF
CLP	1	9.50	356.3	0.7	83.9	-5.10	-191.3	1.883	0.583	30.9	27.7
(ThruHole)	2	4.23	158.6	0.7	77.5	-10.13	-379.9	1.847	0.572	31.5	27.2
	3	3.03	113.6	0.7	81.3	-11.44	-429.0	1.871	0.581	31.0	27.6
	4	11.31	424.1	0.9	84.5	-5.70	-213.8	1.862	0.676	26.6	32.1
	5	9.46	354.8	0.9	75.6	-8.99	-337.1	1.880	0.738	24.4	35.0
CSM1	1	4.23	158.6	0.9	72.8	-13.57	-508.9	1.902	0.714	25.2	33.8
(SMD)	2	-5.10	-191.3	0.8	64.2	-24.25	-909.4	2.037	0.653	27.6	30.5
	3	4.80	180.0	0.8	85.0	-10.91	-409.1	1.897	0.624	28.9	29.6
	4	-3.19	-119.6	0.9	60.8	-20.64	-774.0	2.027	0.698	25.8	32.6
	5	-3.54	-132.8	0.9	57.4	-21.64	-811.5	2.271	0.733	24.6	33.4
CX5	1	-6.91	-259.1	0.7	49.9	-20.91	-784.1	1.652	0.553	32.6	26.8
(SMD)	2	-4.19	-157.1	0.8	42.8	-19.05	-714.4	1.574	0.587	30.7	28.7
	3	-3.72	-139.5	0.7	50.9	-18.24	-684.0	1.644	0.574	31.4	27.9
	4	-4.33	-162.4	0.8	46.7	-19.06	-714.8	1.676	0.584	30.8	28.3
	5	-3.66	-137.3	0.8	47.1	-18.55	-695.6	1.427	0.584	30.8	29.0
AVG		0.79	29.8	0.80	65.36	-15.21	-570.5	1.830	0.630	28.9	30.0

Ref Freq 40.00000 MHz (3rd OT)

CL = 18 pF

		FL		**Ts**	**Rs**	**Fs**		**C0**	**C1**	**L1**	**P**
	Xtal	ppm	Hz	ppm/pF	Ohm	ppm		pF	fF	mH	Hz/pF
CLP	1	6.72	268.8	0.9	40.8	-10.74	-429.6	2.060	0.710	22.3	35.3
(ThruHole)	2	10.72	428.8	1.0	33.6	-8.72	-348.8	2.051	0.788	20.1	39.2
	3	7.35	294.0	0.8	42.4	-9.21	-368.4	2.080	0.668	23.7	33.1
	4	-0.67	-26.8	0.9	36.6	-18.40	-736.0	2.042	0.718	22.0	35.7
	5	5.39	215.6	1.0	33.0	-13.62	-544.8	1.739	0.761	20.8	39.1
CSM1	1	0.72	28.8	0.8	37.9	-16.45	-658.0	2.851	0.725	21.8	33.4
(SMD)	2	9.68	387.2	0.8	47.4	-6.79	-271.6	2.817	0.691	22.9	31.9
	3	2.05	82.0	0.8	42.5	-14.71	-588.4	2.826	0.699	22.6	32.2
	4	-0.17	-6.8	0.9	34.0	-18.38	-735.2	2.824	0.764	20.7	35.2
	5	1.72	68.8	0.8	37.3	-15.20	-608.0	2.827	0.712	22.2	32.8
CX5	1	-4.12	-164.8	0.8	58.0	-20.09	-803.6	1.562	0.627	25.2	32.8
(SMD)	2	-5.06	-202.4	0.8	61.2	-20.82	-832.8	1.694	0.623	25.4	32.1
	3	-4.12	-164.8	0.8	57.7	-19.82	-792.8	1.679	0.620	25.5	32.0
	4	-7.36	-294.4	0.8	54.8	-23.63	-945.2	1.478	0.636	24.9	33.5
	5	-9.41	-376.4	0.8	58.3	-25.45	-1018.0	1.466	0.625	25.3	33.0
AVG		0.90	35.8	0.85	45.03	-16.14	-645.4	2.133	0.691	23.0	34.1

Ref Freq 34.00000 MHz (3rd OT)

CL = 20 pF

		FL		**Ts**	**Rs**	**Fs**		**C0**	**C1**	**Q**	**P**
	Xtal	ppm	Hz	ppm/pF	Ohm	ppm	Hz	pF	fF	k	Hz/pF
CLP	1	-12.40	-421.6		26.2			2.900	1.200	149	38.9
(ThruHole)	2	-13.30	-452.2		26.7			3.000	1.180	148	37.9
HC49/LP	3	-20.80	-707.2		26.6			3.000	1.170	151	37.6
	4	13.60	462.4		31.0			3.000	1.140	133	36.6
	5	11.20	380.8		28.6			3.000	1.250	130	40.2
AVG		-4.34	-147.56		27.82			2.980	1.188	142	38.2

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