Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
Phone: (800) ANALOG-D or (781) 461-3881, FAX: (781) 461-3010, EMAIL: dsp.support@analog.com

ADSP-21xx Serial Port Startup Issues

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Overview

This Engineering Note will describe issues that can arise when starting up an ADSP-21xx Serial Port.

QUESTION:

Engineer #1:

I'm using the 2181 for video processing. I am having some trouble reading in a clocked serial stream on SPORT0. I set up the SPORT to alternate unframed mode, which means it expects a frame signal only at the first bit of a continuous transmission. But, it looks like the first two bits of my data are always getting swallowed; after that it's fine. If I change to normal unframed mode, the first *three* bits get swallowed; so at least the unframed mode is correct. Anyone with experience on this stuff?

Engineer #2:

Yup, read the manual very thoroughly. Also I do invert the frame sync. Setup times are very generous, on the order of several uS. I have heard from one other 2181 user that the first two bits get swallowed in frameless mode. By generating two initial bits on the data stream, everything works out fine. Looks like an undocumented "feature" of the 2181 SPORTs

ANSWER:

Actually, what you are experiencing is a side effect of the startup timing described in section 5.13.2.1 of the 2100 Family User's Manual...

"When a serial port is enabled by a write to the System Control Register, it takes two SCLK cycles before it is actually enabled. On the next (third) SCLK cycle, the serial port becomes active, looking for a frame sync."

The SPORT was designed this way to synchronize the enable signal to the asynchronous serial clock. What happens in your case is that there are no SCLK cycles without the frame signal being asserted. To the clocked serial port, it appears that any cycle could be the start of your frameless data stream; there is a valid frame signal every cycle. This causes the SPORT to skip the data on the first two or three cycles of SCLK if you are not giving any cycles without the frame signal, since it ignores the frame signal until the SPORT becomes active. This situation can happen to anyone using frameless modes with the clock only operating when data is being sent.

The solution of sending a couple dummy bits will work fine if the SPORT is enabled long before the SCLK starts, but could cause trouble if the enable bit is written at about the same time as the first SCLK cycle. An alternate solution would be to have the frame signal de-asserted for 2 or more SCLK cycles, and than asserted when the data starts. Some other processors have a special asynchronous start mode to better support the "toggle the clock only when there is data" type of operation.

The bottom line is that Frameless operation actually means Frame the first word only rather than have no frame signal at all.