ANALOG DEVICES

ADSP-2186M Anomaly List for Revision 2.0

The list below represents the known anomalies and workarounds for the ADSP-2186M. This silicon revision of a particular device can be found on the chip, as shown below:

ADSP-2186M	Part Number
-xxx	Speed Grade/Package
xyzzzzzzz-**2.0**	Lot Number and **Silicon Revision**
Dwwyy	Date Code

The Table below shows which ADSP-2186M's have each anomaly. The left hand side of the table lists the type of anomaly and the numbers on the top of the table refer to the particular revision of the silicon. Any box that has an 'x' contained in it has that anomaly. For a complete description of the anomaly, please refer to the susbsequent page.

	2.0
1. Speed path with decoding a groupIV register write instruction	X
2. When the PDForce bit in SPORT1 Autobuffer Control Register (0x3FEF)is set, it remains HIGH after powerdown	X
3. Latchup Spec. This device can only sink a maximunm of 70mA.	X

Anomaly #1

When writing certain values to a group IV register, the instruction is slow being decoded. This results is that device will execute a push on the PC Stack. This limits the operating voltage, for 75MHz operation to 2.55V-2.65V across the commercial temperature range(0C – 70C).

Anomaly #2

Coming out of powerdown the PDForce bit does not get cleared. This will **not** force another powerdown, and can be ignored. If another powerdown needs to be forced, you must set the PDForce bit again.

This anomaly is only applied to systems entering powerdown by writing the power-down force bit. When exiting power down the PDForce bit does not get cleared. This will **not** force another power down, and can be ignored or manually cleared. You will not encounter any problems if you never read and write back the SPORT1 Autobuffer Control Register. If you are writing back to the SPORT1 Autobuffer Control Register, make sure that that the power-down force bit is always manually written to zero.