Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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Interrupts and Programmable Flags on the ADSP-2185/2186

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Overview

The programmable flag pins on the ADSP-2185/2186 DSPs retain the same functionality as the ADSP-2181 but share these pins with interrupt pins. This engineer's note will describe the different modes of operation for these pins.

Modes of Operation

The ADSP-2185/2186 programmable flag pins PF[7:4] are shared with interrupts, /IRQ2, /IRQL1, /IRQL0, and /IRQE respectively. Both the programmable flags and the interrupts are directly connected to the shared pins. This works because you can use existing control register to chose the desired function for each pin. There are 4 possible states for each pin:

- **IMASK[x]=0, PFTYPE[x]=0 (PF Input)**
  - **Read of PFDATA gives pin value**
  - **No interrupt occurs**
  - **Default after reset**

- **IMASK[x]=1, PFTYPE[x]=0 (PF Input)**
  - **Read of PFDATA gives pin value**
  - **Interrupt occurs on level or edge transition**

- **IMASK[x]=0, PFTYPE[x]=1 (PF Output)**
  - **Write to PFDATA sets pin value**
  - **Read of PFDATA gives set value**
  - **No interrupt occurs**

- **IMASK[x]=1, PFTYPE[x]=1 (PF Output)**
  - **Write to PFDATA sets pin value and may cause interrupt (level or edge sensitive)**
  - **Read of PFDATA gives set value**

After reset, the PF pins will default to inputs and the interrupts will be disabled by the IMASK register's default value. The pins can be used as PF outputs by changing the PFTYPE register and leaving the interrupt disabled in IMASK. If the pins are to be used as interrupts then the PFTYPE register need not be changed, but the interrupt must be enabled in the IMASK register. Even if interrupts are enabled, reading the PFDATA register still sampled the pin's value.

Setting the PFTYPE register for a PF configured as an output and enabling the corresponding interrupt in IMASK, gives writes to PFDATA the ability to cause an interrupt. Interrupts will occur on the proper transitions high to low for edge sensitive and low level for level sensitive.

This could provide you with more flexibility in programming the DSP since you now have the ability to execute a software interrupt.

In summary, interrupts which share pins with the programmable flags behave as interrupts enabled by the IMASK register whether the pin is driven as an input to the chip of drives off chip as an output.