Technical Notes on using Analog Devices' DSP components and development tools
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Mode D and ADSP-218x Pin Compatibility - the FAQs:

Note: *This FAQ is written specifically to explain the functionality of the Mode D pin on the ADSP-218x Family, and not to describe how to use IACK in your design. For general information on the functionality of IACK and IDMA, please refer to the appropriate processor Data Sheet or Section 11.3 of the ADSP-2100 Family Users Manual.*

Q: What is Mode D? Which DSPs contain Mode D? What does it do and why is it useful?

A: Mode D is a multiplexed pin used to set the orientation of IDMA Acknowledge (IACK) after chip reset (caused by either the assertion of RESET or ERESET). Mode D is contained on the ADSP-2187L (Revisions 1.0 and greater), and all revisions of the ADSP-2185M, ADSP-2186M, ADSP-2187M, ADSP-2188M, and ADSP-2189M processors. It is multiplexed with the PF3 pin on these DSPs.

The status of Mode D on reset dictates whether IACK will be an active driven signal or if it will have an open source. **Mode D does *not* change whether IACK is an active low or active high signal!** It is *always* an active low signal.

If Mode D=0, IACK will be configured such that it has an active internal pull-down. This is the same mode that IACK is configured on all ADSP-218x parts that do not contain Mode D. The advantage of configuring IACK in this mode is that it does not require any additional external circuitry to operate properly. However, the disadvantage is that it is not possible to "wire-OR" multiple IACKs together. Therefore, this is the recommended state of IACK if your system only has one DSP and is using the IDMA port.

If Mode D=1, IACK is configured such that it has an open source. This mode requires an external pull-down resistor, but it now is possible to "wire-IACKs to a single host. Therefore, this mode is most useful in designs that include multiple DSPs communicating through the IDMA Port.

Q: How do I determine the value for the pull-down resistor?

A: The value of the pull-down resistor is determined by the processor leakage current (found in the *Electrical Characteristics* section of the Data Sheet) and the number of processors present in a system. As an example, if a system has 2 ADSP-2187Ls, there will be two IACKs using the same pull-down resistor. The resistor must be strong enough to pull down the IACK lines below 0.8v to ensure proper operation. The maximum leakage current from any one ADSP-2187L is 10µA; therefore, the maximum leakage current flowing through the pull-down resistor is 20µA. The minimum resistor value is calculated to be:

$$V = I * R$$
$$0.8v = 20E\text{-}6A * R$$

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$R = 40000\Omega$

This value becomes smaller as the number of processors in your system increases.

Q: How can I design my current system which does not have Mode D such that it will work with a DSP that uses Mode D?

A: If you are currently designing a system that uses a DSP without Mode D functionality and you want to ensure plug-in compatilibility for a DSP which contains Mode D, the board must be designed such that it drives a specific input into PF3 on chip reset, through either of the methods mentioned above. Specifically, if you wish to continue using IACK as an actively driven signal with a DSP that contains Mode D, you should ensure that PF3="0" on the rising edge of RESET and ERESET. However, if in a future design you will be configuring IACK to be an open sourced pin, PF3 should be driven to a logic high on reset.