Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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ADSP-2181 Priority Chain & IDMA Holdoffs

QUESTION:

What is the prioritization of a core write, BDMA write, SPORT write and IDMA write? Does the worst case of 3.5 cycles on an IDMA Long Read Cycle account for concurrent BDMA and SPORT write requests to the same internal memory location? If so, is this a case where /IACK is a must use signal?

ANSWER:

The ADSP-2181 Priority Chain for concurrent requests occurring at instruction cycle boundaries is as follows:

ADSP-2181 PRIORITY CHAIN

1. COMPLETION OF AN EXTERNAL MEMORY ACCESS
2. IDMA INTERNAL MEMORY TRANSFERS
3. BDMA INTERNAL MEMORY TRANSFERS
4. SPORT AUTOBUFFER OPERATIONS
5. EMULATOR INTERRUPT
6. EMULATOR INSTRUCTION
7. POWERDOWN INTERRUPT
8. UNMASKED INTERRUPT
9. NORMAL INSTRUCTION EXECUTION

The 3.5 cycles assumes no external memory operations (multiple external accesses when executing multifunction instructions or an external access with waits states) or Bus Request activity. So in the case of trying to write to the same

memory region (internal) the IDMA port will always execute in 3.5 cycles. Therefore, in this case using /IACK is unnecessary. If your code does contain DMA holdoffs as described in

Chapter 11 of the ADSP-2100 Family user's manual, then you must use /IACK in your design to guarantee that IDMA transfers will always operate properly.

Here is a quick summary of DMA holdoffs:

1) Bus Request
2) External Accesses with waitstates
3) Multiple External Accesses
4) IDLE n Instruction
5) SPORT Autobuffering to external memory with waitstated access
6) EZ-ICE Emulation