Engineer To Engineer Note EE - 17

Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
Phone: (800) ANALOG-D or (781) 461-3881, FAX: (781) 461-3010, EMAIL: dsp.support@analog.com

ADSP-2187L Memory Organization

Last Modified: 5/5/97

Introduction

The ADSP-2187L is a new addition to the ADSP-218x series of DSP microprocessors. The ADSP-2187L shares the same package pinout as the ADSP-2185/2186 processors. With 64K words of on-chip SRAM, the ADSP-2187L performs most algorithms without using external memory.

The processor's internal memory is organized as: 32K words on-chip Program Memory (PM) RAM and 32K words on-chip Data Memory (DM) RAM.

The internal program memory is configured as one permanent 8K segment and three 8K overlay segments that are accessed by the PMOVLAY register.

Internal data memory is configured as one permanent 8K segment and three 8K overlay segments that are accessed by the DMOVLAY register. Two external 8K segments are also available for both PM and DM and are accessed through the PMOVLAY and DMOVLAY registers respectively. This memory organization is shown in Table 1. Memory organization diagrams are shown in Figures 1 and 2.

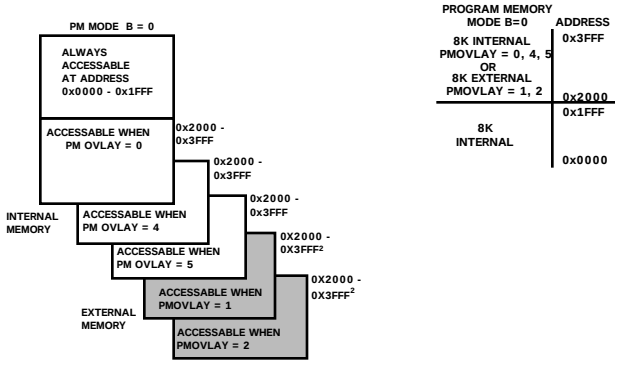

Figure 1. Program Memory Organization

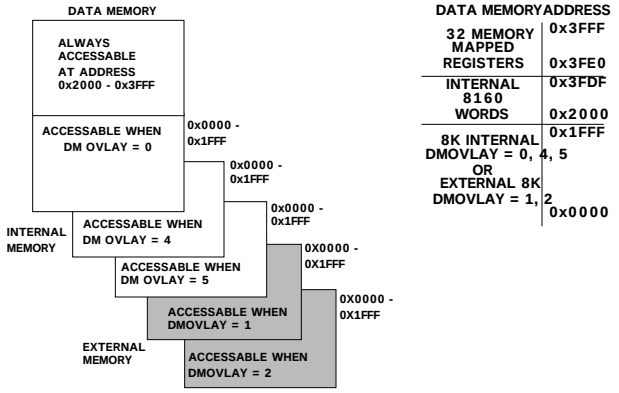

Figure 2. Data Memory Organization

The memory organization differs from other 218x family devices; the internal overlay memory can now be accessed by the IDMA and BDMA ports through two new registers on the ADSP-2187L. These registers are discussed below.

Table 1 - Memory Overlay Pin Configurations

PMOVLAY/ DMOVLAY	MEMORY	A13	A12:0
0,4,5	Internal Overlay	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSB's of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSB's of Address Between 0x2000 and 0x3FFF

Memory Modes

The ADSP-2187L, like the ADSP-2185/2186 can be configured in one of two modes; Full Memory Mode or Host Mode. Four mode pins are used to set memory modes and booting. Mode selection information is located in the ADSP-2187L data sheet.

IDMA Operation (Host Mode)

Host mode provides full use of the IDMA port and access to the full external data bus. However, the use of the external address bus is limited to a single address pin, A0. Additional hardware can be added to generate and latch address signals.

To use IDMA with the ADSP-2187L, the part must be configured in Host Mode. The addition of the IDMA OVLAY Register allows IDMA accesses to the internal overlay memory. A typical IDMA transfer sequence is shown in Figure 3.

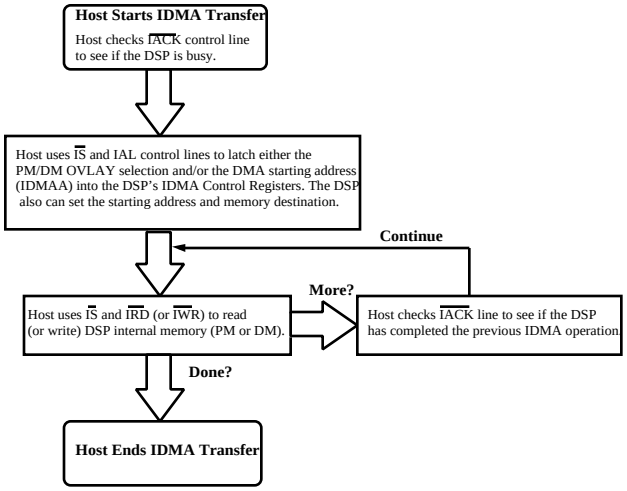

Figure 3. ADSP-2187L IDMA Transfer Sequence

To write to the overlay memory via the IDMA port requires two address latch cycles; one to latch the overlay address and one to latch the starting address. If bit 15 of the IDMA Control Register *(figure 4)* is set to 1, the IDMA port latches the IDMA overlay information. If bit 15 is set to 0, the IDMA port latches the address, and bit 14 determines PM or DM access. If you do not latch the overlay memory, the Overlay Register *(figure 5)* is set to all zeros. If upgrading from a another 218x device to the ADSP-2187L, no additional board hardware is necessary for IDMA transfers.

When beginning a transfer from/to internal PM/DM make sure the overlay page is latched if the program addresses will increment into an overlay segment.

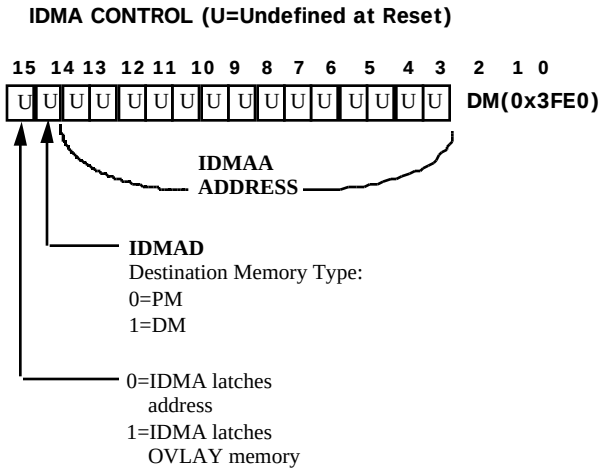

Figure 4. ADSP-2187L IDMA Control Register

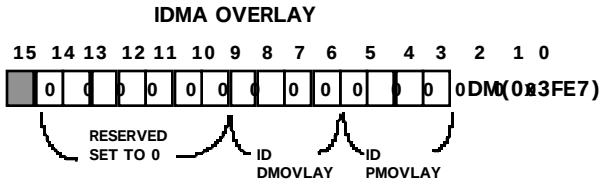

Figure 5. ADSP-2187L IDMA Overlay Register

The following code segment shows an example of writing to the internal overlay memory through the overlay register:

```
ax0=0xe000;

dm(0x3fe0)=ax0;  /*latch overlay
page at DM

                 address 0x2000 */

ax0=0x0005;

dm(0x3fe7)=ax0;  /*latch DM
internal

                overlay */
```

***Note: The above sequence can occur in any order*

The IDMA port on the ADSP-2187L has an additional feature that allows the IACK signal to be configured either as an open drain (can be "wire-or'ed") or as always driven, depending on the state of the MODE D pin. This is useful for applications that require more than one ADSP-2187L to be connected by their IACK pins. Mode selection can be found in the ADSP-2187L Data Sheet.

BDMA Operation (Full Memory Mode)

If the ADSP-2187L is configured for full memory mode, all address and data lines are available and the processor boots from the BDMA port (the IDMA port is disabled). I/O capability is retained in full memory mode as is access to the external data and address buses.

The byte memory space on the ADSP-2187L is an 8-bit wide external memory space which allows up to 4 Mbits of ROM or RAM to be used. Writes to internal memory are done using the Byte DMA Controller. The part must be configured for Full Memory Mode to use the BDMA port.

The BDMA controller of the ADSP-2187L allows access to the internal overlay segments through four BDMA Overlay bits (7:4) in the BDMA Control Register (*figure 6*).

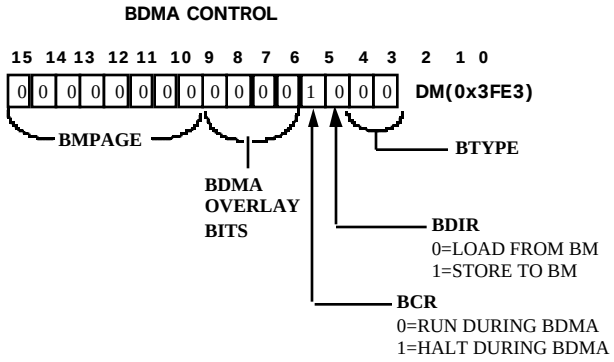

Figure 6. ADSP-2187L BDMA Control Register

The following code segment demonstrates how to set up BDMA registers for a BDMA access to internal overlay memory.

```
ax0=0x0048;

dm(0x3fe3)=ax0;   /* start BDMA
transfer from page

                0,  write to
internal PM overlay,

               use 24-bit words
*/

ax0=0x0000;

dm(0x3fe2)=ax0;   /* load
external addresses beginning

                at 0x0000 */



ax0=0x2000;

dm(0x3fe1)=axo;      /* start
internal addresses at 0x2000
       */

ax0=0x0200;

dm(0x3fe4)=axo;  /* set the count
equal to 512 words */
```