Technical Notes on using Analog Devices' DSP components and development tools
Phone: (800) ANALOG-D, FAX: (781) 461-3010, EMAIL: dsp.support@analog.com, FTP: ftp.analog.com, WEB: www.analog.com/dsp

Minimum Rise Time Specs For Critical Interrupt and Clock Signals on the ADSP-21x1/21x5

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By: JT

Introduction:

The EE-note was created because of questions a customer had about the serial ports on the ADSP-2105. When they got the latest revision of 2105 silicon (0.5 micron process with faster rise/fall times than previous 0.8 micron devices), their serial ports stopped working and the problem was traced to glitches and rise time on SCLK signal. The customer requested information on the Maximum Slew Rate for the ADSP-2105 for an internal/external SCLK (not specified in data sheets), so they could modify their board design to ensure correct SPORT operation. This EE-Note will describe why a minimum rise time specification is important on critical signals such as interrupts and clocks.

The information below discusses the ADSP-2105. However, the same information is directly applicable to other ADSP-21xx 0.5 micron devices such as the 2101, 2111, 2115 and 2162. ADI's recommendation is to ensure that all critical input clock signals should have 'minimum' risetimes of 0.5 V/ns (We do not specify a maximum, it can be much larger than what the DSP part requires for a minimum). For output clocks, we can provide you with a chart detailing typical 2101/21x5/216x /2111 Output Driver I/V Characteristics so you can estimate what the DSP output clock signal rise/fall times will be produced (call our DSP support hotline).

Recommendations For Critical Signals

All input signals are subject to some amount coupling from adjacent traces on a PC board or adjacent pins within the package of a part. This coupling can cause moderate size "glitches" say 50-500mV to become superimposed upon rising or falling signals. If the glitch is wide enough(>1ns) and occurs right around the trip point of the TTL input buffer(1.4V) it may be able to overcome the hysteresis (typically 100-200mV) of the input buffer and pass through the internal logic gates.

Besides good layout practices to reduce coupling, a moderately fast signal rise/fall time should be maintained if possible. For example a 2ns wide 400mV negative glitch which occurs when the input is at 1.6V can cause the input to fall to 1.2V for 2ns and then recover to 1.6V. On a very slowly rising signal the glitch width will be a full 2ns. However, if the signal is rising fairly fast (1V/ns) this 400mV glitch will only be present for 0.4ns. Our input buffers can reject glitches which are below about 1ns, so fast risetimes help by limiting the pulse width of moderately sized glitches. ***All critical signals should have minimum risetimes of 0.5V/ns if at all possible.***

NOTE: **These glitches are most problematic for signals such as Serial Port clocks (SCLK & RFS) or hardware interrupts (/IRQx) which CANNOT glitch at any time.** Data signals for example can glitch during transitions as long as they are stable at the time they are latched. For this reason we add special deglitching input buffers to critical signals. These deglitching input buffers will reject moderately sized glitches better than our standard input buffers.

Additional Information:

Chapter 5 - Serial Ports*, ADSP-2100 Family User's Manual*, Analog Devices, Norwood, MA 0

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