



Hardware Design Checklist for the Blackfin® Processors

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Introduction

This engineer-to-engineer note describes the most common mistakes to avoid when designing with Blackfin® processors. In addition to this document, the designer should read the most current data sheet, hardware reference manual, and silicon anomaly list (available from the Analog Devices web site) for the specific Blackfin processor being used.

General Hardware Problems

The following sections address design issues not associated with memory interfaces or specific peripherals.

NMI Polarity

Double-check the polarity of the Non-Maskable Interrupt (NMI) signal for the processor being used. On several Blackfin processors (the ADSP-BF531/BF532/BF533/BF535 and the ADSP-BF561), the NMI signal is active high. On all the other Blackfin processors, the NMI signal is active low in order to better connect to standard Supervisory parts. Also, please remember that if the NMI signal is not used, it should be tied to its inactive state.



Do not let the NMI signal float, and do not tie it to its active state.

Five-Volt Tolerance

Applying five volts to signals that are not rated for this potential can damage the device and cause malfunction. Blackfin processor inputs should not be connected to the outputs of five-volt devices. Most Blackfin processor signals cannot tolerate five volts. There are a few exceptions, such as some of the Two-Wire Interface (TWI) signals. Level shifters are required on all other processor signals to keep the signal voltage at or below absolute maximum ratings as defined in the specific Blackfin processor data sheet. Level shifters are commonly required for CAN transceivers and the ATAPI interface. Current-limiting resistors do not provide sufficient protection against high voltage.

Unused Signals

Check the end of the signal list description section of the data sheet to see what to do with unused signals. In general, the need to terminate unused signals has been eliminated, but the signals that require termination can be found in the data sheet. Failure to connect unused signals such as /NMI, NMI or /BR may cause symptoms that appear to be power sequence or reset problems. Applications requiring high EMC susceptibility / immunity may terminate all unused signals, if desired.

Signal Integrity

Rapid rise-time and fall-time of signals is a primary cause of signal integrity issues such as intermittent communication failure. The edge rates on the Blackfin processor differ from signal to signal. Likewise, some signals have greater sensitivity to noise and reflections than other signals. Use simple signal integrity methods to prevent transmission-line reflections that may cause extraneous clock and sync signals. Short trace length and series termination are critical for the following signals:

- CLKIN signals should have impedance-matching series resistance at the driver
- SPORT interface signals ($TCLK$, $RCLK$, RFS , and TFS) should use termination
- PPI signals, such as PPI_CLK and Sync signals, also benefit from these standard signal integrity techniques
- SDRAM clocks, control, address, and data can benefit from series termination that also reduces unwanted EMI

In cases where signals have multiple sources, it will be difficult to keep the traces short, and simulation may be appropriate. IBIS models that can assist with signal simulation are available from the Analog Devices web site.

Some new and future Blackfin processor family members will support additional signal integrity features such as programmable input hysteresis or programmable output drive strength. Consult the appropriate hardware reference manual for details.

Test Points and Signal Access

The debug process can be aided by adding test points on signals such as $CLKOUT$ or $SCLK$, bank selects, PPI_CLK , and $/RESET$. If selection inputs such as Boot Mode ($BMODE$) are connected directly to power or ground, they will be inaccessible under a BGA-package chip. For debugging, it is helpful to use pull-up and pull-

down resistors instead of tying inputs directly to power or ground.

Bypass Capacitors

Appropriate bypass capacitors on the internal power supply become critical at higher operating speeds. Unwanted parasitic inductance in capacitors and traces reduces the effectiveness at high frequency. Two things are needed when processors operate above 100 MHz. First, capacitors should be physically small and their leads should be short to reduce inductance. Surface mounted capacitors of size 0402 will yield better results than larger sizes. Second, lower values of capacitance will raise the resonant frequency of the LC circuit. Although several 0.1 uF capacitors work well below 50 MHz, a mix of 0.1, 0.01, 0.001 uF and even 100 pF is preferred in the 500 MHz range for V_{DDINT} .

Driving /RESET

The inputs of most Blackfin processors have no hysteresis, thus, they require a monotonic rise and fall. Therefore, even the $/RESET$ signal should not be connected directly to an R/C time delay because such a circuit would be noise sensitive. Instead, $/RESET$ should be provided through a reset supervisory chip.

Board to Board Communications

Some communication standards such as CAN and TWI have special requirements when unpowered. For example, an unpowered pull-up resistor may cause excessive leakage, thereby disrupting communication between other units on the bus. This unpowered situation is a common consideration in 'hot swap' applications.

JTAG

The Blackfin processor JTAG reset pin, $/TRST$, should be pulled down in normal operation. An application note is dedicated entirely to

considerations for JTAG connections. Refer to *Analog Devices JTAG Emulation Technical Reference (EE-68)*^[1] for details.

GPIO Port Signals Used as Inputs and Outputs

At power-on reset, all general purpose signals are inputs. During the boot process, some of these signals may change to outputs, depending on the selected boot mode. For parts with `HWAIT`, this signal is an output for all boot modes. Output signals should not be used as inputs when driven by an external device. `HWAIT` should not be used as an output if the value is critical during the booting phase of operation.

GPIO signals used as outputs should have pull-up or pull-down resistors to determine their state after reset. Outputs to be considered here include device enables (such as NAND flash) and communication handshake signals. Some examples are `HWAIT`, `UARTxTX`, `UARTxRTS`, `CANxTX`, SPI slave-select inputs and outputs, serial TWI, and all chip select signals.

Some general-purpose outputs that can be used at 5 V like `SDA` and `SCL` are open-drain in all modes. These are listed in the datasheet and require pull-ups to function as a general-purpose output. Signal capacitance may limit the output speed of these signals.

Using EZ-KIT Lite® Schematics

The EZ-KIT Lite evaluation system schematics are a good starting reference. Because the EZ-KIT Lite board is for evaluation and development, extra circuitry is provided in some cases. Read the EZ-KIT Lite board schematic carefully because sometimes a component is not populated and sometimes extra components have been added to make it easier to modify or measure.

Asynchronous Memory

Bus Request

The Bus Request signal (`/BR`) requires a pull-up resistor in all designs. Erroneous bus requests will prevent bus operation if this signal is not pulled up or driven by an external device.

Asynchronous Bus / GPIO Signal Muxing Considerations

Asynchronous bus signals may be multiplexed with GPIO functions on some Blackfin processors. This may require the bus request GPIO to be programmed as bus request and require that GPIO be connected to a pull-up, as described above.

As shown in the signal description, some processors allow some unused bus signals to be used as general-purpose input/output signals. However, if the asynchronous bus is used for booting, all address signals will be driven. Also, on some processors, `/BG` and `/BGH` will be driven during the boot process and `/BR` is used as an input. This occurs when `BMODE` is set to parallel memory or, for processors featuring One-Time Programmable (OTP) memory, when the asynchronous bus is enabled by OTP programming.

Other processors share other asynchronous bus signals with GPIO. Consult the booting section of the hardware reference manual for details.

8/16-Bit Memories

Remember to use the proper addresses to connect to 8-bit memory on the `ASYNC` memory banks. Because there is no true byte addressing to external memory, 8-bit memory is addressed the same as 16-bit memory. Use `A1` (not `/ABE0` or `/ABE1`) as the LSB of the address. 16-bit memory with byte enable signals can be accessed 8 bits at a time. Otherwise, 16-bit memories are word wide only. Blackfin devices with a 32-bit `EBIU`

can be programmed to connect with 16-bit memory, using /ABE3 as the least significant address of the external device. Refer to the processor's hardware reference manual for more information.

ARDY

If not used, ARDY can be terminated. In addition, ARDY can also be programmed to be ignored via software. If ARDY is used, consult the hardware reference manual. Some Blackfin devices require the ARDY input to be synchronous to SCLK (CLKOUT).

Hibernate Considerations

The datasheet may indicate that all external signals are tristate during hibernate. This includes bus strobes. Pull-up resistors are required on peripheral chip selects such as /AMSx.

Other External Bus Interface Control Signals

Although not required, pull-up resistors should be considered for all active low bus control signals to guarantee their state during power up and power down. Future Blackfin family members may have many device control signals multiplexed with GPIO and other functions. These may require pull-up resistors to prevent data corruption and bus contention during reset and prior to configuration.

SDRAM Memory

SDRAM Bank Addressing

- Use ADDR18 to connect to BA0.
- Use ADDR19 to connect to BA1.

SDRAM Address SA10

Use SA10 to directly connect to A10 of the SDRAM device. SA10 replaces the Blackfin processor's ADDR_x, based on whether a 16- or 32-

bit (for 32-bit-wide external memory interface derivatives) device is connected to the SDRAM interface. As an example, for an ADSP-BF561 Blackfin processor, SA10 replaces ADDR11 when a 16-bit SDRAM device is used, and SA10 replaces ADDR12 when a 32-bit device is used. On the ADSP-BF533 Blackfin processor, SA10 replaces ADDR11. Note that the replaced ADDR_x signal is not used. Therefore, the next higher processor address is connected to A11 of the memory. Refer to the "SDRAM Address Mapping" section of the hardware reference manual for details.

Hibernate Considerations

A pull-up resistor is recommended on /SMS.

Synchronous DDR Memory

DDR PCB Layout

Proper PCB layout is a requirement of any DDR memory design. Review the AC timing and specifications listed in the processor datasheet. Signal timing is a combination of device timing and the characteristics of the printed circuit board. Trace length difference, cross-talk, and voltage change may account for 300 to 500 ps of timing error. Follow the layout recommendations given by the memory manufacturer. Of critical importance is the reduction of DQS0 to DQ0-7 skew and DQS1 to DQ8-15 skew. The amount of allowed skew can be improved with the use of fast speed grade memory. Use careful trace length matching and increased spacing to reduce crosstalk. Serpentine traces should have a spacing of four times the trace width to provide sufficient delay. The trace length for the DCLK0-1, DQS0-1, DQM0-1 and DQ0-15 signals should be less than 3.5 inches. DDR_VSSR should be connected directly to ground at the processor. DDR_VREF should be a low-impedance 30 mil wide connection.

DDR Termination

Use series termination on all data, address and control signals for up to four memory devices.

Hibernate Considerations

Pull-up resistors are recommended on the /DDRC_S chip selects.

Synchronous Burst Flash Memory

Some Blackfin family members can attach directly to burst mode and page access mode flash devices. Care must be taken if the device functions as a boot source. If the Blackfin processor resets itself by a software reset command or watchdog timer event, the processor and memory may then operate in incompatible access modes. Use the `OTP_RESETOUT_WAIT` feature to instruct the processor to configure the flash device before reboot. Consult the hardware reference manual and datasheet for booting, timing and connectivity information.

Hibernate Considerations

Pull-ups are required on peripheral chip selects such as /AMS_x.

SPI Interface

Bootting

SPI Master Boot mode requires a pull-up resistor on the GPIO signal used as the chip-select for the SPI memory device. The name of the chip-select changes from one Blackfin processor to another. Check the SPI booting section of the Blackfin processor's data sheet to find the SPI /CS connection for booting. Most current processors require a pull-up resistor on MISO. In all SPI systems, SPI_SCK is best used with a pull-down resistor to define the initial state and to reduce noise. Also, refer to the "SPI Master Booting"

section of the application note *ADSP-BF533 Blackfin Booting Process (EE-240)*^[2].

MOSI and MISO

The SPI interface requires that all MOSI signals are tied together and all MISO signals are tied together. To prevent contention and possible damage to the device, double-check that these signals have not been interchanged. Connect MISO to MISO and MOSI to MOSI. If the peripheral signal names are DIN or DOUT, connect them according to their master or slave function. Proper schematic signal names will reduce confusion.

Two-Wire Interface

The Two-Wire Interface is an I2C-compatible peripheral. Because SCL and SDA are open drain outputs, both TWI signals need pull-up resistors just like the I2C standard requires them.

SD/SDIO Interface

The Secure Digital (SDIO) interface is designed such that it requires no external pull-ups or pull-downs in most applications. SD/MMC cards may require a weak pull-up on SD_CMD. Other resistor functions are provided internal to the processor. However, impedance-matching series termination resistors should be added on all signals. Consult the SD specification and the timing numbers in the datasheet to determine the maximum frequency for supporting both standard and high-speed SD devices. Also consider the time of flight if the SD connector is located remotely.

SPORT Interface

SPORTs in multi-channel mode that master the clocks and frame syncs should not connect TFS to RFS. In this mode, the TFS frames the active transmit channel data in the role of a Transmit Data Valid (TDV) signal.

Clock Input Signals

CLKIN

The clock input to the Blackfin processor should start toggling after power-up and be continuous while power is applied.

XTAL

When using an oscillator output instead of a crystal, the XTAL output signal should not have a capacitor to ground. It is shown this way on some EZ-KIT Lite board schematics. Note that it is not populated on the board, and it should not be populated in an end design.

Crystal Inputs

In addition to the clock source for the processor core CCLK and the peripheral clock SCLK, some Blackfin processors have additional clock domains. Examples are Real-Time Clock, Ethernet, USB and MXVR. Like CLKIN and XTAL, these clock domains can use a crystal or an external clock can drive the input signal. The external clock may be square wave or sinusoidal. If using a sine wave, the voltage levels must be kept within the minimum and maximum limits found in the datasheet. Some peripheral XTAL pins may also be driven by the CLKBUF output of some processors. If using an external clock instead of a crystal, the corresponding XTAL output signal must be left floating. If using a crystal, check the datasheet and crystal specifications for recommended series or parallel resistors. It is important not to overdrive small crystals. If a clock domain is not used by your application, pull the input clock high or low to prevent oscillation.

Power Regulator

A software controlled internal regulator circuit using an external FET, diode and inductor is offered on some Blackfin family processors. The

core voltage (V_{DDINT}) can also be powered with standard external regulation. The internal voltage regulator may be an attractive option for some designs using power management that controls both clock speed and core voltage.

Be aware that the internal voltage regulator is a switching regulator circuit (not a linear regulation circuit). Ensure that the diode shown in the data sheet is present. Keep the VROUT signal trace short, as this signal can be a source of radiated noise! Refer to the application note *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)*^[3] for further details on component selection.

New power control functions have been added to some Blackfin Processors. A VRSEL input selects internal regulator or external regulator mode. An EXT_WAKE output may be provided to turn off an external regulator when using hibernate state. It is a high true power-up signal that can be connected directly to the low true shut down input of many regulators.

A PG or SS/PG signal is a feature on some processors. In internal mode, SS/PG can be used to give a Soft Start at power up and at the end of hibernate. In external mode, it can be used as a low true Power-Good signal to safely start core processing after wake from hibernate mode.

Multiple Power Domains

Does your design require a battery for continuous time information? If not, connect the RTC power to V_{DDEXT} even if the RTC is not used. All power and ground signals must be connected at levels described in the datasheet. This is true if you do not use the associated peripheral and is even true if the peripheral does not exist on the processor being used in the design. Failure to drive all voltage connections may result in JTAG failures and improper initialization and operation.

USB OTG Interface

Several members of the Blackfin family of processors allow a direct physical USB interface. This is also called the Universal Transceiver Macro Interface in the hardware reference manuals.

USB Clocking of USB_XI

An external crystal or crystal oscillator is required to generate the internal USB2 high-speed clock. The frequency should be chosen to operate the internal clock at 960 MHz. External frequency and programmed multiplication values can be any combination that gives a half speed clock of 480 MHz. The circuit shown in the corresponding datasheet for CLKIN connections can also be used as an example for this clock.

USB_ID

USB_ID is unique to USB OTG. It allows the OTG cable to determine host (A-Device) or peripheral (B-Device) initial status of the interface. If not using OTG but using the USB interface as a host (A-Device), this pin should be grounded. If not using OTG but using the interface as a USB peripheral (B-Device), USB_ID can be left floating or connected to a weak pull-up.

D+ and D- Connection

The Blackfin USB_DP and USB_DM signals should be routed as an impedance-controlled differential pair directly to the D+ and D- of the USB connector. Traces should have no extraneous side

traces, sometimes called stubs. Further care should be taken to isolate this differential pair from high-speed signals or other noise sources like VROUT. The Blackfin processor provides termination resistance needed for OTG compliance.

USB_VBUS Connection

USB_VBUS is an input to the processor, except when programmed to output Session Request pulses. When using host or OTG (A-Device) mode, an external 5 V source of more than 8 mA is required to drive USB_VBUS on the cable. This supply needs to be fully disabled when in OTG (B-Device) mode. A GPIO signal should be used for enable/disable. USB_VBUS should be connected directly to the USB connector.

Check the datasheet for 5 V tolerance of USB_VBUS. Some processors are not 5 V-tolerant if V_{DDUSB} external power is zero volts. A few applications may expect their products to experience very long exposure to 5 V on USB_VBUS when the processor has no local power. These applications may wish to provide power to V_{DDUSB} by using the 5 V power from USB_VBUS. An example of such a protection circuit can be found in the ADSP-BF548 EZ-Kit lite schematics.

USB ESD Protection

Additional ESD protection is recommended on cable signals USB_DP, USB_DM, USB_ID, and USB_VBUS. Protection devices should be placed near the connector.

References

- [1] *Analog Devices JTAG Emulation Technical Reference (EE-68)*. Rev 10. April 2008. Analog Devices, Inc.
- [2] *ADSP-BF533 Blackfin Booting Process (EE-240)*. Rev 3. January 2005. Analog Devices, Inc.
- [3] *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)*. Rev 1. February 2005. Analog Devices, Inc.
- [4] *Estimating Power for ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)*. Rev 4. December 2007. Analog Devices, Inc.

Document History

Revision	Description
<i>Rev 1 – October 19, 2005 by Robert Kilgore</i>	Initial release
<i>Rev 2 – July 7, 2008 by Robert Kilgore</i>	Added information to cover new peripherals and features in the Blackfin processor portfolio