ANALOG DEVICES

Using External Switching Regulators with Blackfin® Processors

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Introduction

The Blackfin® family of embedded processors includes an optional internal programmable pulse width modulation (PWM) voltage controller. Together with a set of external components, the PWM controller provides an adjustable internal voltage power supply that can be applied to the core and on-chip memory.

This EE-Note describes how an external regulator can be used in conjunction with the internal voltage controller to:

- Improve dynamic performance

- Improve efficiency

- Improve stability

- Reduce the PCB area required

- Reduce the rating required for the external components

This EE-Note also provides guidelines for designing such a regulator and gives test results from prototype circuitry designed using the recommendations herein. Also described is a method for using the behavior of the on-chip regulator to control the external regulator when the Blackfin processor is transitioned into the ultra-low power hibernate state.

Connecting Blackfin Processors to an External Buck Regulator

The structure of the internal voltage regulator is based on a very simple voltage controller. It does not include current-limiting functionality or synchronous rectification. It also does not include soft start capabilities. Figure 1 shows the recommended external circuitry to complete the regulator design, which includes a power FET (Q1), a diode (D1), an inductor (L1), and several capacitors (C1 - C5). See *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-328)*[1] for details regarding component selection for this circuit and regulator design techniques and calculations for regulator-related specifications (e.g., efficiency).
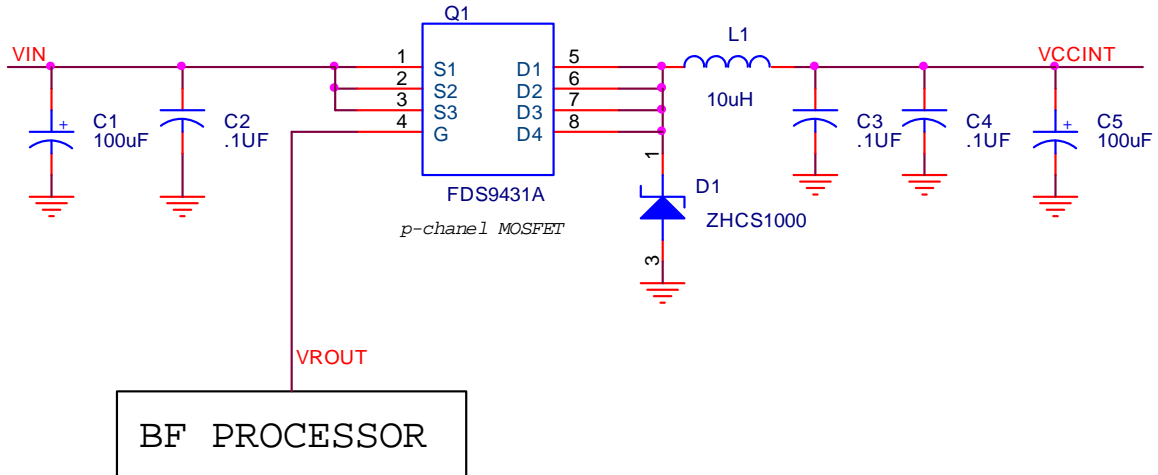
Figure 1. Recommended regulator circuit design

In conjunction with the design shown in Figure 1, the goal is to interface to an external adjustable buck converter, shown in Figure 2:
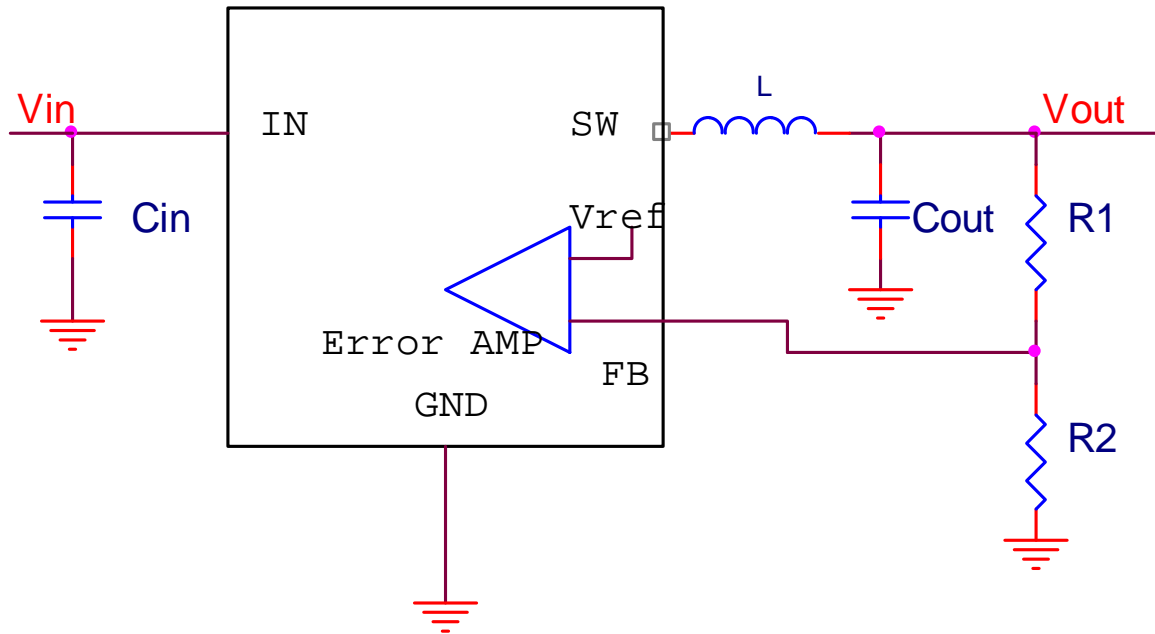

Figure 2. External adjustable buck regulator

The regulator output voltage (V_{out}) is determined by the voltage divider created between R1 and R2 connected to feedback pin (FB), according to Equation 1:

$$V_{out} = V_{ref} * (1 + R1/R2)$$

Equation 1. Regulator output voltage

In Equation 1, V_{ref} is the regulator's internal voltage reference specification.

The configuration of the R1/R2 voltage divider may be modified with an additional resistor (R3) and an additional voltage source from the on-chip regulator (V_{cntrl}), as shown in Figure 3.
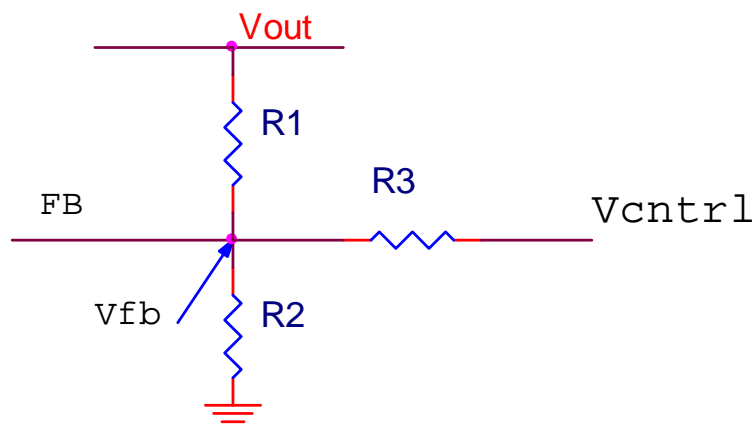

Figure 3. Modified voltage divider circuit

The fact that the Buck converter is a closed-loop feedback system allows the assumption to be made that the voltage on FB (V_{fb}) is equal to the internal voltage reference V_{ref}.

Since $V_{fb} = V_{ref}$, V_{out} may then be calculated using a modified version of Equation 1 that takes the second voltage divider circuit into account, as shown in Equation 2:

$$V_{out} = V_{ref} * (\ 1 + R1/R2 + R1/R 3) - V_{cntrl} * (R1/R3)$$

Equation 2. Modified regulator output voltage

As indicated in Equation 2, V_{out} is a function of the buck regulator's internal voltage reference (V_{ref}), the additional external voltage (V_{cntrl}), and the ratios of the R1, R2, and R3 resistors connected to the feedback pin (FB) of the regulator. If the VR_{out} pins of the Blackfin processor are connected through a low-pass filter to resistor R3, an internal voltage regulator is formed using the Blackfin processor's voltage controller as part of an additional feedback loop.

The voltage on the VR_{out} pins of the Blackfin processor is a PWM voltage with a duty cycle D[1]. After passing this through the low-pass filter, the generated DC voltage (V_{cntrl}) can be expressed as:

$$V_{cntrl} = D * V_{in}$$

Equation 3. Voltage generated by on-chip regulator

In Equation 3, V_{in} is the DC supply voltage on the I/O pins of the Blackfin processor.

Choosing External Components

Now that the connection between the on-chip regulator's complementary external circuitry and the external buck regulator circuitry has been defined, the next step is to determine the values for all the parameters and components to provide reliable regulator operation.

Known Values

The values for some of the components and parameters are already known. V_{out} can be obtained from the processor data sheet as the acceptable V_{DDINT} range. For example, the 500-MHz ADSP-BF534 Blackfin processor[2] defines this range to be $V_{out(min)} = 0.8$ V to $V_{out(max)} = 1.32$ V, and the default value at power-on is 1.2 V. Note that this range equates to 0.85 V to 1.20 V in terms of programmable values in the on-chip regulator after the regulator's specified tolerance is factored in.

V_{in} can be obtained from the processor data sheet[2], as well, from the specification for V_{DDEXT}. Using the ADSP-BF534 Blackfin processor as the example again, $V_{in(nom)} = 3.3$ V, and the specified range is $V_{in(min)} = 2.7$ V to $V_{in(max)} = 3.6$ V.

V_{ref} can range from 0.6 V to 1.2 V, as determined by the manufacturer's specifications for the regulator. R1 and R2 are also usually specified by the buck regulator's manufacturer.

To provide a specific dynamic range margin for the Blackfin processor's on-chip controller, D should be in the range of 0.2 – 0.7 [1]. Using Equation 3, the range of V_{cntrl} can be determined:

$$V_{cntrl(min)} = D_{min} * V_{in(min)} = 0.54 \text{ V}$$

$$V_{cntrl(max)} = D_{max} * V_{in(max)} = 2.52 \text{ V}$$

Unknown Values

The values of R3 and the parameters for the low-pass filter components can be calculated from the known values described in the previous section.

Because of the large variation in the values for R1 and R2 that are recommended by different regulators manufacturers, the ratios R1/R2, R1/R3 and R1/R2 should be used instead for the calculations.

If it is assumed that R2 = R3, then the ratios R1/R2, and R1/R3 are also equal. As such, Equation 2, for the maximum core voltage ($V_{out(max)}$), may be rewritten as:

$$V_{out(max)} = V_{ref} * (1+2R1/R2) - V_{cntrl(min)}*(R1/R2)$$

Equation 4. Maximum regulator output voltage

If $V_{ref} = 0.8$ V, the R1/R2 ratio can be obtained by solving Equation 4:

$$1.2 = 0.8 * (1 + 2 * R1/R2) - 0.54 * R1/R2$$

This gives R1/R2 = 0.4 for $V_{ref} = 0.8$ V.

This process can be employed for any value of V_{ref}. For example, if V_{ref} is 0.6 V, the optimal R1/R2 ratio is 0.9. Similarly, if V_{ref} is 1.0 V, the optimal R1/R2 ratio is 0.43.

With R1/R2 = 0.4 and V_{ref} = 0.8 V, Equation 4 can be solved for V_{cntrl} in terms of the duty cycle from the PWM controller (D), as defined by Equation 3. In other words:

$$V_{out} = V_{ref}*(1 + 2 * R1/R2) - (D * V_{in})*(R1/R2)$$

Equation 5. Modified regulator output voltage

Recalling that V_{in} ranges from 2.7 V to 3.6 V, with a nominal value of 3.3 V, Table 1 shows the requirements for D for various desired V_{out} levels using Equation 5 and given that R1/R2 = 0.4 for V_{ref} = 0.8 V.

Parameter	V_{out} (V)				
	1.20	**1.10**	**1.00**	**0.90**	**0.80**
D ($V_{in(min)}$)	0.22	0.31	0.41	0.50	0.67
D ($V_{in(nom)}$)	0.18	0.26	0.33	0.40	0.54
D ($V_{in(max)}$)	0.17	0.24	0.30	0.37	0.50

Table 1. Duty cycle requirements

As seen in Table 1, all D values are within the range defined by the preliminary assumptions. Further, taking the data from Table 1, Equation 3 can be applied to obtain values for V_{cntrl} as shown in the following table.

Parameter	V_{out} (V)				
	1.20	**1.10**	**1.00**	**0.90**	**0.80**
V_{cntrl} (V)	0.60	0.85	1.10	1.32	1.80

Table 2. Voltage from VR$_{out}$

Before it can be used as V_{cntrl}, the VR$_{out}$ PWM signal should also be low-pass filtered. The best way of implementing a low-pass filter function is by splitting R3 into two resistors, R3a and R3b, and putting a filtering capacitor C3 to GND, as shown in Figure 4:
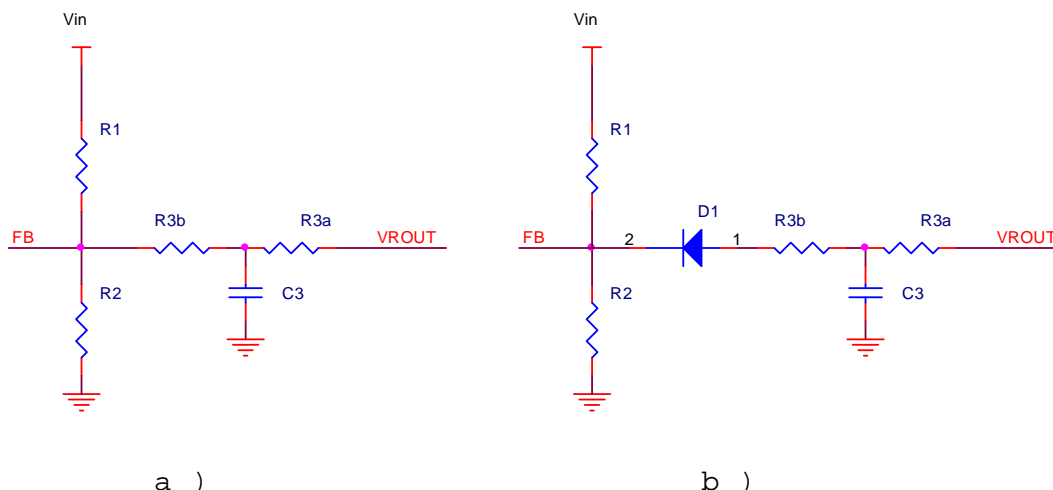
Figure 4. Low pass filter recommendations

The capacitance for C3 may be chosen from the cut-off frequency equation for the low-pass filter:

$$f_c = \frac{1}{2\pi R_3 C_3}$$

Equation 6. Low-pass filter cut-off frequency

In order to provide effective filtering of the 1-MHz PWM VR_{out} signal (and not reduce the bandwidth of the external regulator), the cut-off frequency should be chosen to be around 100 kHz. Diode D1 shown in Figure 4b serves as a decoupling component for the impedance of the VR_{out} pins in order to prevent additional biasing of regulator feedback input. The diode's forward voltage (V_{df}) should be low enough to not substantially increase the value of the needed V_{cntrl} signal. A Panasonic Schottky barrier diode MA27D29 has a V_{df} of 0.25 V, which is low enough to be used in this application. For other diodes, the calculation of R1/R2 should be made after adding V_{df} to $V_{cntrl(min)}$.

Practical Implementation and Test Results

The PCB layout and the lead-lag compensation of the error amplifier of the external voltage regulator are the most critical aspects of a practical implementation of core power supplies using this method, as the additional feedback loop from the Blackfin processor's voltage controller may cause instability for that power supply.

In the PCB layout process, designers should follow the recommendations of the chosen regulator's manufacturer. In most of the voltage regulator specifications, the recommended PCB layout is given, and designers should make their PCB layout resemble that recommended layout as close as possible.

Configuration of and values for the error amplifier compensation components are given by the chosen voltage regulator's manufacturer. Usually, following these recommendations will provide stable operation of the regulator. If the regulator is unstable with the recommended values of compensation components, try to make compensation more "stiff" by decreasing the value of the compensation resistor and proportionally increasing the value of the compensation capacitor.

The Blackfin processor's internal voltage regulator was successfully implemented with several external regulators. Linear Technology's LTC3406 step-down regulator was tested with the ADSP-BF537 and ADSP-BF533 Blackfin processors. The LTC3406 did not require any external compensation.

Linear Technology's LTC3411 was verified with the dual-core ADSP-BF561 Blackfin processor. For this system to work reliably, compensation was necessary. Specifically, additional external resistance (R_c = 1.3 kΩ) and capacitance (C_c = 10,000 pF) were needed.

Finally, the Analog Devices ADP3051 buck switching regulator was verified for the ADSP-BF537 Blackfin processor. Again, to ensure reliability, compensation components were needed (R_c = 6.2 kΩ, and C_c = 3,900 pF).

The schematic for the core voltage power supply using the ADP3051 regulator is shown in Figure 5. The NAND gate in U7, the R194 and R219 resistors, the C91 and C92 capacitors, and the D9 diode form the circuitry responsible for the "hibernate wake-up" function of the core voltage supply. Pin 7 of the voltage regulator from U7 is the shutdown signal (/SHDN). /SHDN should be high during normal operation and low when the processor is in hibernate state.

The operation of this circuit is based on two assumptions that are derived from the behavior of the VR_{out} pins when using the Blackfin processor's on-chip regulator. First, during the normal modes of operation, the VR_{out} signal is always a PWM signal. Second, in hibernate state, VR_{out}, is driven high.
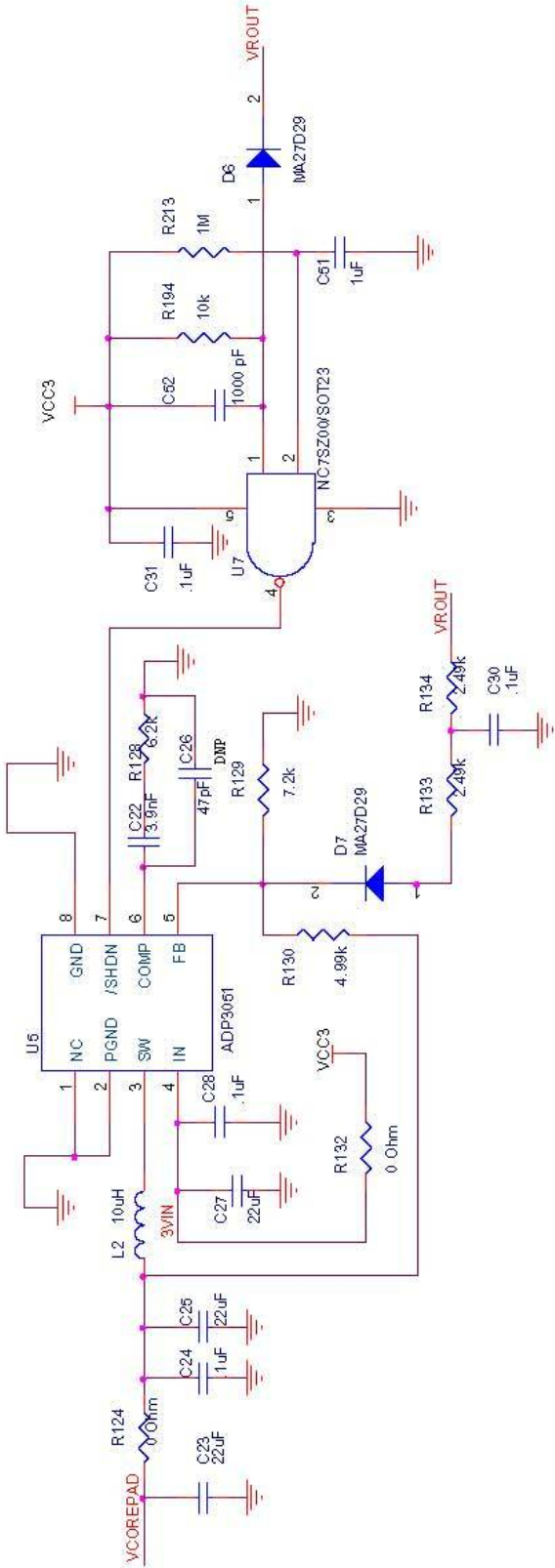
Figure 5. Core voltage power supply schematic

The timing diagram depicting transitions between any of the "normal" operating modes and hibernate state is presented in Figure 6.
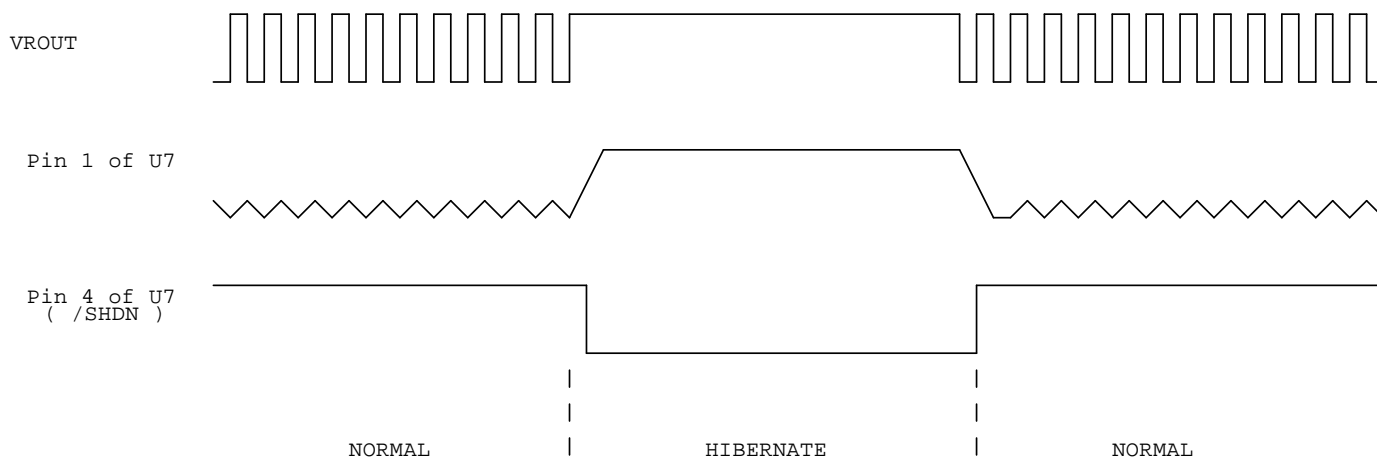

Figure 6. Timing diagram for transitions between normal modes of operation and hibernate state

The efficiency of this regulator design can also be analyzed. Again, see *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-328)* [1] for details regarding how to calculate efficiency. Table 3 captures the efficiency rating for the recommended design given various loading conditions at four discrete preset levels for V_{out}.

Conditions (Load, V_{out} Level)	V_{in} (V)	V_{ddint} (V)	I_{in} (mA)	I_{ddint} (mA)	P_{in} (mW)	P_{ddint} (mW)	Efficiency (%)
Low, 1.20 V	3.3	1.255	23.2	54.2	76.56	68.02	88.8
Low, 1.00 V	3.3	1.049	16.0	41.1	52.80	43.11	81.6
Low, 0.90 V	3.3	0.940	12.8	35.8	42.24	33.65	79.7
Low, 0.80 V	3.3	0.890	11.7	32.6	38.61	34.47	89.3
Medium, 1.20 V	3.3	1.260	43.7	103.2	144.2	130.0	90.2
Medium, 1.00 V	3.3	1.055	29.0	78.9	95.70	83.24	87.0
Medium, 0.90 V	3.3	0.943	22.9	68.5	75.57	64.59	85.4
Medium, 0.80 V	3.3	0.897	22.4	65.5	73.92	58.75	79.5
High, 1.20 V	3.3	1.278	76.3	181.7	251.8	232.2	92.2
High, 1.00 V	3.3	1.067	51.4	142.5	169.6	152.1	89.6
High, 0.90 V	3.3	0.951	41.7	124.0	125.1	118.0	95.1
High, 0.80 V	3.3	0.901	36.3	115.3	119.8	103.9	86.7

Table 3. Efficiency rating for regulator design at various loads and V_{out} levels

Finally, an oscilloscope plot was captured, showing the voltage response when transitioning from the hibernate state to the full-on mode of operation. Figure 7 depicts the relationship between the core voltage (V_{DDINT}) and the on-chip regulator's oscillation output over the VR_{out} pins.
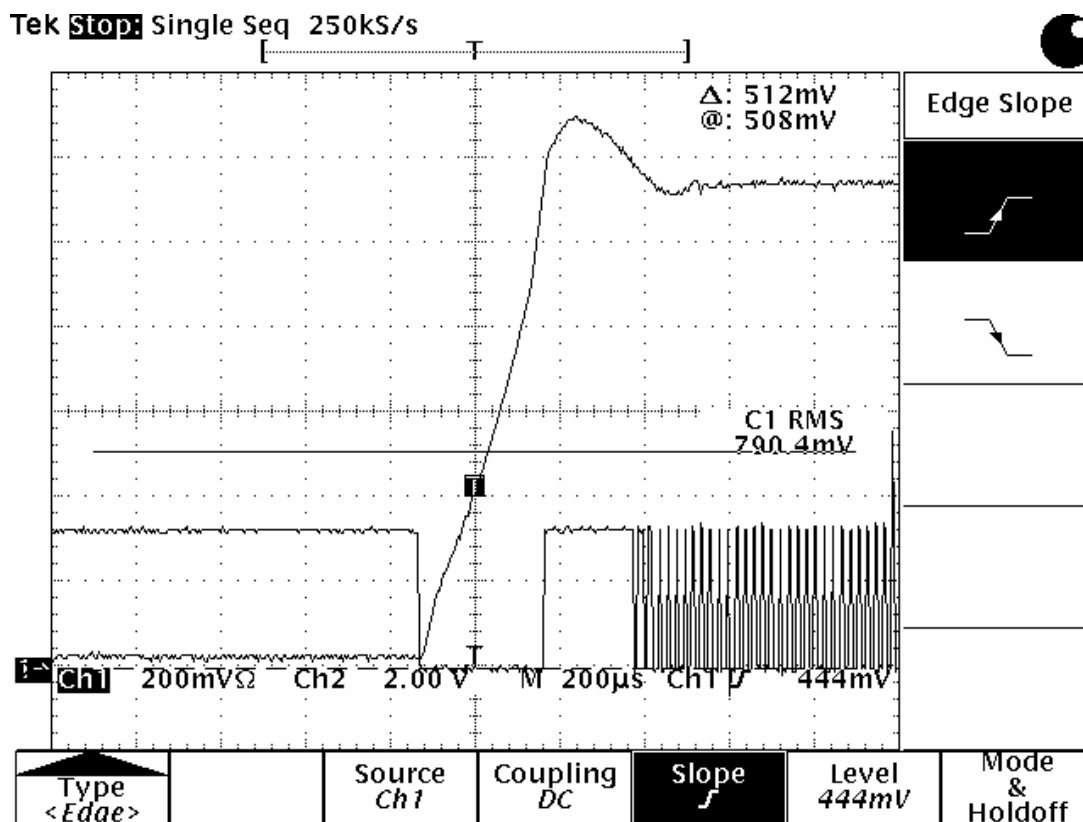
Figure 7. Oscilloscope plot for transition from hibernate state to full-on mode of operation

In Figure 7, channel 1 is the upper trace, which is the V_{DDINT} plot at 200 mV/division, and channel 2 is the lower trace, which is the VR_{out} signal at 2.0 V/division.

References

[1] *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-328).* Rev 1, February 2005. Analog Devices, Inc.

[2] *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Embedded Processor Data Sheet.* Rev F, May 2008. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – May 14, 2008 *by T. Seliverstov*	Initial Release