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Power Mode Transition Times of Blackfin® Processors

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Introduction

This application note describes how Blackfin® processors transition between their operating modes. Specifically, the number of cycles required to move into and out of each of the following modes - `Full-On`, `Active`, `Sleep`, `Deep-Sleep`, and `Hibernate` - will be described. The times for each of these transitions are summarized. In addition, the process to change the PLL `VCO` frequency is discussed. This information will help system designers balance the power saving and performance aspects of their applications.

The measurements in this note were taken on an ADSP-BF533 EZ-KIT Lite® evaluation system.

General Mode Transition

Blackfin processors support five operating modes, each of which has different power saving characteristics, as shown in Table 1. They can be programmed on the fly to switch among these modes to meet specific power saving and performance requirements. Figure 1 illustrates all the supported transitions and the conditions under which they occur.

A write to the `STOPCLK` or `PWDN` bits of the PLL control register (`PLL_CTL`[1]), can switch the processor from a running state (`Full On` and `Active`) to a dormant state (`Sleep` and `Deep-Sleep`). To get into `Hibernate` mode from one of the running states, a write of `b#00` to the `FREQ` bits of the voltage regulator control register (`VR_CTL`[1]) is needed.

Mode	PLL	PLL Bypass	CCLK*	SCLK*	V_{DDINT}	V_{DDEXT}
Full On	Enabled	No	On	On	On	On
Active	Enable /Disable	Yes	On	On	On	On
Sleep	Enabled	-	Off	On	On	On
Deep Sleep	Disabled	-	Off	Off	On	On
Hibernate	Disabled	-	Off	Off	Off	On

** CCLK is Core Clock, and SCLK is System Clock.*

Table 1. Operating Modes

Writes to the `PLL_CTL` and `VR_CTL` registers must be followed by the PLL programming sequence[1], shown in Listing 1, in order for the changes to take place. After the `IDLE` instruction is executed, the processor begins to transition to the intended mode.

```
/* Enable wakeup on certain sources */
p1.h = hi(SIC_IWR);
p1.l = lo(SIC_IWR);
r0.h = 0x0000;
r0.l = 0x0080; /* this value is for
                  RTC, to be changed to
                  reflect other sources
                  */
[p1] = r0;

Cli r0; /* Disable interrupts*/
Idle;
Sti r0; /* Enable interrupts, not
           needed for Hibernate mode */
```

Listing 1. PLL Programming Sequence

A valid wakeup signal can wake the processor up from a dormant state to a running state. The wakeup signals include PLL wakeup, all peripheral wakeups, and hardware reset. Different modes may have different wakeup conditions (see Figure 1 for details). Other than hardware reset, all wakeups can be enabled or disabled by setting the system interrupt wakeup-enable register (SIC_IWR[1]). This is useful to ensure that only the desired wakeup signals are used to wake up the processor.

After the processor wakes up, it takes approximately 10 CCLK clocks to execute the first instruction following IDLE. This is because the ten-stage instruction pipeline of the core is flushed before the core gets into IDLE. When the core resumes execution, 10 core clocks are needed to fill up the pipeline and to execute the first instruction.

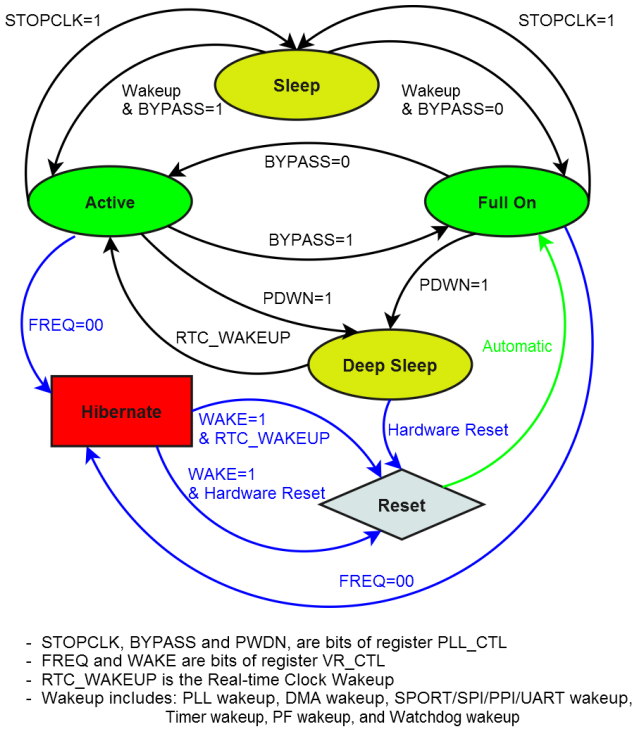

Figure 1. Operating Mode Transition

All the transitions from a running state to a dormant state must go through the IDLE state, during which the processor finishes its previous operations, idles the core, and notifies the PLL or the on-chip core voltage regulator to take actions according to the settings of the PLL_CTL and VR_CTL registers. These two registers, as well as SIC_IWR, must be properly set before entering the IDLE state.

Some of the mode transitions involve enabling/disabling the PLL bypass. This operation can be simplified as shown in Figure 2. When bypass is enabled, the bypass switch connects to CLKIN so that the source of both CCLK and SCLK is selected as CLKIN. Otherwise, VCO, the output of the PLL, is selected to derive CCLK and SCLK. In order to avoid glitches on CCLK and SCLK, the processor disables both for 3-4 CLKIN clocks when the bypass switch goes from VCO to CLKIN, and for around two CLKIN clocks when it switches from CLKIN back to VCO.

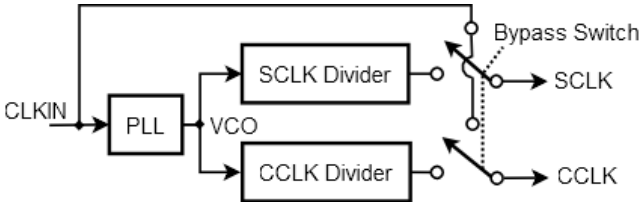

Figure 2. Bypass Switch for PLL

Transition Process

The process for each possible mode transition is listed in Table 2. The times needed for completing the transitions are also included.

In Table 2, each multi-state transition is presented as a shaded three-row group. The sequence of actions taken for every transition is given in the "Step" column along with its corresponding time in the "Time" column. Though the times are described in terms of the numbers of core clocks (CCLK), system clocks (SCLK), and input clocks (CLKIN), they can be easily converted to absolute time given the CLKIN frequency and SSEL/CSEL/MSEL/DF settings.

Please note that all the numbers given in Table 2 are close approximations, since clock synchronization may vary slightly.

PLL Frequency Change Process

The clocks of the processor, namely core clock (CCLK) and system clock (SCLK), can be changed by setting the SSEL/CSEL bit fields of the PLL divisor register (PLL_DIV) or by changing the PLL itself, which involves manipulating the MSEL and DF bit fields of PLL_CTL. If the PLL setting was changed, the procedure would be similar to the mode transition process discussed in the previous section. It includes writing to PLL_CTL, entering the idle state, and then waking up. The most common wakeup signal is the PLL wakeup, which means that the processor wakes up on the expiration of the internal PLL lock counter. The counter increments by one for each CLKIN clock after the IDLE state is entered. When it reaches the value set in the PLL lock count register (PLL_LOCKCNT), the wakeup occurs and the processor starts the execution of the instruction following IDLE.

In order to avoid glitches on CCLK and SCLK when changing the VCO frequency, the PLL is automatically bypassed before applying the new MSEL/DF settings, and pulled back after its output stabilizes. As a result, there are two periods of transition time for disabling and enabling bypass. Figure 3 is a recording of SCLK when MSEL is changed in Full On mode. T1 and T3 are the transition times dedicated to "Bypass Switch from PLL to CLKIN" and "Bypass Switch from CLKIN to PLL", respectively. T2 is the period for the internal PLL lock counter to expire. Its value (in units of CLKIN cycles) depends on the setting of PLL_LOCKCNT. After time T3, the processor resumes its normal operation of executing instructions. It may be noted that the frequency of SCLK is not uniform after T3. This is because PLL_LOCKCNT is set to a relatively small number (10) in this particular case, which is not long enough for the PLL to converge after its parameters (MSEL/DF) are changed. So, to ensure CCLK/SCLK have the desired frequency after the processor wakes up, PLL_LOCKCNT must be given a number large enough, such as the default value of 512, which allows the PLL to stabilize during the bypass period (T2).

As a result, the time for PLL frequency change is

$$T_1 + T_2 + T_3 = \frac{\sim 6 + PLL\_LOCKCNT}{CLKIN \text{ frequency}}.$$

While the processor core is idle in this transition process, the peripherals are still running at CLKIN for a period of T2. As a matter of fact, in T2, SCLK is the same as CLKIN, since the PLL is bypassed. So, it is safe to use either CLKIN or SCLK to describe T2.

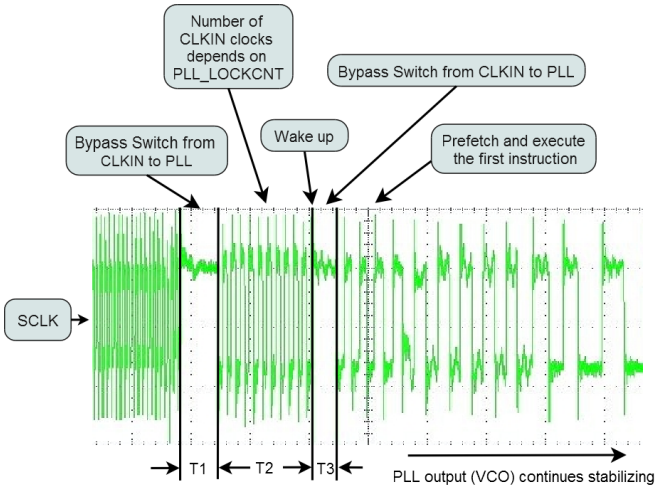

Figure 3. SCLK During PLL Frequency Change

Conclusion

Power can be saved if the processor is put into dormant states or lower frequency states when operations permit. Transitions between these power saving states take time though. In cases where the application has critical requirements for response times, the information provided by this application note can be used to optimize the power saving capability without compromising performance.

Transition	Step	Time
Full On→ Sleep	• IDLE state • Turn off CCLK	~ (4 SCLK + 3 CCLK)
Sleep	CCLK Off	See note
Sleep → Active	• Bypass Switch from PLL to CLKIN • Pre-fetch the first instruction	~ (4 CLKIN + 10 CCLK)
Full On→ Sleep	• IDLE state • Turn off CCLK	~ (4 SCLK + 3 CCLK)
Sleep	CCLK Off	See note
Sleep → Full On	Pre-fetch the first instruction	~10 CCLK
Active → Sleep	• IDLE state • Turn off CCLK	~ (4 SCLK + 3 CCLK)
Sleep	CCLK Off	See note
Sleep → Active	Pre-fetch the first instruction	~10 CCLK
Active → Sleep	• IDLE state • Turn off CCLK	~ (4 SCLK + 3 CCLK)
Sleep	CCLK Off	See note
Sleep → Full On	• Bypass Switch from CLKIN to PLL • Pre-fetch the first instruction	~ (2 CLKIN + 10 CCLK)
Full On → Deep Sleep	• IDLE state • Bypass Switch from PLL to CLKIN • Disable PLL • Turn off CCLK/SCLK	~ (5 SCLK + 3 CCLK + 4 CLKIN)
Deep Sleep	CCLK/SCLK Off	See note
Deep Sleep → Active	Pre-fetch the first instruction	~10 CCLK
Active → Deep Sleep	• IDLE state • Disable PLL • Turn off CCLK/SCLK	~ (5 SCLK + 3 CCLK)
Deep Sleep	CCLK/SCLK Off	See note
Deep Sleep → Active	Pre-fetch the first instruction	~10 CCLK
Full On/Active → Hibernate	• IDLE state • Disable on-chip core voltage regulator	~ (4 SCLK + 3 CCLK)
Hibernate	• CCLK/SCLK Off • Core Voltage Off	See note
Hibernate → Reset	Reset process	See [1]

Note: Depends on the wakeup signals.

Table 2. Mode Transition Procedure

References

[1] *ADSP-BF533 Blackfin Processor Hardware Reference.* Rev 3.1, May 2005. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – December 6, 2006 *by Jiang Wu*	Initial release.