ANALOG DEVICES

Estimating Power For The ADSP-TS101S

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Introduction

This EE note will discuss power consumption estimation based on characterized measurements for the ADSP-TS101S digital signal processor. The motivation for this document is to assist board designers by providing data as well as recommendations that will allow the designer to estimate their power budget for their power supply and thermal relief designs.

The ADSP-TS101S is an ultra-high-performance, static superscalar, 32-bit processor from the TigerSHARC® DSP family of Analog Devices. The DSP operates at a core clock frequency of 300 MHz with the core operating at 1.2V (V_{DD}) and the I/O operating at 3.3V (V_{DD_IO}). The data presented in this EE note is actual measured power consumption for silicon revision 0.2 of the ADSP-TS101S.

Power Consumption

Total power consumption has two components, one due to internal circuitry and one due to the switching of external output drivers. The following sections will show how to derive both of these power numbers.

Internal Power Consumption Estimation

The internal power consumption (on the V_{DD} supply) is dependent on the instruction execution sequence and the data operands involved. Analog Devices provides current consumption numbers for discrete activity levels. System application code can be mapped to these discrete numbers to estimate internal power consumption for an ADSP-TS101S processor for a given application.

Table 1 below shows the current consumption for the DSP at different levels of activity. From these internal activity levels (and from an understanding of the program flow using profiling or some other means), you can calculate a weighted-average of power consumption for each ADSP-TS101S processor in a system.

Parameter	Test Conditions	I_{DD} (A)
I_{DDMAX}	T_{CASE}=25C, V_{DD}=1.20V, @ 300 MHz	1.5460
I_{DDTYP}	T_{CASE}=25C, V_{DD}=1.20V, @ 300 MHz	1.5130
I_{DDCTRL}	T_{CASE}=25C, V_{DD}=1.20V, @ 300 MHz	0.8380
I_{DDDMA}	T_{CASE}=25C, V_{DD}=1.20V, @ 300 MHz	0.6835
I_{DDIDLE}	T_{CASE}=25C, V_{DD}=1.20V, @ 300 MHz	0.6650
$I_{DDIDLELP}$	T_{CASE}=25C, V_{DD}=1.20V, @ 300 MHz	0.1723

Table 1: Internal Power Vectors

Internal Power Vector Definitions

The following power vector definitions apply to the internal average power vectors shown above in Table 1:

- I_{DDMAX} --- V_{DD} supply current for maximum activity. Maximum activity is a SIMD quad 16-bit fixed-point

multiply and an add in parallel with two quad-word data fetches. The data fetched and operated on are random. This vector includes DMA activity as described below in the I_{DDDMA} definition.

- $\boldsymbol{I_{DDTYP}}$ --- V_{DD} supply current for typical activity. Typical activity is a SIMD quad 16-bit fixed-point compute operation in parallel with two quad-word data fetches. The data fetched and operated on are random. This vector includes DMA activity as described below in the I_{DDDMA} definition.

- $\boldsymbol{I_{DDCTRL}}$ --- V_{DD} supply current for control activity. Control activity is continuous decision-making and predicted branches. The branch prediction is deliberately set to be incorrect 50% of the time for equal distribution. This vector includes DMA activity as described below in the I_{DDDMA} definition.

- $\boldsymbol{I_{DDDMA}}$ --- V_{DD} supply current for DMA activity. DMA activity is a single external port DMA from external to internal memory, quad-word transfers of 32 words total. The DMA is chained to itself (in order to run continuously), and the DMA does not use interrupts. After setup, the core is not involved, executing the IDLE instruction only.

- $\boldsymbol{I_{DDIDLE}}$ --- V_{DD} supply current for idle activity. Idle activity is the core executing the IDLE instruction only with no DMA or interrupts.

- $\boldsymbol{I_{DDIDLELP}}$ --- V_{DD} supply current for idle low power. Idle Low Power activity is the core executing the IDLE(LP) instruction only with no DMA or interrupts.

The average current consumption for an ADSP-TS101S for a specific application is calculated according to the following formula, where "%" is the percentage of the overall time that the application spends in that state:

(% Maximum Activity Level x I_{DDMAX})
(% Typical Activity Level x I_{DDTYP})
(% Control Activity Level x I_{DDCTRL})
(% DMA Activity Level x I_{DDDMA})
(% Idle Activity Level x I_{DDIDLE})
+ (% Idle Low Power Activity Level x $I_{DDIDLELP}$)

= Total Current for V_{DD}
= I_{DD}

Equation 1: Internal Current (I_{DD}) Calculation

Therefore, the estimated average internal power consumption (P_{DD}) can be calculated as follows:

$$P_{DD} = I_{DD} \; x \; V_{DD}$$

Equation 2: Internal Power (P_{DD}) Estimation Calculation

For example, after profiling the application code the entire system activity is determined as follows:

- 30% Maximum Activity Level
- 30% Typical Activity Level
- 20% DMA Activity Level
- 20% Idle Activity Level

Example 1: Internal System Activity Level Example

From the percentages of this example, one can estimate a value for the current consumption of a single processor as follows:

(30% x 1.5460A)
(30% x 1.5130A)
(20% x 0.6835A)
+   (20% x 0.6650A)

= 1.1874A
= I_{DD}

Example 2: Internal Current Estimation Example

Therefore, the average internal power estimation for the processor can be calculated from example 2 above as follows:

P_{DD} = 1.1874A x 1.20V
= 1.43W

Example 3: Internal Power Estimation Example

External Power Consumption Estimation

The external power consumption (on V_{DD_IO}) is consumed by the switching of the output pins and is system dependent. For each unique group of pins, the magnitude of power consumed depends on the following:

- The number of output pins that switch during each cycle, O
- The load capacitance of the output pins, C
- Their voltage swing, V_{DD_IO}
- The maximum frequency at which the pins can switch, f

The load capacitance should include the input capacitance of each connected device as well as the DSP's own input capacitance (C_{IN}). For additional accuracy, trace capacitance should be included if possible. The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum frequency of ½ SCLK (50MHz).

Equation 3 below shows how to calculate the average external current (I_{DD_IO}) given the above parameters:

$$I_{DD\_IO} = O \text{ x } C \text{ x } V_{DD\_IO} \text{ x } f$$

Equation 3: External Current (I_{DD_IO}) Calculation

Therefore, the estimated average external power consumption (P_{DD_IO}) can be calculated as follows:

$$P_{DD\_IO} = I_{DD\_IO} \text{ x } V_{DD\_IO}$$

Equation 4: External Power (P_{DD_IO}) Calculation

For example, estimate P_{DD_IO} for the external port pins with the following assumptions:

- The example system consists of four ADSP-TS101S processors with one bank of shared external memory (64-bit), where $C_{IN} = 5pF$ per TigerSHARC DSP.
- Two 1M × 32 SDRAM chips are used, each with a load of 5 pF per pin (trace capacitance is neglected for this example).
- Continuous burst of quad-word (128-bit) writes occur every cycle at a rate of SCLK, with 50% of the data pins switching (this represents random data).
- The external address increments sequentially on a transaction boundary (every quad-word). For sequential addressing, the number of address bits switching per cycle approaches 2-bits.
- The control pins switch for refresh cycles and page boundary crossings.
- SCLK = 100Mhz (bus cycle time).

The I_{DD_IO} equation is calculated for each class of pins that can drive as shown in Table 2.

Pin Type	# of Pins	% Switching	x C	x V_{DD_IO}	x f	= I_{DD_IO}
Data	64	50	5pF + 4 x C_{IN}	3.3V	50 MHz	0.1320A
Addr	32	6.25	10pF + 4 x C_{IN}	3.3V	25 MHz	0.0049A
Ctrl	8	50	10pF + 4 x C_{IN}	3.3V	250 KHz	0.0001A

Table 2: External Current (I_{DD_IO}) Calculation Example

From the data tabulated in Table 2 above, the external average current consumed by the DSP can be calculated by summing all of the data from the right-most column:

$$I_{DD\_IO} = 0.1320A + 0.0049A + 0.0001A$$

Example 4: Total Average Estimated Current Calculation

Using the result from Example 4, the estimated average external power can be calculated as follows:

$$P_{DD\_IO} = 0.1370A \text{ x } 3.3V$$

Example 5: Total Average Estimated Power Calculation

Therefore, from this example system an estimated total of 0.4521W has been calculated as the average external power consumption for our system.

Power Supply Design

From the previous two sections we have shown how to estimate the average current and power consumption values for the internal and external power domains for a given system.

When designing a power supply, the designer must ensure that the power supply is capable of handling worst-case sustainable power consumption. Therefore, guard-banded values for the maximum internal (P_{DD}) and external (P_{DD_IO}) power requirements should be used.

This will ensure that the power supply design will provide sufficient voltage at a relatively high efficiency (typically greater than 90%) to each of the two voltage domains (V_{DD} and V_{DD_IO}) during sustained periods of maximum activity. This is due to the fact that the power required during a sustained maximum operating condition may be greater than what can be supplied by bypass and/or bulk capacitance.

For the core voltage (V_{DD}), the power supply design must be capable of supplying the maximum sustainable power consumption under worst-case conditions. This specific value is I_{DDMAX} (from Table 1), $V_{DD} = 1.26V$, 85°C, and 300 MHz (from the data sheet). For the I/O domain (V_{DD_IO}), the power supply design must be capable of supplying a guard-banded conservative power consumption estimate for I/O activity ($V_{DD\_IO} = 3.45V$, from the data sheet). This is to ensure sufficient overhead in the power supply design during sustained periods of high activity on the I/O domain.

Another critical specification when selecting a power supply (that can properly supply your system within normal operating specifications and at maximum efficiency) is the maximum *dI/dt* required by the processor. This number is simply the worst-case change in current required by the processor over a short time interval. This specification corresponds with the response time of your power supply.

We can calculate the value for *dI/dt max* as follows:

$$dI/dt_{MAX} \quad = (I_{DDMAX} - I_{DDIDLE}) / (8 \text{ x } t_{CCLK})$$
$$= (1.5460A - 0.6650A) / (8 \text{ x } 3.3ns)$$
$$= 33.371 \text{ A/}\mu s$$

Example 6: Maximum dI/dt Calculation

Where "t_{CCLK}" represents the core clock period of the DSP while operating at a frequency of 300 MHz, and the value "8" represents the minimum number of cycles to exit an "idle" instruction via an external interrupt, due to the length of the processor's instruction pipeline.

Thermal Relief Design

The overall system power estimation can also be used to estimate the requirements for a thermal relief design. Equation 5 below gives a value for the total average estimated power. Note that this equation yields total estimated average power consumption for a single ADSP-TS101S in a given system. Guard-banding this value is recommended for a thermal relief design that will allow the system to operate within specified thermal parameters.

$$P_{TOTAL} = V_{DD} \text{ x } I_{DD} + V_{DD\_IO} \text{ x } I_{DD\_IO}$$

Equation 5: Total Estimated Average Power

Note that guard-banded values taken at worst-case conditions ($V_{DD} = 1.26V$, $f = 300$ MHz, temp = 85°C), are used when considering a design for thermal relief.

Therefore, for the complete system example, (which is comprised of a cluster of four ADSP-TS101S processors and a shared bank of external memory comprised of two 1M x 32 SDRAM chips), we can estimate the total system power budget as follows:

$$P_{TOTAL} = P_{DD} \text{ (average)} + P_{DD\_IO} \text{ (average)}$$

Equation 6: Total System Power Calculation

Compensation Curves

The following section of this EE note shows I_{DDMAX} compensation curves versus the minimum and maximum allowable values for processor core voltage, operating frequency, and operating temperature. These curves can be used to extrapolate data (from Table 1) to estimate more precise values for a system, depending upon the specific operational parameters of the system.

Figure 1 shows a graph for the maximum internal current (I_{DDMAX}) versus V_{DD} operating range tolerances. The data for this graph was obtained while operating the processor at its maximum operating frequency and at nominal operating temperature, 300 MHz and 25°C, respectively.
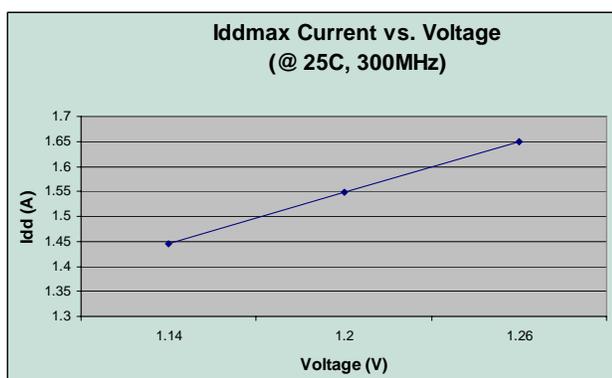
Iddmax Current vs. Temperature (@ 1.20V, 300MHz)

Figure 2: I_{DDMAX} Current vs. Temperature

Figure 3 shows a graph for the maximum internal current (I_{DDMAX}) versus the specified operating frequency range. The data for this graph was obtained while operating the processor at its nominal temperature and voltage, 25°C and 1.20V, respectively.

Iddmax Current vs. Voltage (@ 25C, 300MHz)

Figure 1: I_{DDMAX} Current vs. Voltage

Figure 2 shows a graph for the maximum internal current (I_{DDMAX}) versus the specified temperature operating range. The data for this graph was obtained while operating the processor at its maximum operating frequency and at nominal V_{DD}, 300 MHz and 1.20V, respectively.
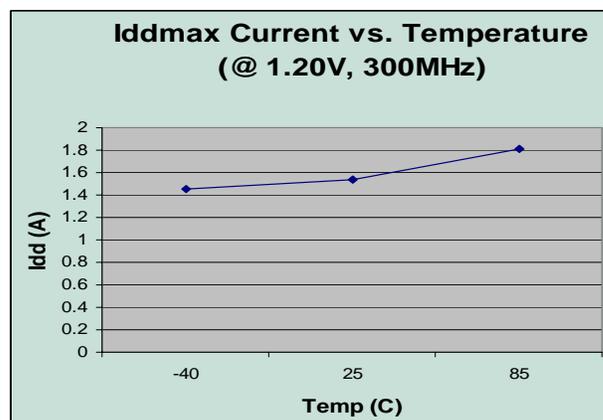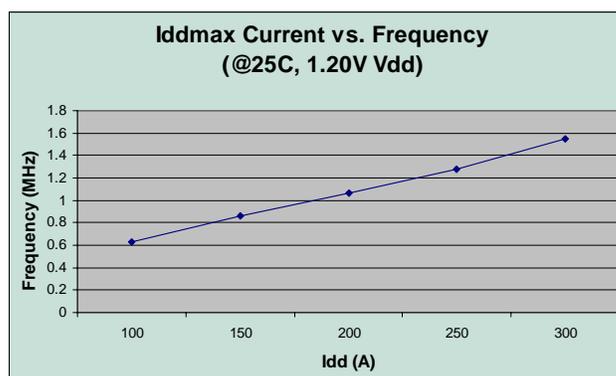
Iddmax Current vs. Frequency (@25C, 1.20V Vdd)

Figure 3: I_{DDMAX} Current vs. Frequency

Document History

Version	Description
Feb 24, 2003 by Greg F.	Updated Data For 300MHz Upgrade
Sep 23, 2002 by Greg F.	Initial Release