AN-1535
APPLICATION NOTE

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ADuM4135 Gate Driver Performance Driving SiC Power Switches

by Hans Brueggemann

INTRODUCTION

In solar photovoltaics (PV) and energy storage applications, there is a trend towards increased power density along with the ever present need of improved efficiency. A solution to this problem comes in the form of silicon carbide (SiC) power devices.

SiC devices are wide band-gap devices that can operate at an increased voltage of >120 V dc and tend to have a low drain source impedance (R_{DSON}). With some devices having an R_{DSON} as low as 8 mΩ, these devices also fill the need for reduced conduction losses and therefore increased efficiency. SiC devices can also exhibit fast switching speeds of >100 kHz with low parasitic capacitance and associated charge during switching. However, disadvantages include a requirement for higher common-mode transient immunity (CMTI) greater than 100 kV/µs required for gate drivers. Another disadvantage is that higher switching across the drain source of the SiC can lead to ringing at the gate of the device. These disadvantages can cause problems when driving higher voltage SiC devices, where significant power density improvement can be achieved by their implementation.

One combination of gate driver and SiC that can solve these problems is the ADuM4135 and the SiC module, as specified in Table 1. The power module is a half bridge SiC device with a 1200 V collector emitter voltage rating and a continuous current capability of 75 A. Its gate source voltage (V_{GS}) rating is +20 V to −10 V. It has an isolation rating of 2.5 kV for 1 min. The input capacitance (C_{ISS}) of the modules is 4.2 nF, with a reverse recovery time of 25 ns.

The ADuM4135 gate driver is a single-channel device with a typical drive capability of 7 A source/sink at a 25 V operating voltage (V_{DD} to V_{SS}). It has a minimum CMTI of 100 kV/µs.

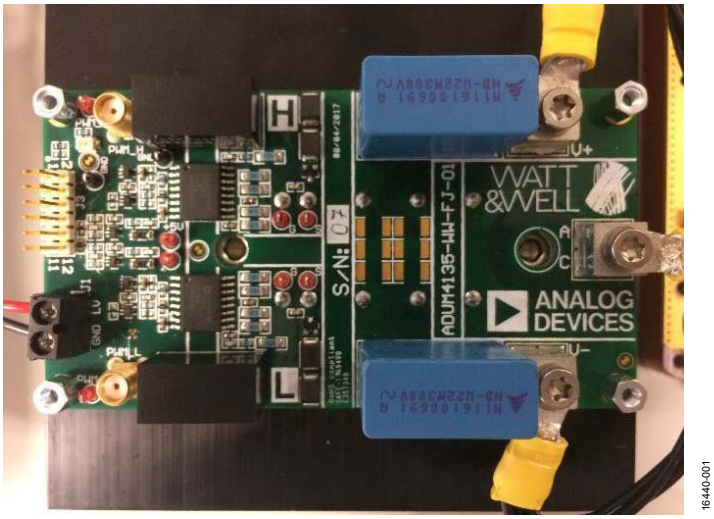

Figure 1. ADuM4135 Gate Drive Module

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REVISION HISTORY

1/2018—Revision 0: Initial Version

EXPERIMENTAL SETUP

MEASURING GATE DRIVE SIGNALS

For high voltage measurement, differential probes are typically used to isolate the user from the high voltage measurement. However, these probes tend to be noisier than standard passive probes and can distort the measurements. Figure 2 shows the difference between the isolated probe and the passive probe when measuring at the same point. For these measurements, the high-side measurement is achieved by isolated probes where there is a need for isolation to higher voltages. However, for the low-side measurement, a standard passive probe is used to obtain a more accurate representation of the signals present. Figure 3 shows how this measurement is achieved, and Figure 2 shows the corresponding result. The signals are as follows:

- V_{GS} is the voltage measured directly at the gate source pins of the power device.
- V_{DS} is the voltage measured at the drain source of the power device.

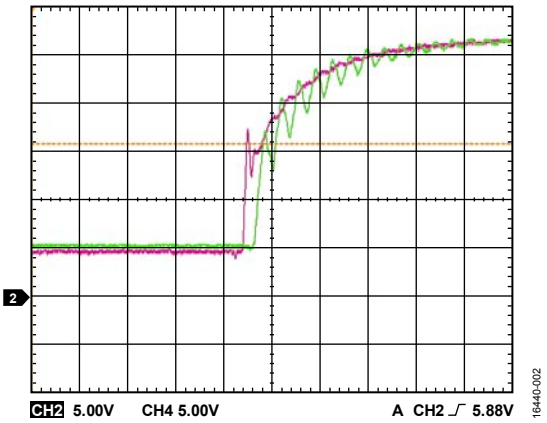

Figure 2. V_{GS} Measurement Using Differential Probe and Passive Probe: Red is Low-Side V_{GS} Measured with Agilent N2863B Passive Probe, 300 MHz; Green is Low-Side V_{GS} Measured with TESTEC TT-SI9110 Differential Probe, 100 MHz

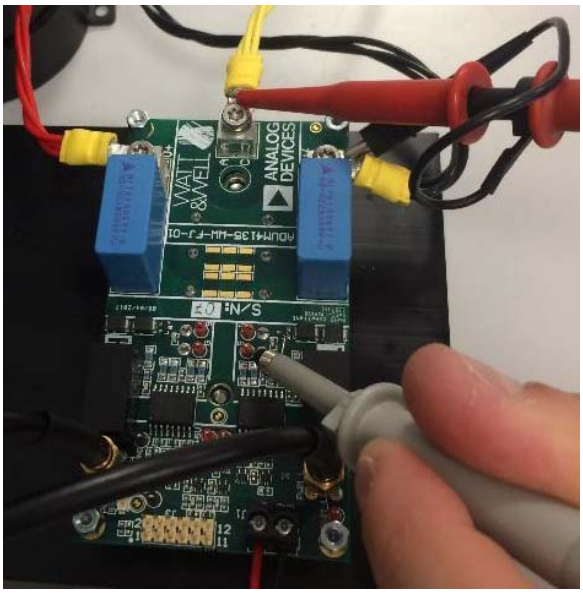

Figure 3. How to Measure Low-Side V_{GS} and V_{DS}

GATE VOLTAGE CONTROL

At the beginning of the tests, it was observed that the gate to source voltage had a sharp rise time, which can cause issues because it creates a restrictive electromagnetic interference (EMI) environment. Therefore, it was decided to soften the switching by adding a 4.7 nF capacitor on the gate. This capacitor was added directly at the pins of the module between gate and source. Figure 4 and Figure 5 show the V_{GS} gate drive signal prior to adding the capacitor; a sharp slew rate is shown. Figure 5 is a zoomed in view of Figure 4. Figure 6 shows the response with the capacitor added at the gate, where a more controlled rise time is shown at the V_{GS}.

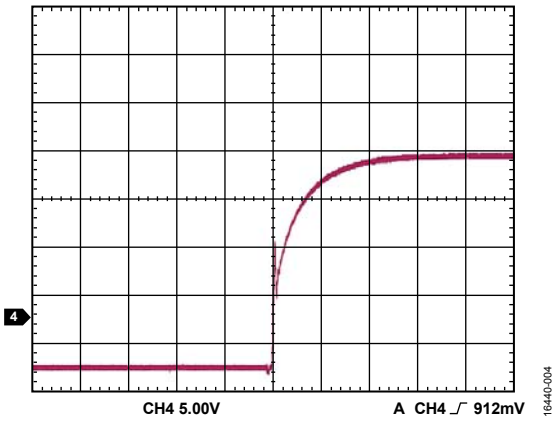

Figure 4. Low-Side V_{GS} Without Additional Capacitor on the Gate

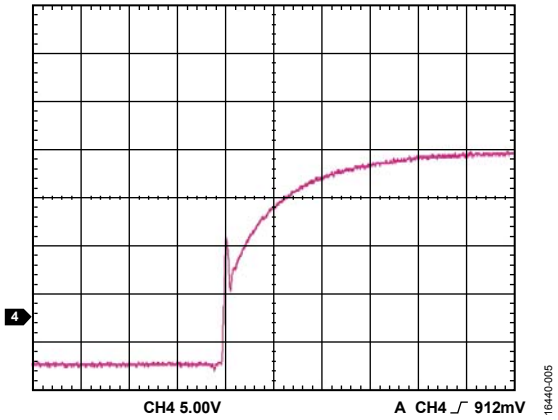

Figure 5. Zoomed Low-Side V_{GS} Without Additional Capacitor on the Gate

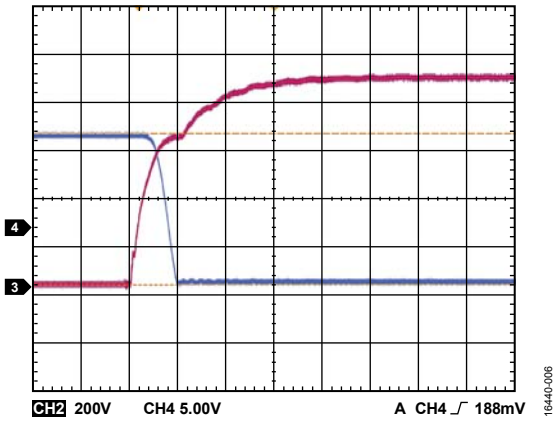

Figure 6. Low-Side V_{GS} with 4.7 nF Additional Capacitor on the Gate

DECOUPLING THE DC LINK

Initially, a 10% to 20% ripple was observed on the dc bus on the dc input voltage when switching. This ripple is shown in Figure 7. To reduce this ripple, extra capacitance to a total of 1100 µF was added to improve the decoupling on the dc bus.

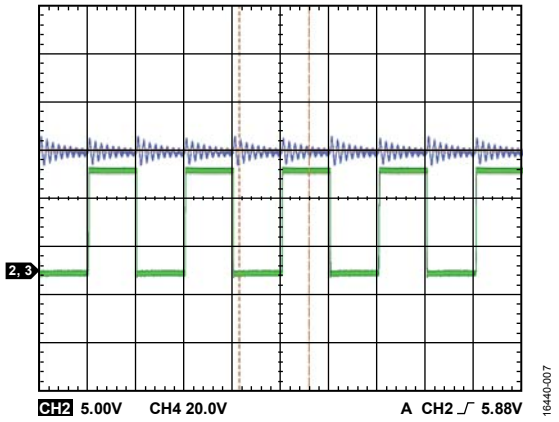

Figure 7. DC Input Voltage Without Decoupling Capacitors

TEST SETUP

ELECTRICAL SETUP

The setup of the system test circuit is shown in Figure 8. A dc voltage is applied to the inputs, which is across the full half bridge, where decoupling capacitors of 1100 µF are added to the input stage. The output stage is an inductor capacitor (LC) filter stage of 200 µH and 128 µF, filtering the output into the load, R1, of 2 Ω to 3 Ω. Table 1 shows a list of the test setup power components. A complete setup is shown in Figure 9, and Table 2 shows the full list of equipment used in the test.

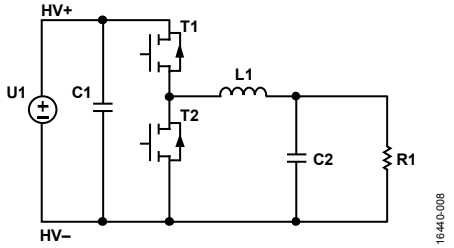

Figure 8. Electrical Setup

Table 1. Test Setup Power Components

Equipment	Value
U1	200 V to 900 V
C1	1100 µF
L1	200 µH
C2	128 µF
R1	2 Ω to 3 Ω

Table 2. Complete Setup Equipment

Equipment	Manufacturer	Type
Oscilloscope	Agilent	DSO-X 3034
DC Supply	Delta Elektronika	SN660-AR-11 (two in serial)
Gate Driver Board	Watt&Well	ADUM4135-WW-FJ-01 SN07
Waveform Generator	Agilent	33522A
Current Probe	Hioki	3275
Passive Voltage Probe	Agilent	N2863B 300MHz
Passive High Voltage Probe	Elditest	GE3421 100MHz

Figure 9. Physical Setup

TEST RESULTS

NO LOAD TESTING

The ADuM4135 is in its first revision released (AA). One change was made: a capacitor of 4.7 nF was added on the gates of the power metal-oxide semiconductor field effect transistors (MOSFETs), Q1 and Q2. Table 3 and Table 4 are a summary of the results observed, and Figure 10 through Figure 15 show the proof of results. Test 1 and Test 3 were carried out at 600 V and 900 V, respectively, at a 50 kHz switching frequency, whereas Test 2 was carried out at 600 V at a switching frequency of 100 kHz.

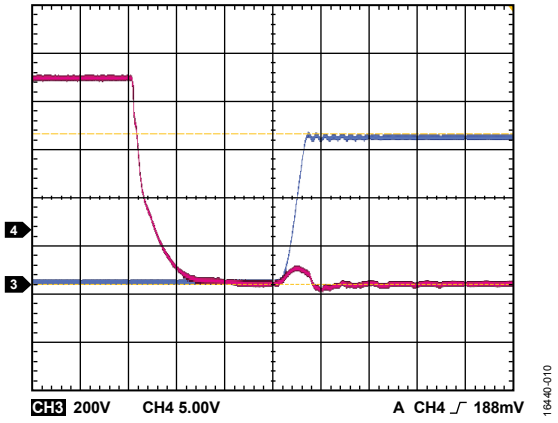

Figure 10. DC Voltage (V_{DC}) = 600 V, f_{SW} = 50 kHz, No Load; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}

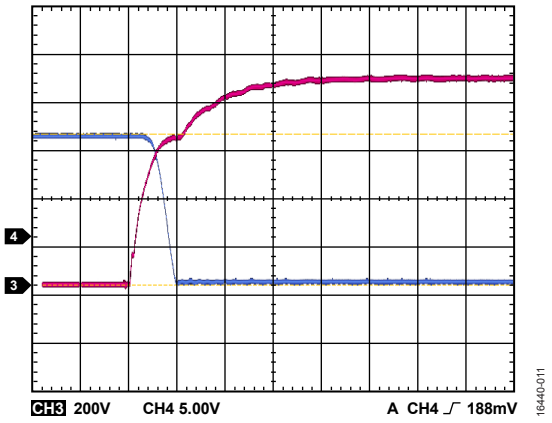

Figure 11. V_{DC} = 600 V, f_{SW} = 50 kHz, No Load; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}

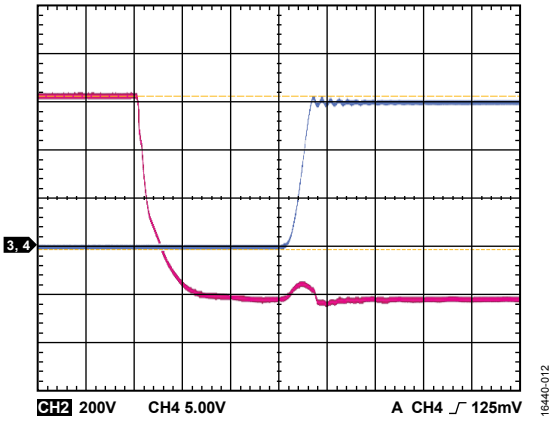

Figure 12. V_{DC} = 600 V, f_{SW} = 100 kHz, No Load; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}

Table 3. No Load Testing—Figure Assignments

Test	V_{DC} (V)	Switching Frequency, f_{SW} (kHz)	Duty Cycle (%)	DC Loss (W)	Figures
1	600	50	50	30	Figure 10 and Figure 11
2	600	100	50	66	Figure 12 and Figure 13
3	900	50	50	63	Figure 14 and Figure 15

Table 4. No Load Testing—Temperature Summary

Test	V_{DC} (V)	f_{SW} (kHz)	Ambient Temperature (°C)	Heatsink Temperature (°C)	DC-to-DC Power Supply Temperature, High-Side (°C)	DC-to-DC Power Supply Temperature, Low-Side (°C)	Gate Driver Temperature, High-Side (°C)	Gate Driver Temperature, Low-Side (°C)
1	600	50	30	57	57	58	57	58
2	600	100	30	67	60	61	65	66
3	900	50	30	70	61	61	65	65

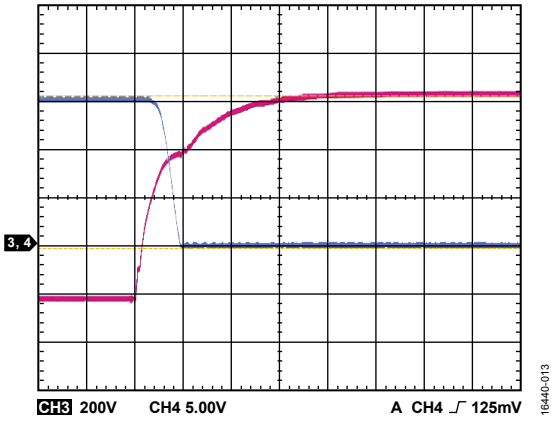

Figure 13. V_{DC} = 600 V, f_{SW} = 100 kHz, No Load; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}

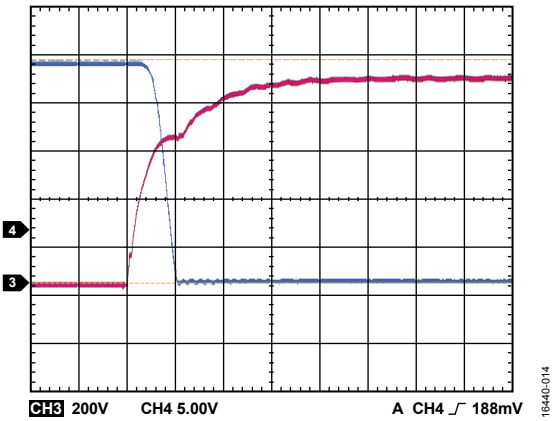

Figure 14. V_{DC} = 900 V, f_{SW} = 50 kHz, No Load; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}

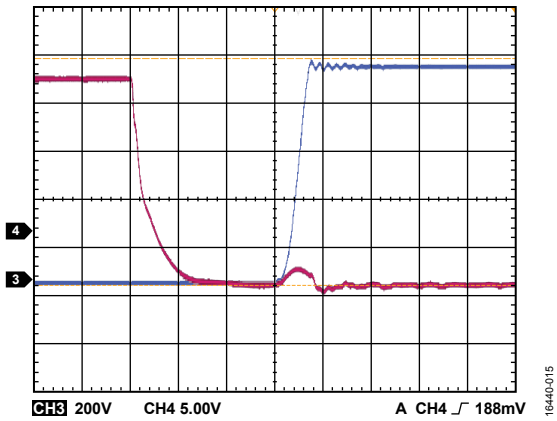

Figure 15. V_{DC} = 900 V, f_{SW} = 50 kHz, No Load; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}

LOAD TESTING

The ADuM4135 is in its first revision released (AA). One change was made: a capacitor of 4.7 nF was added on the gates of the power MOSFETs, Q1 and Q2. Similar to the test setup of the no load tests in the previous section, Table 5 is a summary of the results observed, and Figure 16 through Figure 27 show the proof of results. Test 4, Test 5, and Test 6 were carried out at 200 V at a 50 kHz switching frequency with a 25% duty cycle, whereas Test 7 was carried out at 600 V at a 50 kHz switching frequency with a 25% duty cycle. Test 8 and Test 9 were carried out at 900 V at 50 kHz and 100 kHz switching frequencies, respectively.

The output current (I_{OUT}) was measured at the output of R1, the output load resistor, whereas the output voltage (V_{OUT}) was measured as the voltage across R1. The test results show some Miller feedback on V_{GS}, but V_{GS} remains at the −4 V level at the gate of the SiC. At 900 V, some ringing is seen on V_{DS}, but it is <30 V of the input dc voltage. This design shows how the ADuM4135 can drive SiC MOSFETs with good performance.

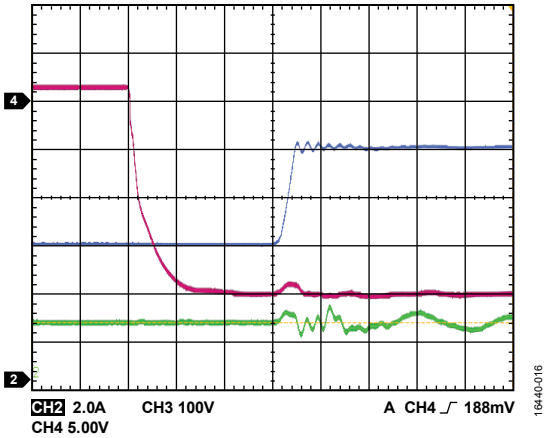

Figure 16. V_{DC} = 200 V, f_{SW} = 50 kHz, Output Power (P_{OUT}) = 100 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

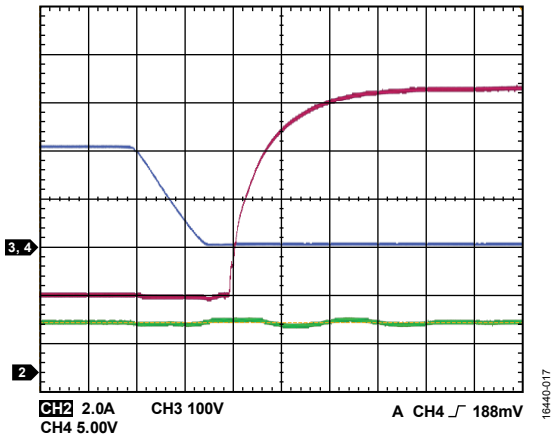

Figure 17. V_{DC} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 100 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

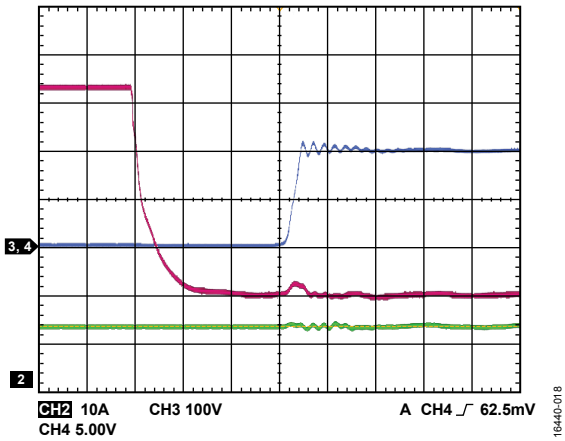

Figure 18. V_{DC} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 460 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

Table 5. Load Testing

Test	V_{DC} (V)	f_{SW} (kHz)	Duty Cycle (%)	I_{OUT}[1] (A)	V_{OUT}[2] (V)	P_{OUT}[3] (W)	I_{IN}[4] (A)	Figures
4	200	50	25	2	48	96	0.59	Figure 16 and Figure 17
5	200	50	25	10	46	460	2.39	Figure 18 and Figure 19
6	200	50	25	13.3	45	600	3.16	Figure 20 and Figure 21
7	600	50	25	10	140	1400	2.42	Figure 22 and Figure 23
8	900	50	25	10	204	2040	2.43	Figure 24 and Figure 25
9	900	100	25	10	188	1880	2.52	Figure 26 and Figure 27

[1] I_{OUT} is the output current in Load Resistor R1.
[2] V_{OUT} is the output voltage across R1.
[3] P_{OUT} is the output power ($I_{OUT} \times V_{OUT}$).
[4] I_{IN} is the input current through U1.

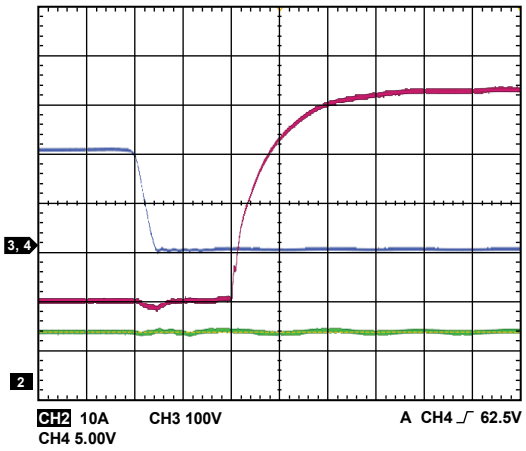

Figure 19. V_{DC} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 460 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

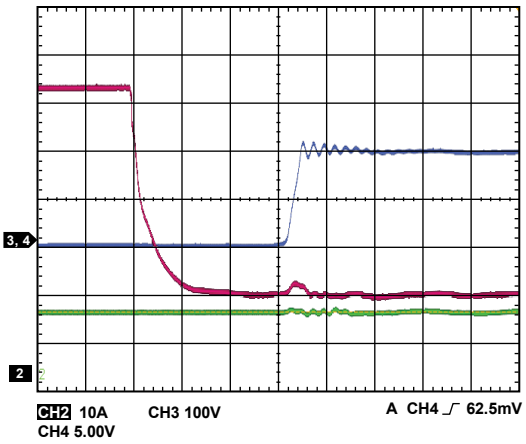

Figure 20. V_{DC} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 600 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

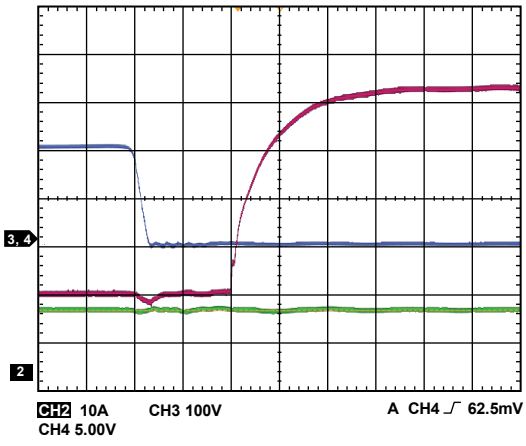

Figure 21. V_{DC} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 600 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

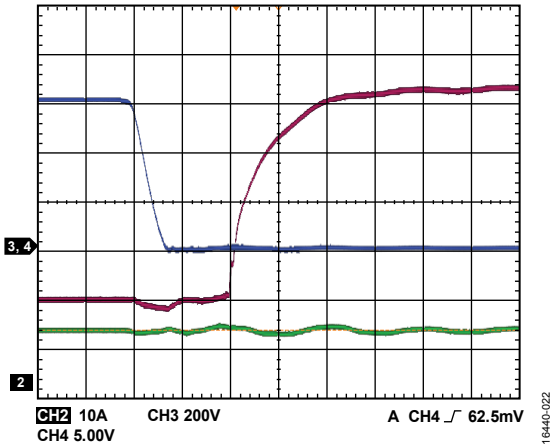

Figure 22. V_{DC} = 600 V, f_{SW} = 50 kHz, P_{OUT} = 1400 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

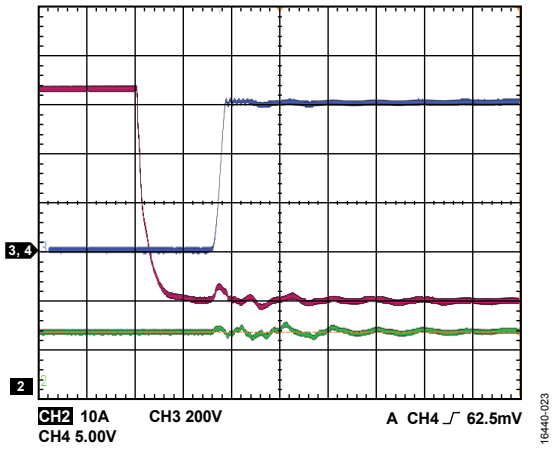

Figure 23. V_{DC} = 600 V, f_{SW} = 50 kHz, P_{OUT} = 1400 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

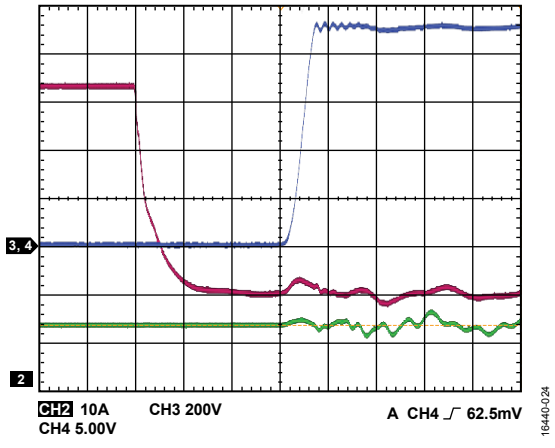

Figure 24. V_{DC} = 900 V, f_{SW} = 50 kHz, P_{OUT} = 2040 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

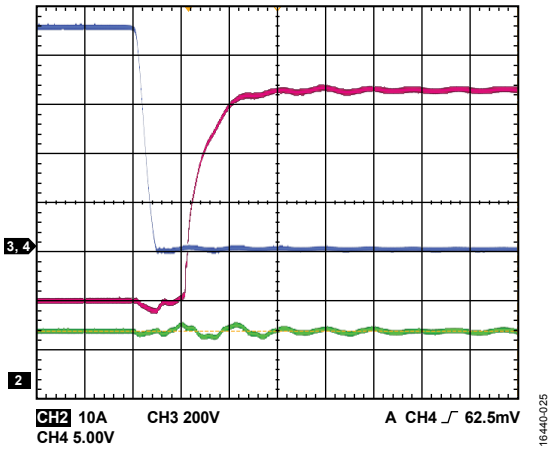

Figure 25. V_{DC} = 900 V, f_{SW} = 50 kHz, P_{OUT} = 2040 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

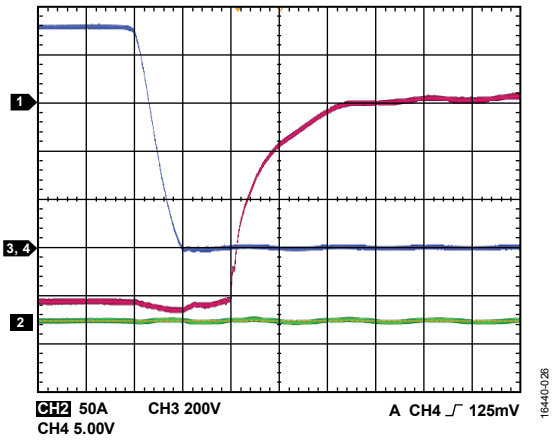

Figure 26. V_{DC} = 900 V, f_{SW} = 100 kHz, P_{OUT} = 1880 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

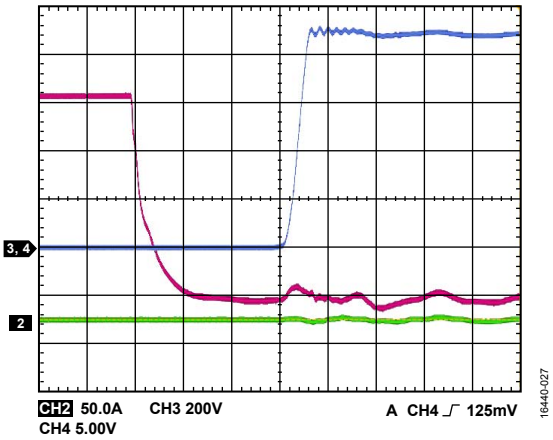

Figure 27. V_{DC} = 900 V, f_{SW} = 100 kHz, P_{OUT} = 1880 W; Red is Low-Side V_{GS}; Blue is Low-Side V_{DS}; Green is Output Current

SCHEMATIC

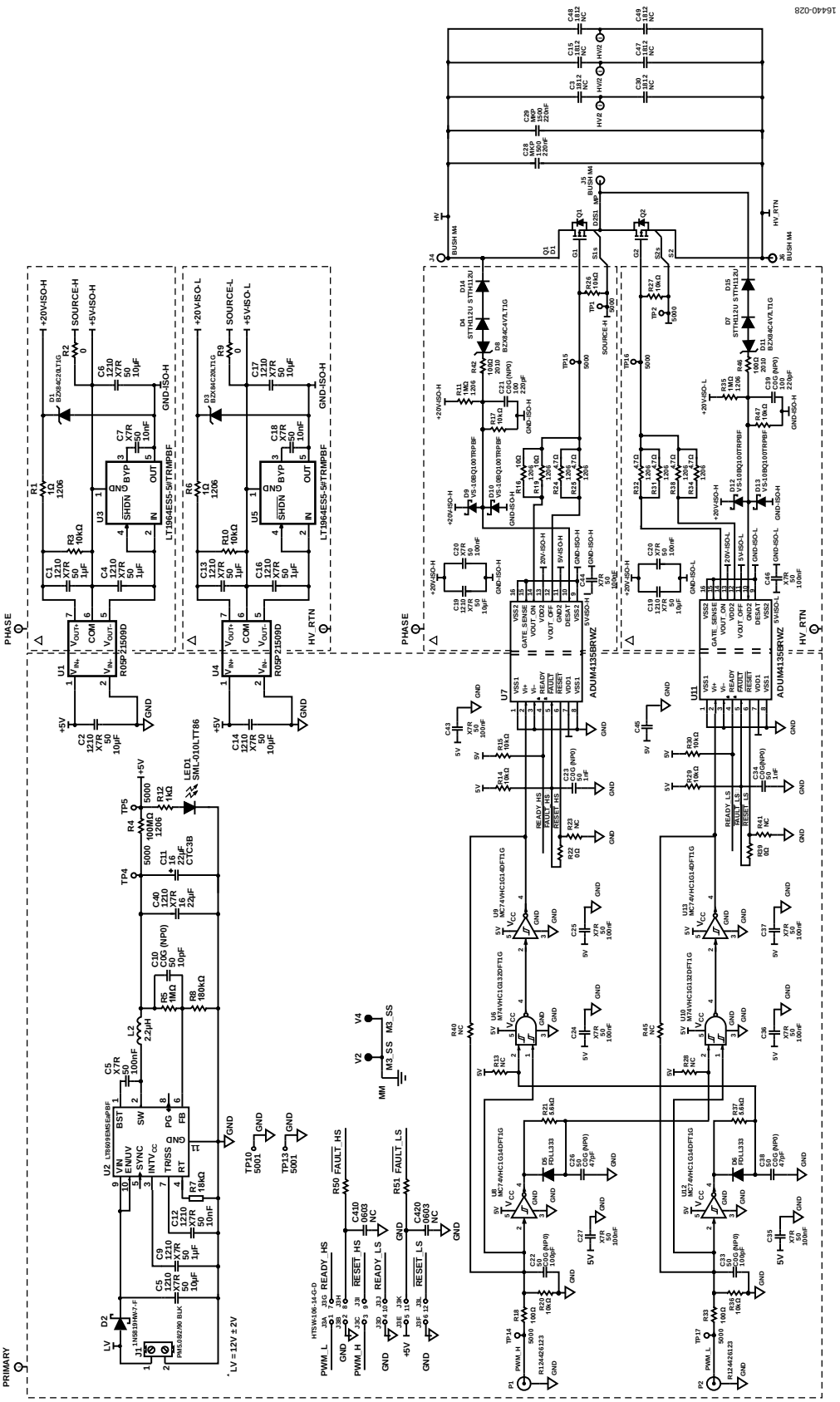

Figure 28. ADuM4135 Gate Drive Board Schematic

CONCLUSION

The ADuM4135 gate driver has the current drive capability, the correct power supply range (30 V maximum), and a strong CMTI capability of 100 kV/µs to deliver good performance when driving SiC MOSFETs.

The test results provide data showing a solution is available on the market for isolated power supply, high voltage gate drivers driving SiC.