AN-1349
APPLICATION NOTE

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PCB Implementation Guidelines to Minimize Radiated Emissions on the ADM2582E/ADM2587E RS-485/RS-422 Transceivers

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INTRODUCTION

The ADM2582E/ADM2587E are fully integrated, signal and power isolated, RS-485/RS-422 transceivers. Signal isolation is implemented with Analog Devices, Inc., *i*Coupler® digital isolation technology. The ADM2582E/ADM2587E also include an integrated, high voltage, isolated, dc-to-dc power supply that is implemented using Analog Devices *iso*Power® technology, which eliminates the need for an external dc-to-dc isolation block. A key component of any isolated power supply is the power transformer. The *iso*Power integrated transformer operates at switching frequencies in the 180 MHz to 400 MHz range. Isolation is implemented on the printed circuit board (PCB) with split reference planes separated by a physical isolation gap. Because of the isolation gap on the PCB layout, unwanted current loops may radiate. Adhering to some basic electromagnetic (EM) suppression guidelines and concepts during PCB layout mitigates radiated emissions.

In industrial and instrumentation applications, several standards for radiated emissions exist. With good PCB design and layout choices, the ADM2582E/ADM2587E devices can easily meet EN55022/CISPR22 Class A (FCC Class A) emissions standards commonly used in industrial environments. With care, these products can also meet EN55022/CISPR22 Class B (FCC Class B) standards in an unshielded environment.

This application note examines specific layout options and component selection to achieve these standards for radiated emissions. Also provided in this application note are specific PCB layout details with measured results in a fully certified, semianechoic, 10 m chamber that achieved both EN55022/CISPR22 Class A (FCC Class A) and EN55022/CISPR22 Class B (FCC Class B) emissions.

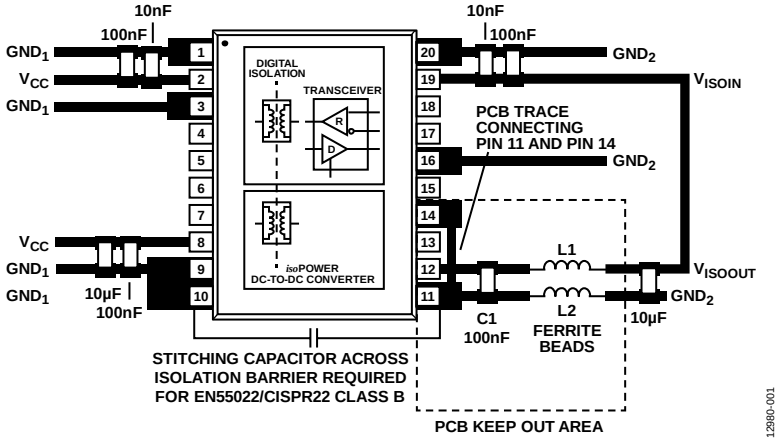

Figure 1. Recommended PCB Layout and Component Placement to Minimize Radiated Emissions

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6/2015—Revision 0: Initial Version

RECOMMENDATIONS

SUMMARY OF PCB RECOMMENDATIONS

To achieve EN55022/CISPR22 Class A (FCC Class A) classification, the following guidelines are recommended:

- Ensure that there is good decoupling on the PCB (follow recommended decoupling per the ADM2582E/ ADM2587E data sheet).
- Place a ferrite bead between the PCB trace connections and the following IC pins: V_{ISOOUT} (Pin 12) and GND_2 (Pin 11 and Pin 14).
- Do not connect the V_{ISOOUT} pin to a power plane; connect V_{ISOOUT} to V_{ISOIN} using a PCB trace. Ensure V_{ISOIN} (Pin 19) is connected through the ferrite to V_{ISOOUT} (Pin 12) as shown in Figure 1.
- Ensure GND_2 (Pin 16 and Pin 20) is connected to GND_2 (Pin 11) on the outside (bus side) of the L2 ferrite as shown in Figure 1.
- Ensure that there is a keep out area for the GND_2 plane in the PCB layout around the L1 and L2 ferrites. The keep out area means there must not be a GND_2 fill or any metal fill on any layer underneath the ferrites. The reason for this is to minimize the parasitic capacitance effects between the PCB traces and layers of the PCB because this reduces the filtering benefits of the ferrites.

For applications that are required to meet the more stringent EN55022/CISPR22 Class B (FCC Class B) emission standards, the previously listed recommendations must be implemented with an additional suppression technique of stitching capacitance across the isolation barrier. Either of the following two methods can be used to create a stitching capacitor by connecting:

- An embedded stitching capacitor between any GND_1 pin and GND_2 pins (Pin 11 and Pin 14) using internal layers of the PCB planes. Do not connect the stitching capacitor to the GND_2 pins (Pin 16 and Pin 20).
- A high voltage discrete capacitor connected between the GND_1 pins (Pin 9 and Pin 10) and GND_2 pins (Pin 11 and Pin 14).

EMISSION SUPPRESSION RECOMMENDATIONS

It is important to adhere to some basic guidelines during PCB design/layout to mitigate radiated emissions. Electromagnetic radiation occurs when large currents are switched in a short time, resulting in large di/dt noise. The level of the radiated emission is dependent on the loop area of the current path, because a large current loop area results in a higher emitted radiation. These guidelines control radiated emissions at the source and minimize the loop area of the current path.

Emission levels from *iso*Power technology can be reduced below Class A limits by

- Good decoupling of the V_{CC} supply.
- Increasing the impedance between specific IC pins and PCB traces.
- Connecting V_{ISOOUT} to V_{ISOIN} with a PCB trace (no plane connection).

To achieve EN55022/CISPR22 Class B (FCC Class B) classification, an additional suppression method is required. Reduce the impedance to high frequency currents across the isolation barrier between GND_1 and GND_2.

To allow additional margin for passing emission limits, the GND_2 plane area must be minimized.

Control of emissions from power/signal cables and chassis shielding techniques are outside the scope of this application note.

PCB GUIDELINES

V_{CC} DECOUPLING

Decoupling capacitors have two primary functions.

- Decoupling capacitors are used as charge storage devices. When an IC switches states and requires additional current, the local decoupling capacitor provides this current through a low inductance path.
- Decoupling capacitors reduce the noise injected into PCB planes, which suppresses high frequency noise in the system. A source of the injected noise can occur when the voltage supply at the V_{CC} pin is temporarily lowered until the adequate current is supplied.

In the ADM2582E/ADM2587E, the *iso*Power technology switches large currents in the 100s of mA range at frequencies of 180 MHz and 400 MHz. The 10 µF capacitor on the V_{CC} pin (Pin 8) provides a large charge reserve locally on the PCB. It is important that these capacitors have a very low equivalent series resistance (ESR) and low equivalent series inductance (ESL) at 180 MHz and 400 MHz.

When the decoupling between the V_{CC} and GND_1 pins is inadequate, these high frequency switching currents are not provided locally from the capacitors but from the power delivery system to the PCB. If the power delivery system used to power the ADM2582E/ADM2587E is not in close proximity to the IC, this results in an increase in the loop area in which the high frequency current flows. An increase in the loop area results in an increase in the emissions levels.

From a PCB layout point of view, it is very important to

- Locate the decoupling capacitors as close as possible to the power and GND_X pins to minimize the inductance and the current loop area size.
- Minimize the impedance path between the V_{CC} power pins and the V_{CC} power plane of the PCB.
- Minimize the impedance path between the IC GND_1 pins and the GND_1 plane of the PCB.

INCREASE IMPEDANCE BETWEEN SPECIFIC IC PINS AND PCB TRACE CONNECTIONS

Increasing the impedance to high frequency currents between specific IC pins and PCB trace connections minimizes the level of electromagnetic radiation. This method of EM suppression controls the radiating signal at its source and minimizes the loop area, which is achieved by placing surface-mount ferrites in series with V_{ISOOUT} (Pin 12) and GND_2 (Pin 11 and Pin 14), as shown in Figure 2. The impedance of the ferrite is chosen to be greater than 2 kΩ between the 100 MHz and 1 GHz frequency range, as shown in Figure 3, where Z is the impedance, R is the resistance, and X is the reactance of the bead. Measured data was gathered using the ferrites shown in Table 1.

Table 1. Example Ferrites

Manufacturer	Device No.
Taiyo Yuden	BKH1005LM182-T
Murata Electronics	BLM15HD182SN1

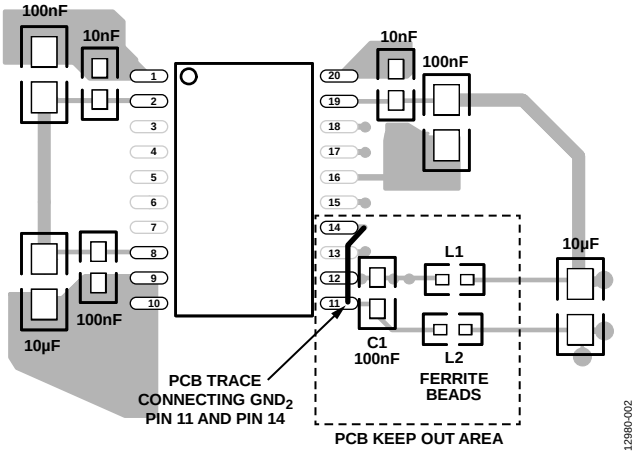

Figure 2. Recommended Component Placement

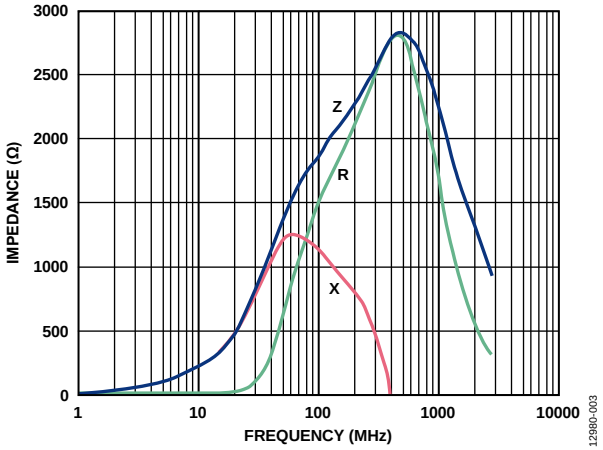

Figure 3. Recommended Ferrite Impedance Plot

REDUCE IMPEDANCE TO HIGH FREQUENCY CURRENTS ACROSS THE ISOLATION BARRIER BETWEEN GND_1 AND GND_2

To achieve EN55022/CISPR22 Class B (FCC Class B) classification, a suppression technique of stitching capacitance across the isolation barrier is required to reduce the emission levels further.

Due to the formation of an isolation gap on the PCB, unwanted ground current loops can result in an increase in radiated emissions. To create the isolated power supply, a transformer switches currents across the isolation barrier. In an ideal operation, only the transformer driver differential currents on the primary side are magnetically coupled across the isolation barrier. However, an inherent issue of a transformer is that parasitic currents are also capacitively coupled across the isolation barrier, as shown in Figure 4. When on the secondary side, these parasitic currents seek a return path back to the source on the primary side. There is no physical connection available for these currents to cross the isolation gap. These high frequency currents become common-mode currents on the secondary side on the V_{ISOOUT} and GND_2 pins. The inability of these high frequency currents to return across the isolation barrier results in the radiated emissions.

Analyzing the current flow in Figure 4, the lack of a physical return path from the secondary side back to the primary side due to the isolation barrier creates a dipole antenna, which can radiate. By providing a low impedance return path for the high frequency common-mode currents, the dipole emission level is reduced.

The stitching capacitor across the isolation barrier provides a low impedance return path necessary for high frequency common-mode currents, while still preserving the required high voltage isolation of the system.

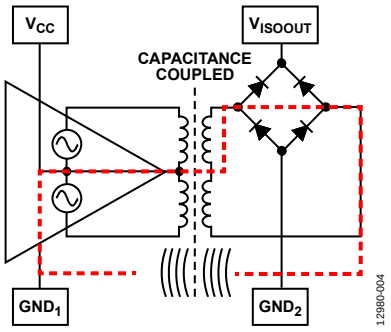

Figure 4. Current Loops Across the Isolation Barrier Implementation of the Stitching Capacitor

IMPLEMENTATION OF THE STITCHING CAPACITOR

The following methods can be used to implement the stitching capacitor that spans across isolation clearance on the PCB:

- High voltage, safety rated discrete capacitor
- Embedded PCB stitching capacitance

HIGH VOLTAGE, SAFETY RATED DISCRETE CAPACITOR

A stitching capacitance can be implemented with a ceramic capacitor across the isolation barrier.

It is recommended to use a surface-mount high voltage capacitor body, if possible, due to the small lead inductance of surface-mount components compared to discrete through hole capacitors. A discrete high voltage capacitor has been used to achieve EN55022B for the ADM2587E when powered at 3.3 V and 5.0 V and for the ADM2582E when powered by 5.0 V.

When completing the PCB design, adhere to the PCB layout shown in Figure 5.

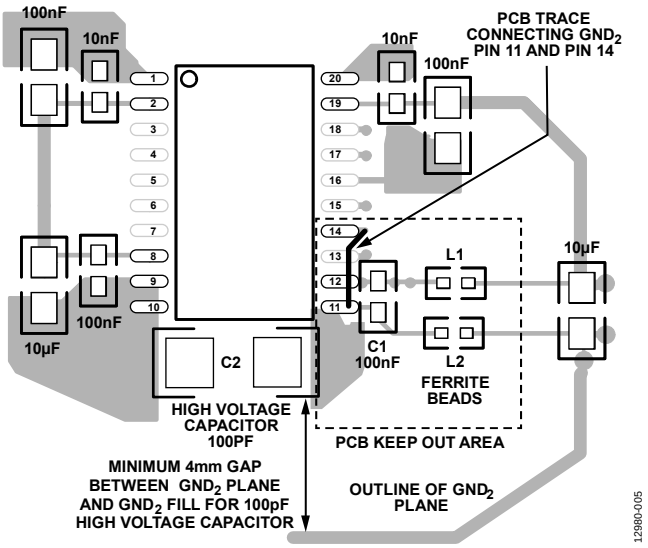

Figure 5. High Voltage Discrete Stitching Capacitor Placement Required for EN55022 Class B Classification

- Ensure GND_2 (Pin 14) is connected to GND_2 (Pin 11) on the inside (device side) of the C1 100 nF capacitor.
- Ensure the C1 capacitor is connected between V_{ISOOUT} (Pin 12) and GND_2 (Pin 11) on the device side of the L2 and L3 ferrites.
- Ensure GND_2 (Pin 16) is connected to GND_2 (Pin 11) on the outside (bus side) of the L2 ferrite as shown in Figure 5.
- Ensure that there is a keep out area for the GND_2 plane in the PCB layout around the L1 and L2 ferrites. The keep out area means there must not be a GND_2 fill on any layer underneath the L1 and L2 ferrites.
- Ensure there is a minimum separation gap of 4 mm between the GND_2 plane fill and the GND_2 fill for the C2 high voltage discrete capacitor pad.

Capacitors with guaranteed creepage, clearance, and the ability to withstand voltage can be obtained from many mainstream capacitor manufacturers (as shown in Table 2).

Table 2. Example Discrete High Voltage Capacitor

Parameter	Value
Manufacturer	TDK Corporation
Device Number	C4532C0G3F101K160KA
Description	Capacitor, ceramic, 100 pF, 3 kV
Body Size	1812

EMBEDDED PCB STITCHING CAPACITANCE

On a multilayer PCB, the PCB layers can be used to create an embedded stitching capacitor structure. An embedded PCB capacitor is created when two metal planes in a PCB overlap each other and are separated by dielectric material. An embedded stitching capacitor is formed by extending the internal reference planes from the primary and secondary layers across the area that is used for creepage on the PCB surface. By overlapping the internal layers across the isolation barrier, a capacitor across the isolation barrier is created. This capacitor provides a return path for high frequency common-mode noise currents across the isolation gap. The internal layers are used to create the capacitor because the surface layers have minimum creepage and clearance requirements; therefore, it is not practical to use the surface layers. The layout and implementation of embedded stitching capacitors is covered in detail in the AN-0971.

The embedded stitching capacitor can be implemented using either of the following two structures:

- Overlap stitching structure
- Floating capacitive structure

Overlap Stitching Structure

The overlap stitching structure uses the concept of extending two of the internal layers of the PCB reference planes across the isolation gap area between the primary reference planes and the secondary plane. The capacitance is created in the gap beneath the isolator, where the top and bottom layers must remain clear for creepage and clearance reasons. The internal metal reference planes are separated by the dielectric material of the PCB (usually FR4), thus creating a capacitor structure. The area of the metal overlap, separated by the dielectric material, is used to calculate the capacitance of the embedded stitching structure, as shown in Figure 6.

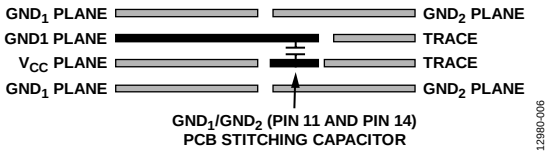

Figure 6. Overlap Stitching Capacitor PCB Layer Stackup

The capacitive coupling is calculated with the following basic relationships for parallel plate capacitors:

$$C = \frac{A\varepsilon}{d}$$

where:
C is the capacitance.
A is the area.
ε is the permittivity.
d is the distance between the layers.

For a PCB with the overlapping stitching capacitor structure, the following formula is used to determine the capacitive coupling:

$$C = \frac{lw\varepsilon}{d}$$

where:
$\varepsilon = \varepsilon_0 \times \varepsilon_r$
ε_0 is the permittivity of free space, 8.854×10^{-12} F/m.
ε_r is the relative permittivity of the PCB insulation material.
w, d, and l are the dimensions of the overlapping portion of the primary and secondary reference planes, as shown in Figure 7.

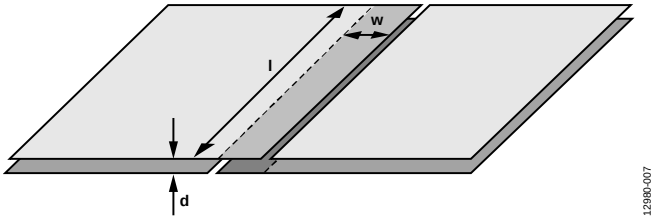

Figure 7. Overlap Stitching Capacitance

The thickness of the dielectric FR4 material between the two reference planes determines the high voltage performance of the system. These gaps are called cemented joints and provide the isolation. This architecture has only a single cemented joint and a single layer of FR4 between the primary and secondary reference planes. To increase the high voltage performance, the dielectric thickness can be increased. However, increasing the thickness of the dielectric material increases the spacing between the internal reference planes and therefore reduces the coupling capacitance achieved. For example, doubling the thickness of the dielectric material between the two internal reference planes of a given area reduces the coupling capacitance between the reference planes by half.

Floating Stitching Structure

For applications that require reinforced high voltage requirements, the floating stitching capacitor architecture is used. The floating architecture uses the concept of a floating internal metal plane to couple the high frequency common-mode currents from the secondary reference plane across the isolation gap to the primary reference plane. This architecture creates two capacitors in parallel, as shown in Figure 8.

Similar to the overlap stitching structure, the dielectric material provides the high voltage isolation across the gap. When compared with the overlapping structure from a high voltage performance point of view, the floating stitching structure has the advantage of two isolation gaps. An isolation gap exists through the thickness of the dielectric material between the secondary plane and the internal floating reference plane. There is also a second isolation gap through the thickness of the dielectric material between the internal floating reference plane and the primary reference plane. The presence of these two gaps is advantageous when creating a reinforced isolation barrier in systems that require an increased level of high voltage isolation.

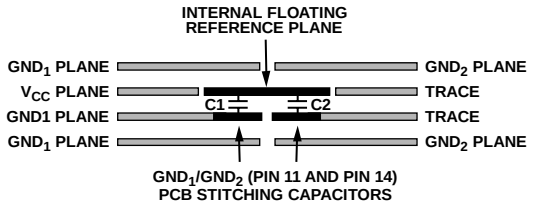

Figure 8. Floating Stitching Capacitor PCB Layer Stackup

The capacitive coupling of the structure in Figure 8 is calculated with the following basic relationships for parallel plate capacitors:

$$C = \frac{C_1 \times C_2}{C_1 + C_2}$$

$$C_1 = C_2 = \frac{A_x \varepsilon}{d}$$

where:
C is the total stitching capacitance.
A_X is the overlap area of the stitching capacitance to each reference plane.
d is the thickness of the insulation layer in the PCB.

$$\varepsilon = \varepsilon_0 \times \varepsilon_r$$

where:
ε_0 is the permittivity of free space, 8.854×10^{-12} F/m.
ε_r is the relative permittivity of the PCB insulation material.

$$C = \frac{l\varepsilon}{d} \times \left(\frac{w_1 \times w_2}{w_1 + w_2} \right)$$

where w_1, w_2, d, and l are the dimensions of the overlapping portions of the floating plane and the primary and secondary reference planes, as shown in Figure 9.

If $w_1 = w_2$, the equation simplifies to

$$C = \frac{lw_1\varepsilon}{2d}$$

Due to the parallel implementation of the capacitors, the effective capacitance is halved per the unit area compared to the overlap capacitor structure.

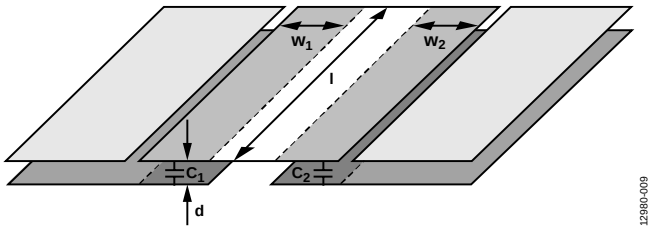

Figure 9. Floating Stitching Capacitance

ADM2582E/ADM2587E MEASURED EMISSION RESULTS PASSING EN55022

This section describes measured emission levels recorded in a certified, semianechoic, 10 m chamber. The measured emissions described reference specific PCB layouts and EM suppression techniques used to achieve

- EN55022 Class A classification
- EN55022 Class B classification

To achieve EN55022/CISPR22 Class A classification, see Figure 10 for layout details of the peripheral components.

To achieve EN55022/CISPR22 Class B classification, the addition of stitching capacitance with the layout recommendations to achieve EN55022A are required.

EN55022 Class A Classification

The EMI suppression techniques/components to achieve EN55022 Class A classification include

- Adequate decoupling capacitors on all V_{CC} and V_{ISO} pins.
- Ferrite beads on V_{ISOOUT} (Pin 12) and GND_2 (Pin 11 and Pin 14).

See Figure 10 for the optimized component placement and PCB layout.

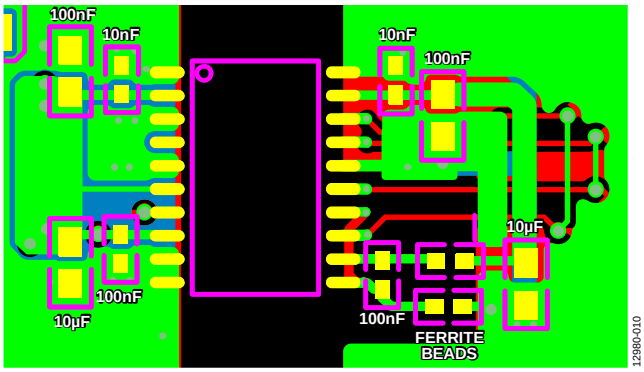

Figure 10. Optimized PCB Layout and Component Placement

The specific placement of the decoupling capacitors and the ferrites on the V_{ISOOUT} and GND_2 pins is critical. Note that the GND_2 connections on Pin 11 and Pin 14 are connected together by a PCB trace before connecting to the ferrite bead. To reduce the radiated emissions, it is important to ensure that these two GND_2 pins are connected through the ferrite before connecting to the PCB GND_2 and GND_2, Pin 16, and Pin 20.

The PCB used was a 4-layer stackup, as shown in Figure 11.

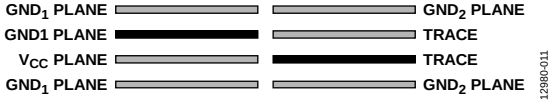

Figure 11. PCB 4-Layer Stackup

Both the ADM2582E and ADM2587E operated at V_{CC} = 3.3 V and their data switched at their maximum data rates (16 Mbps and 500 kbps, respectively). The devices were connected in half-duplex mode, connecting Pin A to Pin Y and Pin B to Pin Z. The emissions were measured in a certified, semianechoic, 10 m chamber at an external compliance test house in accordance with the EN55022 standard.

Figure 12 shows the measured radiated emissions of the ADM2582E, and Figure 13 shows the measured radiated emissions of the ADM2587E.

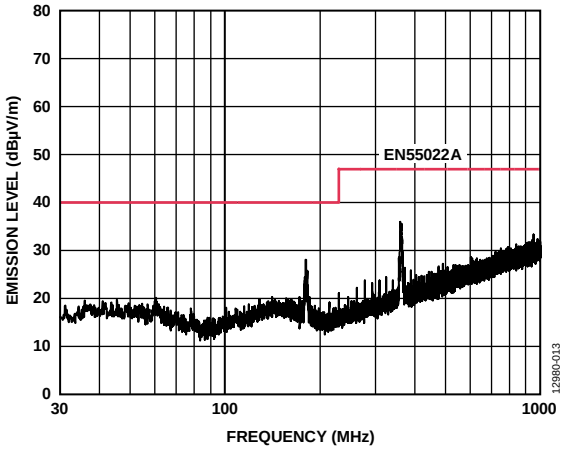

Figure 12. Plot of ADM2582E Data Switching at 16 Mbps (for Worst Case of V_{CC} = 3.3 V)

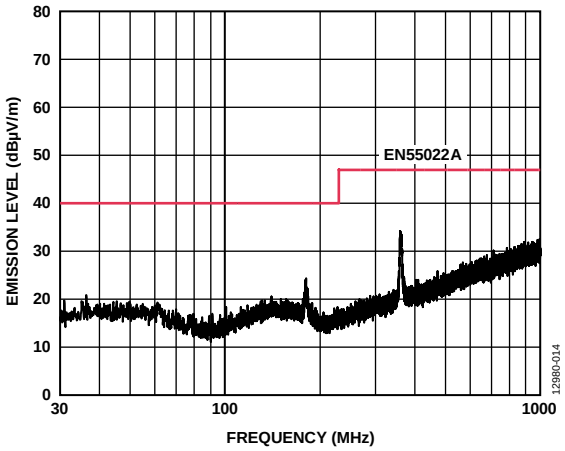

Figure 13. Plot of ADM2587E Data Switching at 500 kbps (for Worst Case of V_{CC} = 3.3 V)

EN55022 Class B Classification

The EM suppression techniques/components to achieve EN55022 Class A classification, as described in the EN55022 Class A Classification section, are also required to be implemented in achieving EN55022 Class B classification. However, an additional suppression technique of stitching capacitance across the isolation barrier is also required to achieve EN55022B. The following two methods of stitching are described:

- High voltage discrete stitching capacitor
- Overlap stitching capacitor

HIGH VOLTAGE DISCRETE STITCHING CAPACITOR

The specific placement of decoupling capacitors, the discrete high voltage capacitor, and the ferrites on the V_{ISOOUT} and GND_2 pins are critical to achieve CISPR22/EN55022B classification. The use of a high voltage discrete capacitor to pass emission limits has been proven for the ADM2587E powered at both 3.3 V and 5.0 V supplies, and for the ADM2582E powered at 5.0 V supply. When testing the ADM2582E powered at 3.3 V and operating at the maximum data rate of 16 Mbps, the high voltage discrete capacitor was not sufficient to achieve Class B Classification.

For layout details of the peripheral components, see Figure 14. The PCB used was a 4-layer stackup, as shown in Figure 15. The PCB stitching capacitance is implemented with a high voltage discrete capacitor. For optimal performance, it is important that the capacitor be connected directly to the GND_2 pin, Pin 11 (between the device pin and the ferrite). Measured results shown were taken with a 100 pF, 1812 body size capacitor. This capacitor has a 3 kV voltage rating and is manufactured by TDK Corporation (C4532C0G3F101K160KA).

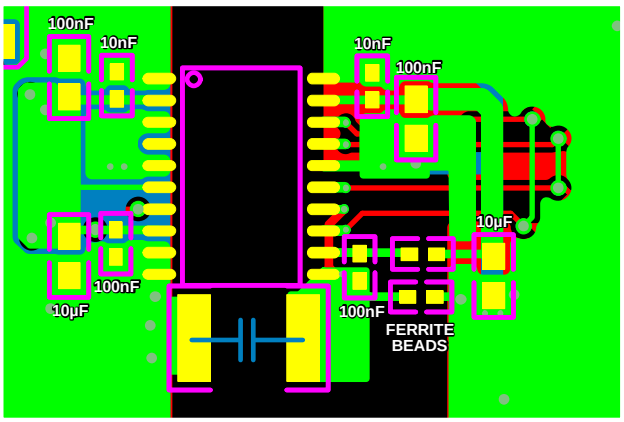

Figure 14. Optimized PCB Layout and Component Placement

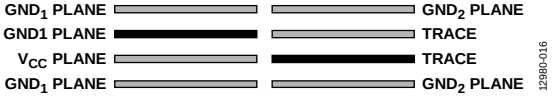

Figure 15. PCB 4-Layer Stackup

The emission measurement was recorded in a certified, semianechoic, 10 m chamber at an external compliance test house in accordance with the EN55022 standard. Figure 16 shows the radiated emissions of the ADM2582E, and Figure 17 shows the radiated emissions of the ADM2587E.

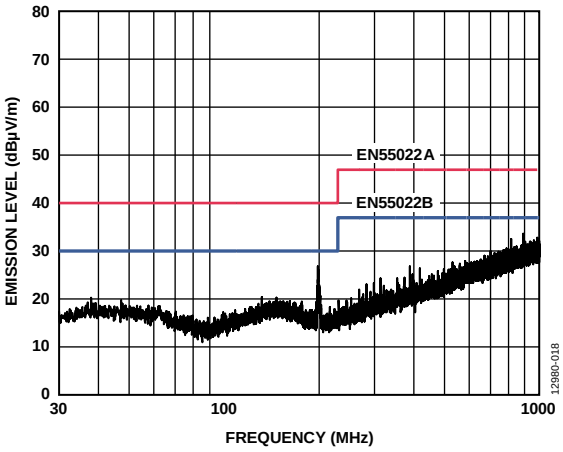

Figure 16. Plot of ADM2582E Data Switching at 16 Mbps (Powered at V_{CC} = 5.0 V)

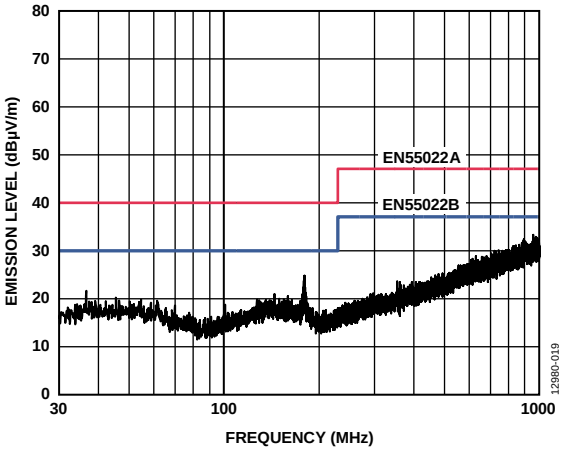

Figure 17. Plot of ADM2587E Data Switching at 500 kbps (for Worst Case of V_{CC} = 3.3 V)

Overlap Stitching Capacitor

The specific placement of decoupling capacitors and the ferrites on the V_{ISOOUT} and GND_2 pins is critical to achieve optimal performance. See Figure 18 for layout details of the peripheral components. The PCB used was a 4-layer stackup, as shown in Figure 19. The example PCB stitching capacitance was implemented using the overlap structure by extending the internal metal plane of Layer 2 (connected to GND_1) and extending a metal area in Layer 3 (connected to V_{ISOOUT}) to create an overlap of metal between Layer 2 and Layer 3. The area of the overlap (see Figure 19) between these two reference planes on Layer 2 and Layer 3 is the size of the ADM2582E/ADM2587E package. The overlap between these two metal reference planes separated by the FR4 material results in a capacitance of ~35 pF when the dielectic FR4 spacing between Layer 2 and Layer 3 is 0.1016 mm. If increased layer spacing compared to this example is required in an application to maintain higher isolation performance, the area of overlap must be increased correspondingly.

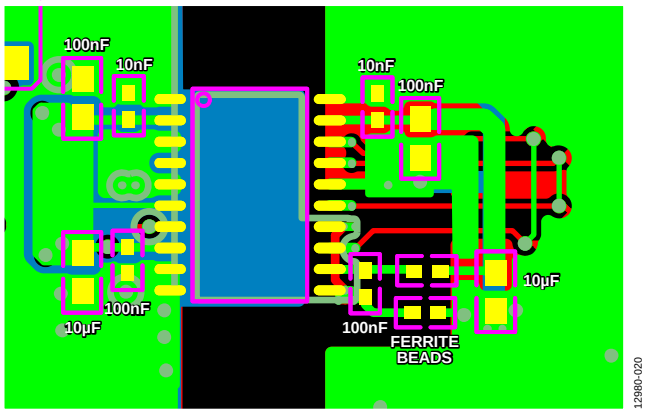

Figure 18. Embedded Stitching Capacitor PCB Layout and Component Placement

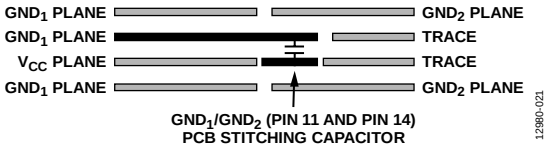

Figure 19. PCB 4-Layer Stackup

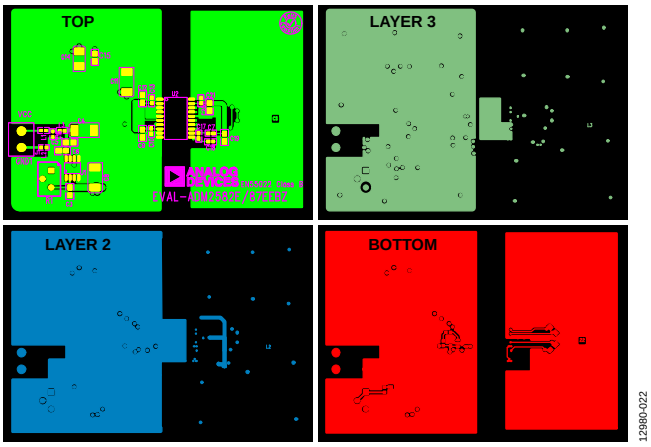

Figure 20. PCB Layout Achieving EN55022 Class

The emission measurement was recorded in a certified, semianechoic, 10 m chamber at an external compliance test house in accordance with the EN55022 standard. Both the ADM2582E and ADM2587E powered at 3.3 V and their data switched at their maximum data rates (16 Mbps and 500 kbps, respectively). Figure 21 shows the measured radiated emissions of the ADM2582E, and Figure 22 shows the measured radiated emissions of the ADM2587E.

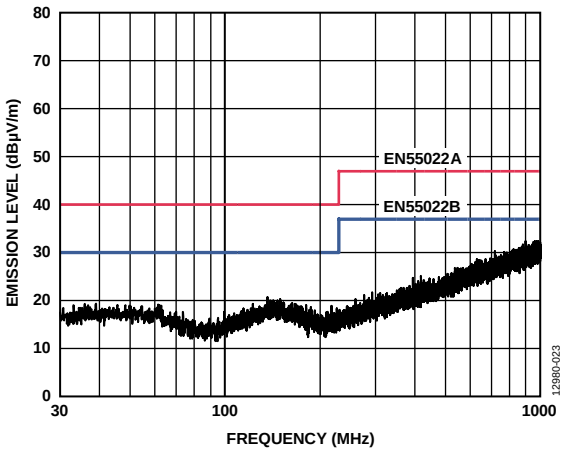

Figure 21. Plot of ADM2582E Data Switching at 16 Mbps

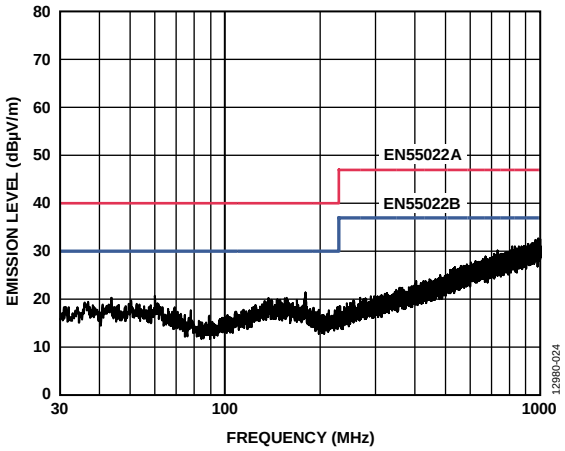

Figure 22. Plot of ADM2587E Data Switching at 500 kbps

EVALUATION PCBS AVAILABLE TO USERS WITH MEASURED RADIATED EMISSIONS RESULTS

Evaluation PCBs are available to order from the EVAL-ADM2587E and EVAL-ADM2582E product pages. Emission measurements are recorded in a certified, semianechoic, 10 m chamber at an external compliance test house in accordance with the EN55022 standard. Both the ADM2582E and ADM2587E are powered at 3.3 V and 5.0 V and data was switched on the ADM2582E and ADM2587E TxD pin at their maximum data rates (16 Mbps and 500 kbps, respectively).

The following evaluation PCBs with 2-layer and 4-layer PCB stackup are available:

- The 2-layer boards: EVAL-ADM2582EEMIZ and EVAL-ADM2587EEMIZ
- The 4-layer boards: EVAL-ADM2582EEBZ or EVAL-ADM2587EEBZ

EN55022 certification documents for these evaluation boards are available to users upon request from Analog Devices Central Applications or the local Analog Devices field applications engineer (see the Technical Support page).

2-Layer User Evaluation PCB Emission Results

Table 3 shows a summary of the EN55022 radiated emissions test results from EVAL-AD2582EEMIZ/EVAL-AD2587EEMIZ user guide for the 2-layer boards.

4 -Layer User Evaluation PCB Emission Results

The EN55022 radiated emission test results in Table 4 are obtained by following the PCB guidelines in this application note and implementing the embedded PCB stitching capacitance between GND1 and GND2. For further design and layout details of the 4-layer PCBs, see the EVAL-ADM2582EEBZ/ EVAL-ADM2587EEBZ user guide.

Table 3. Summary of EN55022 Radiated Emissions Test Results for the EVAL-ADM2582EEMIZ and EVAL-ADM2587EEMIZ 2-Layer Boards

Device	High Voltage Capacitor	Supply	Data Rate	Load	EM55022 Class	Pass Margin (dBµV)
ADM2582E	No	3.3 V	16 Mbps	54 Ω	A	1.2
ADM2582E	No	5.0 V	16 Mbps	54 Ω	A	4.7
ADM2582E	Yes	3.3 V	16 Mbps	54 Ω	B	3.7
ADM2582E	Yes	5.0 V	16 Mbps	54 Ω	A	7.5
ADM2587E	No	3.3 V	500 kbps	54 Ω	A	3.9
ADM2587E	No	5.0 V	500 kbps	54 Ω	A	4

Table 4. Summary of EN55022 Radiated Emissions Test Results for the EVAL-ADM2582EEMIZ and EVAL-ADM2587EEMIZ 4-Layer Boards

Device	Embedded Stitching Capacitor	Supply	Data Rate	Load	EM55022 Class	Pass Margin (dBµV)
ADM2582E	Yes	3.3 V	16 Mbps	54 Ω	B	4.7
ADM2582E	Yes	5.0 V	16 Mbps	54 Ω	B	6.5
ADM2587E	Yes	3.3 V	500 kbps	54 Ω	B	5.5
ADM2587E	Yes	5.0 V	500 kbps	54 Ω	B	8.5

REFERENCES

AN-0971 Application Note, *Control of Radiated Emissions with isoPower Devices*. Analog Devices, Inc.

Archambeault, Bruce R. and James Drewniak. *PCB Design for Real-World EMI Control*. Boston: Kluwer Academic Publishers, 2002