ANALOG DEVICES

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APPLICATION NOTE

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Recommendations for Control of Radiated Emissions with *i*Coupler Devices

by Brian Kennedy and Mark Cantrell

INTRODUCTION

*i*Coupler® data isolation products can readily meet CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment, with proper PCB design choices. This application note examines PCB-related EMI mitigation techniques, including board layout and stack-up issues.

Several standards for radiated emissions exist. In the U.S., the Federal Communications Commission (FCC) controls the standards and test methods. In Europe, the International Electrotechnical Commission (IEC) generates standards, and CISPR test methods are used for evaluating emissions. The methods and pass/fail limits are slightly different under the two standards. Although this application note references IEC standards, all results are applicable to both standards.

Data transitions at the input of *i*Coupler digital isolators are encoded as narrow pulses that are used to send information across the isolation barrier. These 1 ns pulses have peak currents of up to 70 mA and may cause radiated emissions and conducted noise if not considered during printed circuit board (PCB) layout and construction. This application note identifies the radiation mechanisms and offers specific guidance on addressing them through high frequency PCB design techniques.

Control of emissions from signal cables and chassis shielding techniques are outside of the scope of this application note.

EMI MITIGATION OVERVIEW

Best-practice techniques for EMI mitigation include a combination of the use of input-to-output ground plane stitching capacitance, edge guarding, and the reduction of supply voltage levels for noise reduction. For the purposes of this application note, a 4-layer board was designed and manufactured using materials and structures well within industry practice.

The EMI reduction examples used in this application note are based on the 4-channel *i*Coupler products, but the information is relevant to all the *i*Coupler product families, examples of which are shown in Figure 1.

For information on reducing emissions from products using *iso*Power, integrated isolated power, refer to the AN-0971 Application Note, which includes additional recommendations and techniques.

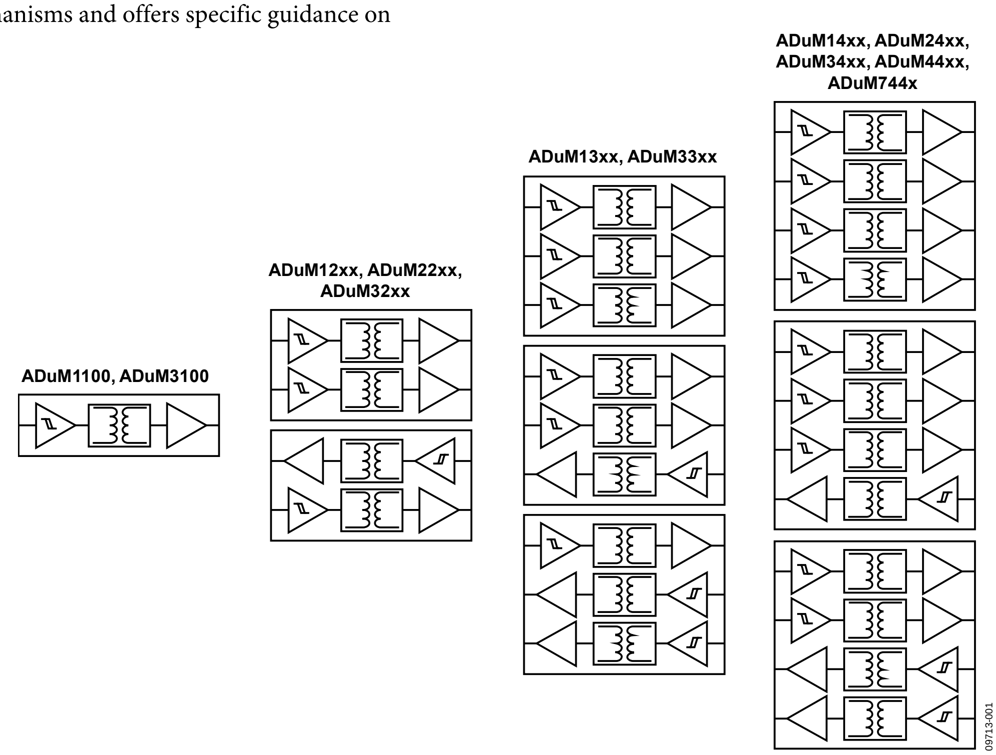

Figure 1. Example of iCoupler Device Families

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REVISION HISTORY

4/11—Revision 0: Initial Version

SOURCES OF RADIATED EMISSIONS

There are two potential sources of emissions in PCBs: edge emissions and input-to-output dipole emissions.

EDGE EMISSIONS

Edge emissions occur when unintended currents meet the edges of ground and power planes. These unintended currents can originate from

- Ground and power noise, generated by inadequate bypass of high power current sinks.
- Cylindrically radiated magnetic fields coming from inductive via penetrations radiated out between board layers eventually meeting the board edge.
- Stripline image charge currents spreading from high frequency signal lines routed too close to the edge of the board.

Edge emissions are generated where differential noise from many sources meet the edge of the board and leak out of a plane-to-plane space, acting as a wave guide (see Figure 2).

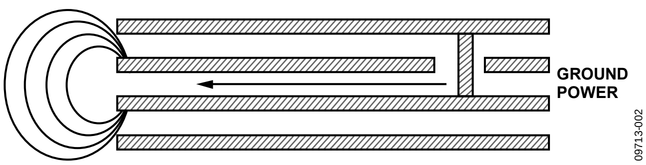

Figure 2. Edge Radiation from an Edge Matched Ground Power Pair

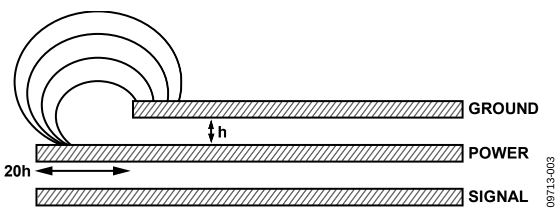

Figure 3. Edge Radiation from an Edge Mismatched Power Ground Pair

At the edge boundary, there are two limiting conditions: the edges of the ground and power planes are aligned as in Figure 2 or one edge is pulled back by some amount as shown in Figure 3. In the first case, with aligned edges, there is some reflection back into the PCB and some transmission of the fields out of the PCB. In the second case, the edges of the board make a structure similar to the edge of a patch antenna. When the edges mismatch by 20h where h is the plane-to-plane pacing, the fields efficiently couple out of the PCB, resulting in high emissions (see “Minimizing EMI Caused by Radially Propagating Waves Inside High Speed Digital Logic PCBs” in the References section). These two limiting cases are important considerations as described in the edge treatment of the PCB in the Edge Guarding section.

INPUT-TO-OUTPUT DIPOLE EMISSIONS

The primary mechanism for radiation is an input-to-output dipole generated by driving a current source across a gap between ground planes. Isolators, by their very nature, drive current across gaps in ground planes. The inability of high frequency image charges associated with the transmitted current to return across the boundary causes differential signals across the gap driving the dipole. In some cases, this may be a large dipole, as shown in Figure 4. A similar mechanism causes high frequency signal lines to radiate when crossing splits in the ground and power planes. This type of radiation is predominantly perpendicular to the ground planes.

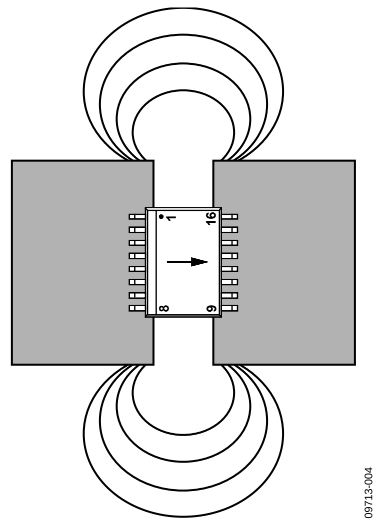

Figure 4. Dipole Radiation Between Input and Output

The ADuM140x devices serve as a good example of the issues involved in generating and mitigating emissions.

When operating under a full 5 V V_{DD} supply voltage, the peak currents of the transmitter pulses is about 70 mA, and these pulses are 1 ns wide with fast edge rates.

Bypass capacitors are intended to provide this high frequency current locally. The capacitor must provide large charge reserves. At the same time, the capacitor should have a very low series resistance at high frequencies in the 100 MHz to 1 GHz range. Even with multiple low ESR capacitors near the pins, inductively limited bypassing generates voltage transients, and the noise may be injected onto the ground and power planes. The self-resonant frequency of capacitors should be considered. Having multiple capacitors of various sizes, 100 nF, 10 nF, and 1 nF, may help reduce this effect.

Figure 5 shows emissions data collected in an anechoic chamber taken with a 4-channel ADuM1402 with 5 V supplies, running at 1 Mbps signal frequency and using a standard 4-layer PCB, but without an input-to-output ground plane stitching capacitance.

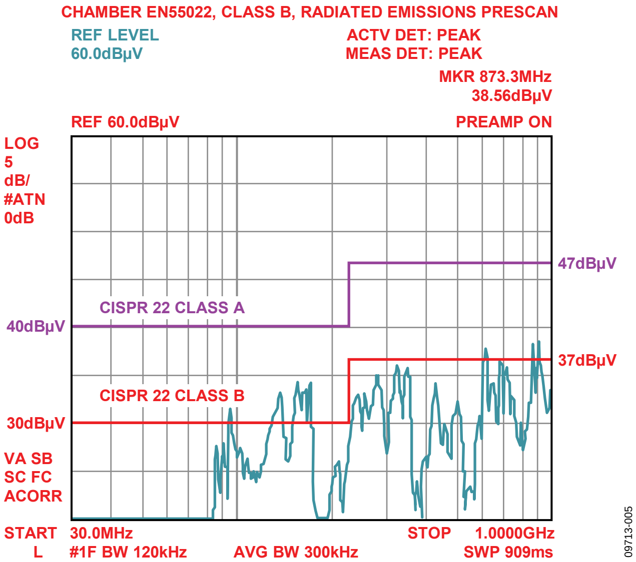

Figure 5. Anechoic Chamber Emissions from a Standard 4-Layer Board with 4-Channel ADuM1402 at 1 Mbps

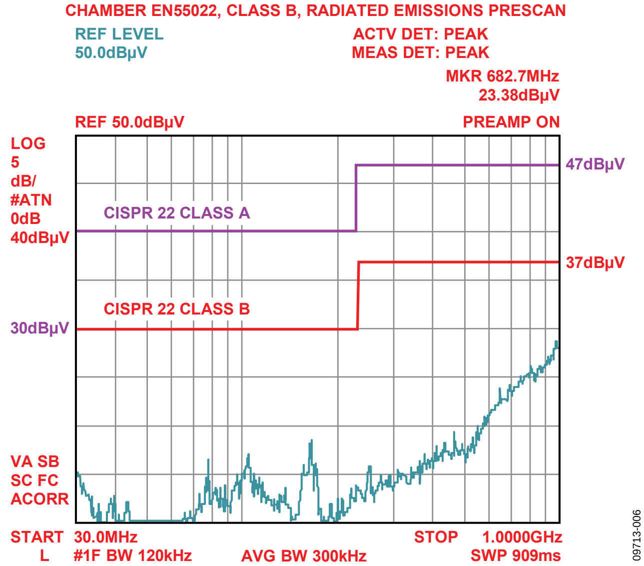

Figure 6. Anechoic Chamber Emissions from a Low Noise 4-Layer Board with 300 pF Stitching Capacitance and 4-Channel ADuM1402 at 1 Mbps

The emissions data for this board, as shown in Figure 5, passes CISPR 22 Class A emissions standards by approximately 6 dBµV in the 30 MHz to 230 MHz range (40 dBµV requirement). In contrast, Figure 6 shows the results of a low noise, 4-layer board using a 300 pF stitching capacitance. This was tested under the same conditions as the standard board but passes CISPR 22 Class A and CISPR 22 Class B by a wide margin. The EMI Mitigation Techniques section describes how to use some recommended PC layout techniques like those used on the low noise board to control radiated emissions.

SOURCES OF CONDUCTED NOISE

Large currents and frequencies also generate conducted noise on the ground and power planes. This can be addressed with the same techniques for radiated emissions because the causes and remedies for both types of EMI can be improved with the same PCB ground and power structures.

The inability of the bypass capacitors and ground/power planes to provide adequate high frequency current to the *i*Coupler device causes V_{DD} noise. The *i*Coupler isolator transmits data across the transformer in bursts of 1 ns pulses with an amplitude of 70 mA. An ideal bypass capacitor of 100 nF should be adequate to supply the ac component of the current. However, bypass capacitors are not ideal and may connect to the ground or power planes through an inductive via. In addition, a large distance between ground and power planes creates a large inductance between them, which restricts the ability to supply current quickly. These factors may contribute to a large fraction of a volt of high frequency noise on the V_{DD} plane.

EMI MITIGATION TECHNIQUES

Many mitigation techniques are available to the designer. Several techniques that apply directly to the *i*Coupler devices are identified in this section. There are trade-offs between how aggressively to address EMI to pass IEC or FCC emissions levels and the requirements of the design, including cost and performance.

To take full advantage of PCB related EMI mitigation practices, a PCB should rely on having relatively continuous ground and power planes with the ability to specify relative positions and distances in the stack-up. This suggests the use of at least three layers to take full advantage of these techniques: ground, power, and signal planes.

For practical considerations in board manufacture, a 4-layer board is the minimum stack-up. More layers are acceptable and can be used to greatly enhance the effectiveness of the recommendations. If a 2-layer board is used, a safety stitching capacitor can be used to reduce emissions, as described in the Input-to-Output Stitching section.

The following techniques are effective in reducing EMI radiation and on-board noise:

- Input-to-output ground plane stitching
- Edge guarding
- Interplane capacitive bypass
- Power control (3.3 V operation)

Circuit boards with test structures were prepared to evaluate each of these EMI mitigation techniques using the ADuM140x. The layout of each board was varied as little as possible to allow meaningful comparison of results. Testing was conducted at an EMI test facility under standard conditions for CISPR 22 Class B certification. Results are shown in Figure 14 to Figure 17 and summarized in Table 4 to Table 7.

INPUT-TO-OUTPUT STITCHING

When current flows along PCB traces, an image charge follows along the ground plane beneath the trace. If the trace crosses a gap in the ground plane, the image charge cannot follow along. This creates differential currents and voltages in the PCB, leading to radiated and conducted emissions. The solution is to provide a path for the image charge to follow the signal. Standard practice is to place a stitching capacitor in proximity to the signal across the split in the ground plane (see "*PCB Design for Real-World EMI Control*" in the References section). This same technique works to minimize radiation between ground planes due to the operation of *i*Coupler isolators.

There are at least three options to form a stitching capacitance.

- A safety rated capacitor applied across the barrier.
- Ground and power planes on an interior layer can be extended into the isolation gap of the PCB to form an overlapping stitching capacitor.
- A floating metal plane can span the gap between the isolated and nonisolated sides on an interior layer, as shown in Figure 8.

Each option has advantages and disadvantages in effectiveness and area required to implement. Note that, for medical applications, the total isolation capacitance allowed between isolated ground and earth ground may only be as large as 10 pF to 20 pF.

Safety Stitching Capacitor

Stitching capacitance can be implemented with a simple ceramic capacitor across the isolation barrier. Capacitors with guaranteed creepage, clearance, and withstand voltage can be obtained from most major capacitor manufacturers. These safety rated capacitors come in several grades depending on their intended use. The Y2 grade is used in line-to-ground applications where there is danger of electric shock and is the recommended safety capacitor type for a stitching capacitor in a safety rated application. This type of capacitor is available in surface-mount and radial leaded disk versions. See Table 1 for a list of some Y2 grade safety capacitors.

Because safety capacitors are discrete components, they must be attached to the PCB with pads or through holes. This adds parasitic inductance in series with the capacitor, on top of its intrinsic inductance. It also localizes the stitching capacitor, requiring currents to flow to the capacitor, which can create asymmetrical image charge paths and added noise. These discrete capacitors are effective at frequencies up to 200 MHz. Above 200 MHz, capacitance built into the PCB layers can be very effective.

Capacitance Built Into the PCB

The PCB itself can be designed to create a stitching capacitor structure in several ways. A capacitor is formed when two planes in a PCB overlap. This type of capacitor has some very useful properties in that the inductance of the parallel plate capacitor formed is extremely low, and the capacitance is distributed over a relatively large area.

These structures must be constructed on internal layers of a PCB. The surface layers have minimum creepage and clearance requirements; therefore, it is not practical to use surface layers for this type of structure.

Table 1. Safety Capacitors

Safety Rating	Working Voltage Rating (VAC)	Isolation Voltage Rating (VAC)	Package Type/Size	Value (pF)	Manufacturer	Part No.
X1/Y2	250	1500	SMT/1808	150	Johanson Dielectrics	502R29W151KV3E-SC
X1/Y2	250	2000	Radial/5 mm	150	Murata	DE2B3KY151KA2BM01
X1/Y2	300	2600	Radial/7.5 mm	150	Vishay	VY2151K29Y5SS63V7

Overlapping Stitching Capacitor

A simple method of achieving a good stitching capacitance is to extend a reference plane from the primary and secondary sides into the area that is used for creepage on the PCB surface.

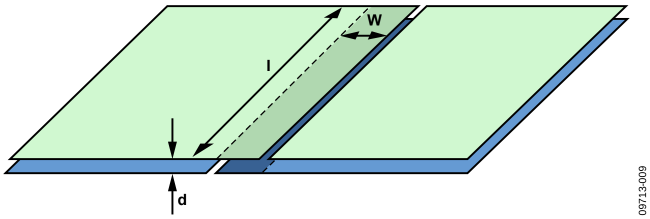

Figure 7. Overlapping Plane Stitching Capacitance

The capacitive coupling of the structure in Figure 7 is calculated with the following basic relationships for parallel plate capacitors:

$$C = \frac{A\varepsilon}{d} \text{ and } \varepsilon = \varepsilon_0 \times \varepsilon_r$$

where:
C is the total stitching capacitance.
A is the overlap area of the stitching capacitance.
ε_0 is the permittivity of free space, 8.854×10^{-12} F/m.
ε_r is the relative permittivity of the PCB insulation material, which is about 4.5 for FR4, as shown in Table 2.

$$C = \frac{lw\varepsilon}{d} \quad (1)$$

where w, d, and l are the dimensions of the overlapping portion of the primary and secondary reference planes as shown in Figure 7.

The major advantage of this structure is that the capacitance is created in the gap beneath the isolator, where the top and bottom layers must remain clear for creepage and clearance reasons. This board area is not utilized in most designs. The capacitance created is also twice as efficient per unit area as the floating plane.

This architecture has only a single cemented joint and a single layer of FR4 between the primary and secondary reference planes. It is well suited to smaller boards where only basic insulation is required.

Table 2. Electrical Properties

Type	Dielectric Constant at 1 MHz	Dielectric Strength (V/mil)
FR4	4.5	1000 to 1500
GETEK	3.6 to 4.2	1000 to 1200
BT-Epoxy	4.0	750

Floating Stitching Capacitor

A good option is to use a floating metal structure on an interior layer of the board to bridge between the primary and secondary power planes. Note that planes dedicated to ground or power are referred to as reference planes in this application note because, from an ac noise perspective, they behave the same and can be used interchangeably for stitching capacitance.

An example of a floating stitching capacitance is shown in Figure 8. The reference planes are shown in blue and green, and the floating coupling plane is shown in yellow. The capacitance of this structure creates two capacitive regions (shown with shading) linked by the nonoverlapping portion of the structure. To ensure that there is no dc voltage accumulated on the coupling plane, the area on the primary and secondary should be approximately equal.

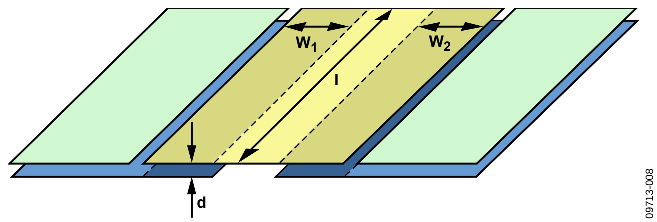

Figure 8. Floating Stitching Capacitance

The capacitive coupling of the structure in Figure 8 is calculated with the following basic relationships for parallel plate capacitors:

$$C_x = \frac{A_x\varepsilon}{d},\ \varepsilon = \varepsilon_0 \text{ x } \varepsilon_r,\ C = \frac{c_1 \times c_2}{c_1 + c_2}$$

where:
C is the total stitching capacitance.
A is the overlap area of the stitching capacitance.
ε_0 is the permittivity of free space, 8.854×10^{-12} F/m.
ε_r is the relative permittivity of the PCB insulation material, which is about 4.5 for FR4, as shown in Table 2.

$$C = \frac{l\varepsilon}{d} \times \left(\frac{w_1 \times w_2}{w_1 + w_2}\right) \quad (2)$$

where w_1, w_2, d, and l are the dimensions of the overlapping portions of the floating plane and the primary and secondary reference planes as shown in Figure 8.

If $w_1 = w_2$, the equation simplifies to

$$C = \frac{lw_1\varepsilon}{2d} \quad (3)$$

There are advantages and disadvantages to this structure in real applications. The major advantage is that there are two isolation gaps, one at the primary and one at the secondary. These gaps are referred to as cemented joints, where the bonding between layers of FR4 provides the isolation.

There are also two sequential paths through the thickness of the PCB material. The presence of these gaps and thicknesses is advantageous when creating a reinforced isolation barrier under some isolation standards. The disadvantage of this type of structure is that the capacitance is formed under the active circuit area so there can be via penetrations and traces that run across the gaps. Equation 2 also shows that the net capacitance resulting from two capacitors in series is only half the value that results from using the same PCB area to form a single capacitor. Therefore, this technique is less efficient from a capacitance per unit area perspective. Overall, it is best suited to applications where a large amount of board area is available, or where reinforced insulation is required.

EDGE GUARDING

Noise on the power and ground planes that reaches the edge of a circuit board can radiate as shown in Figure 2 and Figure 3. If the edge is treated with a shielding structure, the noise is reflected back into the interplane space (see "Minimizing EMI Caused by Radially Propagating Waves Inside High Speed Digital Logic PCBs" in the References section). This can increase the voltage noise on the planes, but it can also reduce edge radiation.

Making a solid conductive edge treatment on a PCB is possible, but the process is expensive. A less expensive solution that works well is to treat the edges of the board with a guard ring structure laced together by vias. The structure is shown in Figure 9 for a typical 4-layer board. Figure 10 shows how this structure is implemented on the power and ground layers of the primary side of a circuit board.

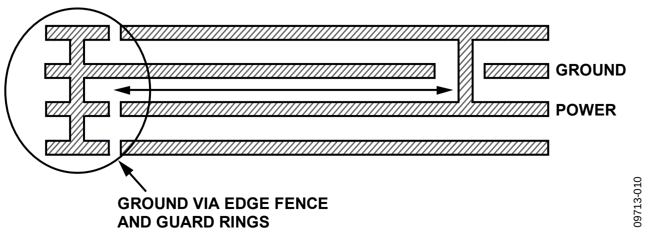

Figure 9. Via Fence Structure, Side View

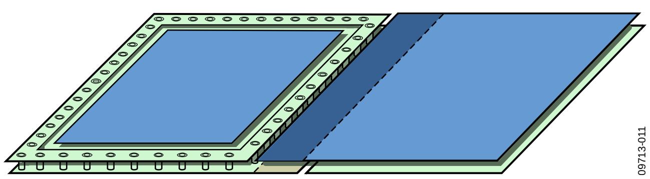

Figure 10. Via Fence and Guard Ring, Shown on the Primary Power Plane Layers

There are two goals in creating edge guarding. The first goal is to reflect cylindrical emissions from vias back into the interplane space, not allowing it to escape from the edge. The second goal is to shield any edge currents flowing on internal planes due to noise or large currents flowing on traces.

The spacing of the vias used to create the edge guard is difficult to determine without extensive modeling. Analog Devices, Inc., test boards used 4 mm via spacing for their evaluation boards. This spacing is small enough to provide attenuation to signals less than 18 GHz

INTERPLANE CAPACITANCE

Interplane capacitance bypassing is a technique intended to reduce both the conducted and radiated emissions of the board by improving the bypass integrity at high frequencies. This has two beneficial effects. First, it reduces the distance that high frequency noise can spread in the ground and power plane pair. Second, it reduces the initial noise injected into the power and ground planes by providing a bypass capacitance that is effective between 300 MHz and 1 GHz (see *PCB Design for Real-World EMI Control* in the References section). Power and ground noise reduction provides a better operating environment for noise sensitive components near the *i*Coupler isolator. Both conducted and radiated emissions are reduced proportionate to the reduction in power and ground noise. The reduction in radiated emissions is not as significant as that achieved with the stitching or edge guarding techniques; however, it significantly improves the power environment of the board.

The stack-up used for EMI test boards was signal-ground-power-signal, as shown in Figure 11. A thin core layer is used for the power and ground planes. These tightly coupled planes provide the interplane capacitance layer that supplements the bypass capacitors required for proper operation of the isolator.

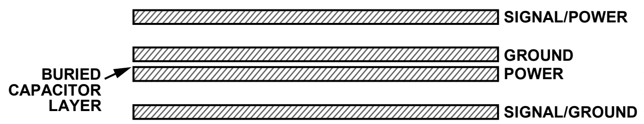

Figure 11. PCB Stack-Up for Interplane Capacitance

In addition to the ground and power planes, the capacitance can be increased even further by filling signal layers with alternating ground and power fill. The top and bottom layers in Figure 11 are labeled signal/power and signal/ground to illustrate the fills on those particular layers. These fills have the added benefit of creating additional shielding for EMI that leaks around the edges of a via fence structure, keeping it in the PCB. Care should be taken when making ground and power fills. Fills should be tied back to the full reference plane, because a floating fill can act as a patch antenna and radiate instead of shielding. Some recommended practices for fills include

- Fills should be tied to their appropriate reference plane along the edges with vias, every 10 mm.
- Thin fingers of fill should be removed.
- If the fill has an irregular shape, put vias at the extreme edges of the shape.

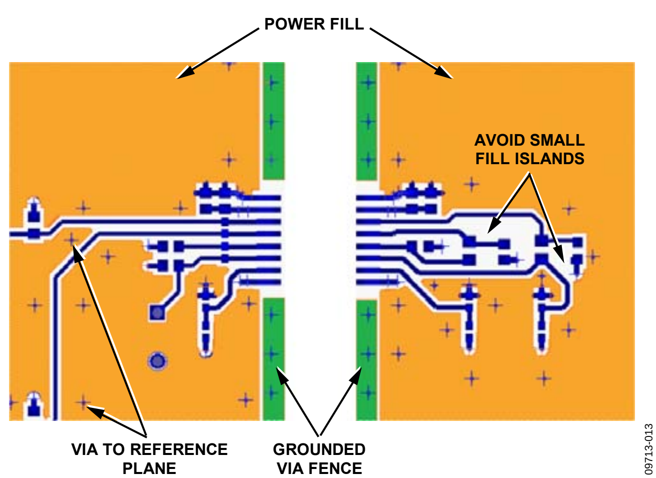

Figure 12. Features of Fill

The effectiveness of interplane capacitance is shown in Figure 13. It shows the noise generated on the V_{DD} supply by the encoder pulses in an ADuM140x series part. In the top section, it shows about 0.17 V p-p noise on the V_{DD1} pin generated on a 2-layer board. The bottom section shows a PCB with ground and power planes separated by a 0.1 mm core spacing with a substantial improvement in noise to only 0.03 V p-p. This illustrates that if tightly spaced ground and power planes are used, the power supply noise can be dramatically reduced.

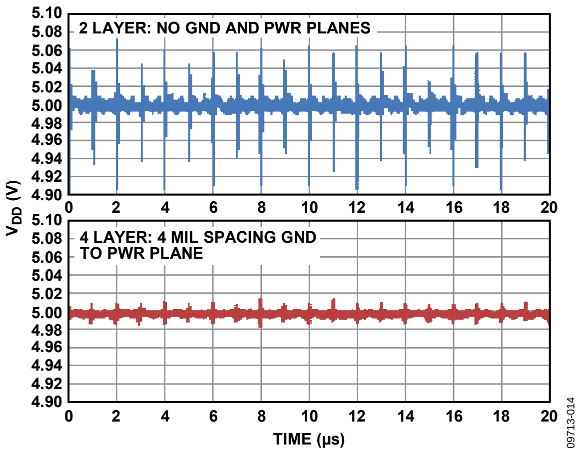

Figure 13. V_{DD} Voltage Noise for Different PCB Layouts

3.3 V OPERATION

Many *i*Coupler products can operate with 3.3 V input and output supplies. Operation at lower voltages reduces generated noise as well as production of radiated emissions. Figure 14 to Figure 17 show how emissions are reduced using a standard 4-layer evaluation board with the 4-channel ADuM1402 when 3.3 V supplies are used instead of 5 V supplies.

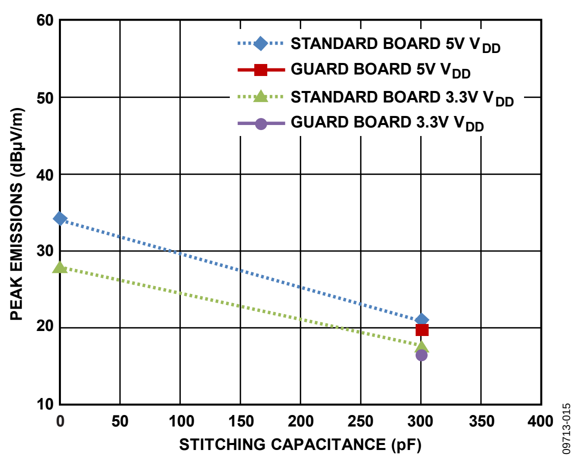

Figure 14. Peak Emissions at Frequencies of 30 MHz to 230 MHz at 1 Mbps Rate for Stitching Capacitance and Guard Options

Figure 14 to Figure 17 also show the emissions for a variety of 4-layer evaluation boards that vary in amount of primary side to secondary side stitching capacitance and guard options. The data in these figures is used for Table 4 to Table 7 in the Example Board section to show how to apply layout techniques to reduce emissions to meet CISPR 22 Class B emissions standards.

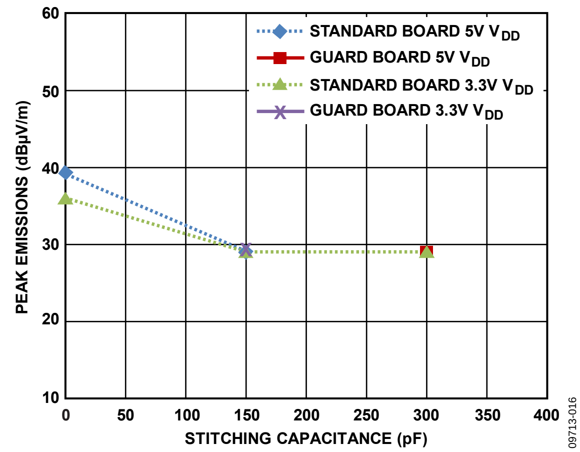

Figure 15. Peak Emissions at Frequencies of 230 MHz to 1000 MHz at 1 Mbps Rate for Stitching Capacitance and Guard Options

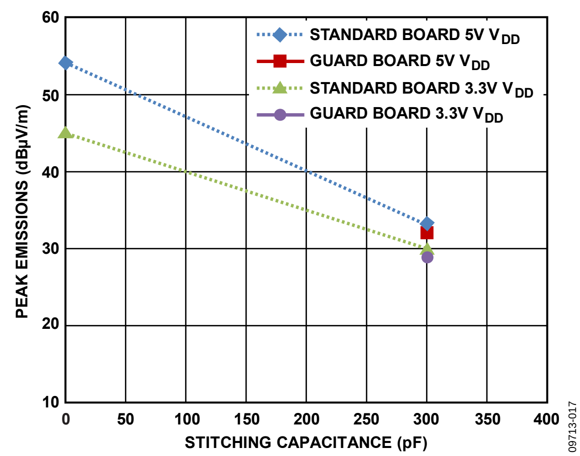

Figure 16. Peak Emissions at Frequencies of 30 MHz to 230 MHz at 10 Mbps Rate for Stitching Capacitance and Guard Options

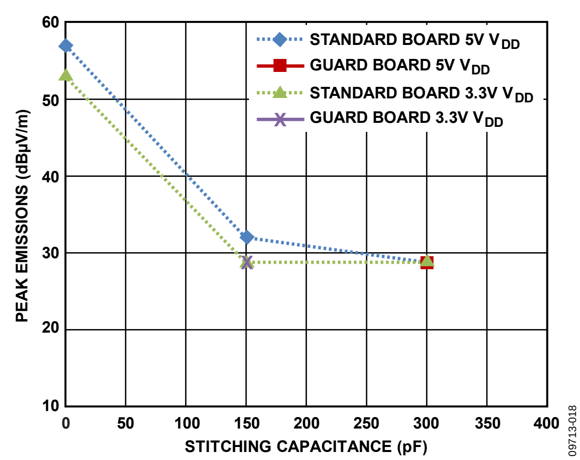

Figure 17. Peak Emissions at Frequencies of 230 MHz to 1000 MHz at 10 Mbps Rate for Stitching Capacitance and Guard Options

RECOMMENDED DESIGN PRACTICES

Consider the following general practices:

- Use a minimum stack-up of four layers.
- Make the GND layer as close as possible to the V_{DD} layer to maximize the bypass capacitance value.
- All vias in the power path should be as large as practical. Small vias have high inductance and generate noise. Using multiple small vias is not as effective in reducing via inductance as a single large via because the bulk of the current goes through the closest via, even if multiple paths are present.
- Be careful to route signal lines over a single reference plane. It is vital to maintain the image charge path so that image charges do not travel by circuitous routes to meet with the original signal on another plane.
- Do not route high speed lines close to the edges of the PCB.
- Routing data or power off boards, especially through cables, can introduce an additional radiation concern. Feed-through filter capacitors or similar filter structures can be used to minimize cable radiation.

MEETING ISOLATION STANDARDS

Most of the techniques described in this application note do not affect board isolation, with the exception of the stitching capacitor. When stitching is implemented with a safety capacitor, the capacitor has rated working and transient voltages, as well as specified creepage and clearance. This makes the safety capacitor relatively easy to deal with from a certification point of view. However, its performance as an EMI suppression element is limited.

The PCB stitching capacitor by its nature is most effective when conductors are located as close to each other as possible. For maximum performance from these elements, it is necessary to push the internal spacing requirements as far as possible, while maintaining safety. The limits of internal spacing depend heavily on the standard that the system is built for. Different standards can have completely different approaches to PCB construction.

Certification agencies treat the surface layers of a multilayer PCB differently from interior layers. The surface has creepage and clearance requirements that are driven by air ionization and voltage breakdown along dirty surfaces. Interior layers are treated as solid insulation or permanently cemented joints between solid insulation.

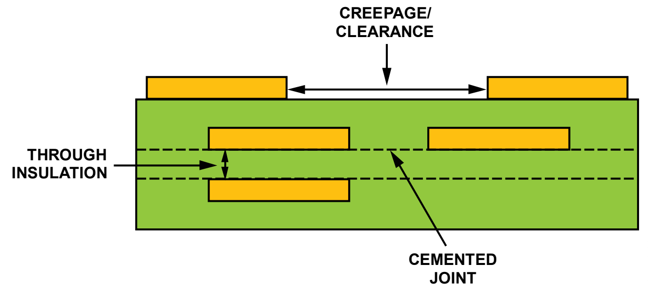

Figure 18. Critical Distances in PCB design

In PCB insulation, it is important to certification agencies that materials have an adequate dielectric breakdown to pass the transient test requirements and that they are constructed in a way that the insulation does not break down over time. Table 3 compares four standards. Each has a different solution to what is required to make a basic or reinforced insulation barrier inside a PCB.

In the case of the IEC 60950 standard in PCBs, there is no minimum specification for distance through the insulation for functional or basic insulation standards. Thus, the designer has a great deal of flexibility in board layout. Materials such as FR4 must be thick enough to withstand the required overvoltage for the life of the product.

If reinforced insulation is required, a minimum distance of 0.4 mm (about 16 mil) of insulation along a bonded surface, such as the gap between copper structures on an internal PCB layer or directly through the insulation from layer to layer, must be maintained in most cases. In addition, there can be type testing requirements for circuit boards unless multiple layers of insulation are used between active structures. Although this requirement necessitates careful board design and possibly more than four layers, it should not be burdensome if taken into account at the start of a design.

Capacitive coupling across the isolation barrier allows ac leakage and transients to couple from one ground plane to the other. Although 300 pF seems small, high voltage, high speed transients can inject significant currents across the barrier through this capacitance. Take this into account if the application is to be subjected to these environments.

Table 3. Comparison of Isolation Creepage in Isolation Standards

	IEC 60950		IEC 61010 2nd Edition		IEC 61010 3rd Edition		IEC 60601
Type of Insulation	Through insulation (2.10.6.4)	Along a cemented joint (2.10.6.3)	Through insulation (6.7.2.2.3)	Along a cemented joint (6.7.2.2.3)	Through insulation (6.7)	Along a cemented joint (6.7)	Cemented and solid insulation
Functional Insulation	No requirement	No requirement	No requirement	No requirement	0.4 mm minimum	0.4 mm minimum	Verified by test
Basic Insulation	No requirement	No requirement	No requirement	No requirement	0.4 mm minimum	0.4 mm minimum	Verified by test
Supplemental/ Reinforced insulation	0.4 mm minimum or multiple layers of insulation, precured	0.4 mm min (2.10.5.2)	No requirement	No requirement	0.4 mm minimum or multiple layers of insulation, precured	0.4 mm minimum	Verified by test

EXAMPLE BOARD

Choosing a combination of PCB structures and techniques can achieve the desired system radiated EMI goal without the use of a chassis shield. In this example, a system based on the ADuM140x that passes CISPR 22 Class B certification was chosen.

The starting point for this example is a 4-layer PCB with ground and power planes on inner layers. All reductions in EMI are relative to the emissions and noise from this 4-layer board. The CISPR 22 Class B standard was selected because it involves just two frequency ranges, but FCC Class B can be used as well, as shown in Figure 19. To meet CISPR 22 Class B (green line), the emissions within the frequency range of 30 MHz to 230 MHz must be below 30 dBμV/m, and emissions within the frequency range of 230 MHz to 1000 MHz must be below 37 dBμV/m, normalized to a 10 m antenna distance. To achieve these emissions levels, a few EMI reduction techniques can be employed.

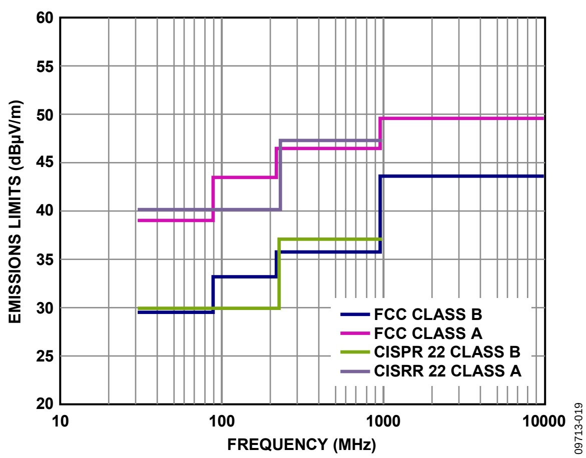

Figure 19. CISPR 22 and FCC Limits Normalized to 10 m Antenna Distance

The first example uses the standard PCB board without stitching capacitance to meet CISPR 22 Class B with four channels at 1 Mbps input signal frequency. As shown in Table 4, the ADuM1402 was tested at 1 Mbps data rate for the four channels. The 4-layer board used as a reference meets CISPR 22 Class B emissions for 3.3 V V_{DD} supplies. For 5 V V_{DD} supplies at 1 Mbps data rate, the ADuM1402 meets CISPR 22 Class A, but exceeds CISPR 22 Class B limits at the 30 MHz to 230 MHz range by 4 dBμV/m, and in the 230 MHz to 1000 MHz range exceeds Class B by 2 dBμV/m.

To reduce emissions to meet CISPR 22 Class B limits with four data channels at 1 Mbps, data was taken with the ADuM1402 using techniques in various board layouts and displayed in Table 5. Data at 5 V V_{DD} and 1 Mbps show that, to meet CISPR 22 Class B limits, only 2 dB to 4 dB reduction is needed; therefore, adding a 150 pF stitching capacitance reduces emissions 5 dB to 10 dB and more than meets the emissions limits for Class B.

Table 4. CISPR 22 Class A and Class B Emission Limits, Standard 4-Layer PCB, Four Channels at 1 Mbps

Requirements	3.3 V V_{DD}, 30 MHz to 230 MHz	3.3 V V_{DD}, 230 MHz to 1000 MHz	5 V V_{DD}, 30 MHz to 230 MHz	5 V V_{DD}, 230 MHz to 1000 MHz
4-Layer PCB Emissions	28 dB	36 dB	34 dB	39 dB
CISPR 22 Class A Limit	40 dB	47 dB	40 dB	47 dB
CISPR 22 Class B Limit	30 dB	37 dB	30 dB	37 dB
Required EMI Reduction to Meet CISPR 22 Class B	0 dB	0 dB	4 dB	2 dB

Table 5. Techniques to Reduce Emissions, 4-Layer PCB with added Stitching Capacitance, Four Channels at 1 Mbps

Techniques	3.3 V V_{DD}, 30 MHz to 230 MHz	3.3 V V_{DD}, 230 MHz to 1000 MHz	5 V V_{DD}, 30 MHz to 230 MHz	5 V V_{DD}, 230 MHz to 1000 MHz
Add 150 pF Stitching Capacitance	−5 dB	−7 dB	−7 dB	−10 dB
Add Another 150 pF Stitching Capacitance	−5 dB	0 dB	−6 dB	0 dB
Add Fence and Guard Rings	−1 dB	0 dB	−1 dB	0 dB
Available EMI Reduction	−11 dB	−7 dB	−14 dB	−10 dB

Table 6. CISPR 22 Class A and Class B Emission Limits, Standard 4-Layer PCB, Four Channels at 10 Mbps

Requirements	3.3 V V_{DD}, 30 MHz to 230 MHz	3.3 V V_{DD}, 230 MHz to 1000 MHz	5 V V_{DD}, 30 MHz to 230 MHz	5 V V_{DD}, 230 MHz to 1000 MHz
4-Layer PCB Emissions	45 dB	53 dB	54 dB	57 dB
CISPR 22 Class A Limits	40 dB	47 dB	40 dB	47 dB
CISPR 22 Class B Limits	30 dB	37 dB	30 dB	37 dB
Required EMI Reduction to Meet CISPR 22 Class B	15 dB	16 dB	24 dB	20 dB

Table 7. Techniques to Reduce Emissions, 4-Layer PCB with Added Stitching Capacitance, Four Channels at 10 Mbps

Techniques	3.3 V V_{DD}, 30 MHz to 230 MHz	3.3 V V_{DD}, 230 MHz to 1000 MHz	5 V V_{DD}, 30 MHz to 230 MHz	5 V V_{DD}, 230 MHz to 1000 MHz
Add 150 pF Stitching Capacitance	−8 dB	−24 dB	−11 dB	−25 dB
Add another 150 pF Stitching Capacitance	−7 dB	0 dB	−10 dB	−3 dB
Add Fence and Guard Rings	−1 dB	0 dB	−1 dB	0 dB
Available EMI Reduction	−16 dB	−24 dB	−22 dB	−28 dB

The second example is to meet CISPR 22 Class B with four channels at 10 Mbps input signal frequency. As shown in Table 6, the standard 4-layer ADuM1402 evaluation board without stitching capacitance was tested at a higher data rate of 10 Mbps for the four channels, and the results show the standard layout does not meet CISPR 22 Class A or Class B emissions. Using stitching capacitance, and possibly reducing supply voltages to 3.3 V, helps reduce the emissions levels.

The results of using these EMI reduction techniques are shown in Table 7 with their corresponding reduction in radiated emissions. Using all the techniques for 3.3 V V_{DD}, the required reduction is met for CISPR 22 Class B. Using all the techniques for 5 V V_{DD}, the results meet CISPR 22 Class A, but are still 2 dBμV/m above the limit at 30 MHz to 230 MHz. To meet CISPR 22 Class B limits at 10 Mbps for four channels, extend the blue line (standard board, 5 V) in Figure 16 to 400 pF by adding another 100 pF stitching capacitance to obtain an additional 5 dBμV/m to 6 dBμV/m of emissions reduction.

Emissions depend on the size of the transmitter side ground plane, as well as the spacing between ground and power planes. It is recommended to use larger transmitter side interplane capacitance areas where possible. Larger distances to the edges of the board and smaller distances between ground and power planes limit EMI. For small transmitter side ground planes, the use of via fence and interplane capacitance may help reduce emissions.

The allowed emissions levels for Class A are about 10 dB higher than for Class B. This allows additional flexibility in choosing the EMI mitigation techniques. With this example board, the Class A levels can be met with the addition of stitching capacitance alone.

The PCB related techniques are illustrated in Figure 20. This is a cutaway view where some of the structures have been removed for a clearer view of the underlying structures. Figure 20 clearly shows how the stitching capacitance and primary side fencing are implemented. It does not show interplane capacitive bypassing because that structure is too subtle to be shown in this view.

This illustration shows the stitching capacitors sharing a layer with the power. This is an elegant and compact solution, but it can restrict the available space for creating a capacitor because it partitions the power plane. If there is insufficient space to build a large enough capacitor in this plane, the stitching structure can be moved to its own board plane or share a signal plane. If a signal plane is used, care should be taken to avoid islands in the stitching structures. The stitching structures should always be close to the *i*Coupler isolator and should fill the gap when possible, regardless of which plane is used to implement them.

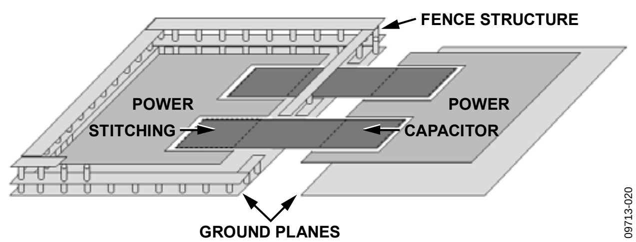

Figure 20. Capacitive Stitching and Via Fence Techniques

Refer to the Appendix A—PCB Example section for a description of the PCB structures implemented in the ADuM140x evaluation board. This appendix illustrates the structures described in this section with the values of coupling and bypass capacitance achieved.

GAP BOARD LAYOUT RESULTS

A concern raised in some applications with the input-to-output stitching layout is the performance of stitching capacitance when the certifying standards of PCBs in an application may require a wide gap between planes within a PCB layer. This requires a wide section of keep-out area in the internal layers of ground and power used to make the stitching capacitance. To test this, emissions chamber measurements were performed, where a 4-layer board was tested with a standard 0.4 mm spacing in the inner planes compared to 4-layer boards with a wide gap of 4 mm between the internal GND and V_{DD} layers, as shown in Figure 21, Figure 22 and Figure 23. Four different boards were tested: the standard board, a standard board with guard and fence added, a gap board, and a gap board with guard and fence added. The gap used was 4 mm wide, but for most applications, the gap spacing can be much smaller than this. The results are summarized in Figure 24 and Figure 25. Results show that there is 1 dB or less difference between the standard board and the gap board; therefore, the emissions can be controlled using the gap board layout. The guard board showed about a 2 dB improvement over the standard board for the emissions frequency range of 30 MHz to 230 MHz, which may indicate that the guarding improves the edge emissions at the gap because it helps cancel the 20h effect described in the Edge Emissions section.

For further information about the gap board, see Appendix A—PCB Examples, including layout drawings and clearance areas for vias and components in the overlap areas.

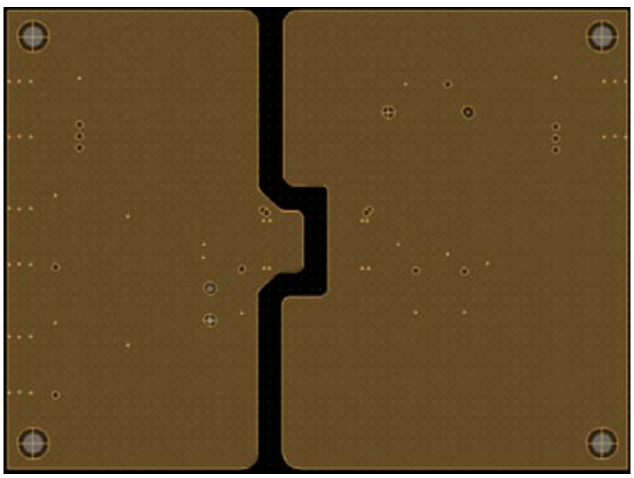

Figure 21. Gap Board Layout of ADuM1xxx with 4 mm Gap Showing GND Layer 2

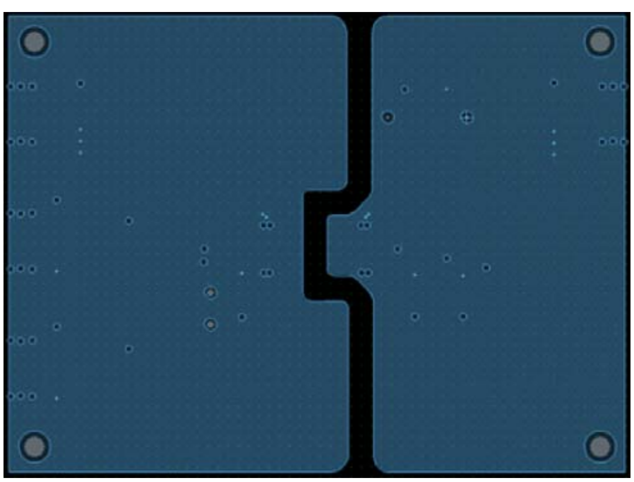

Figure 22. Gap Board Layout of ADuM1xxx with 4 mm Gap Showing V_{DD} Layer 3

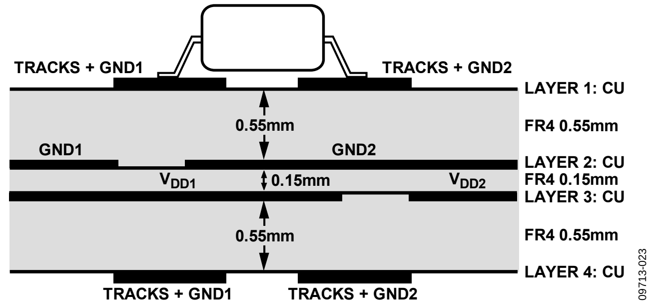

Figure 23. Cross Section of Gap Board Layout of ADuM1xxx with Dielectric of 0.15 mm Showing GND Layer 2 and V_{DD} Layer 3

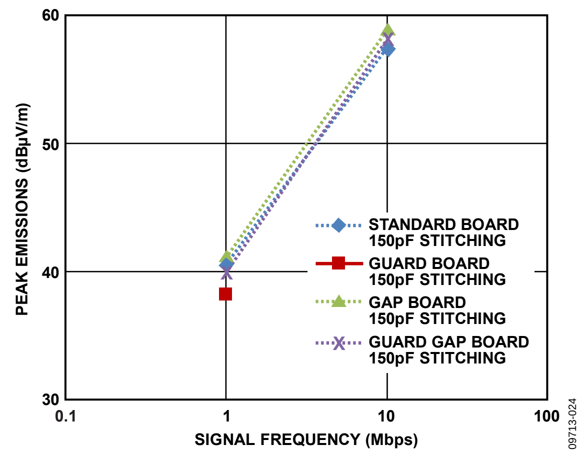

Figure 24. 5 V V_{DD} Peak Emissions for Gap Board Comparisons at Emissions Frequency Range of 30 MHz to 230 MHz

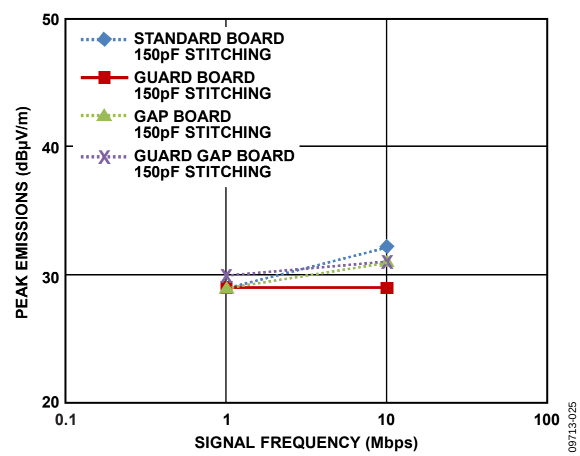

Figure 25. 5 V V_{DD} Peak Emissions for Gap Board Comparisons at Emissions Frequency Range of 230 MHz to 1000 MHz

CONCLUSIONS

Each method outlined in this application note addresses specific radiation sources and can be combined with the other techniques described to achieve the desired reductions in the associated emissions. Test boards easily meet CISPR 22 Class B standards with no external shielding by utilizing stitching capacitance and edge fencing. In addition, use of interplane decoupling capacitance in the ground and power planes yields a very quiet environment for precision measurement applications.

While this application note relies on data collected on the four-channel ADuM140x devices, the techniques are applicable across the *i*Coupler data isolator portfolio. For additional information on how to suppress EMI in *iso*Power integrated, isolated power products, refer to the AN-0971 Application Note, *Control of Radiated Emissions With* iso*Power Devices*.

Where low ac leakage is required, as in some medical applications, stitching capacitance may not be a viable solution. In other applications, there may be concern about stitching capacitance coupling noise from the high noise side to the low noise side. In this case, the use of interplane capacitance bypass and edge guarding with power and ground fills may help reduce the conducted noise. In applications where stitching capacitance cannot be used and other techniques are not effective, grounded metalized chassis enclosures may be the most practical solution for minimizing emissions.

APPENDIX A—PCB EXAMPLES

LOW NOISE PCB EXAMPLE

The standard evaluation board layout has been shown to meet CISPR 22 Class A limits (and FCC Class A limits, as shown in Figure 19). Like the standard board, the low noise board uses a 4-layer stack-up with Layer 1 to Layer 4 consisting of signal, ground, power, and signal. The ground and power layers are separated by 0.1 mm, which creates an interplane capacitance between Layer 2 and Layer 3 that helps bypass the 1 ns wide pulses used to drive the internal transformers. The ground layers have effectively created a dipole by the approximately 8 mm separation between GND1 and GND2. This dipole is driven by power supply noise created on the grounds by the high frequency transformer pulses, and can cause RF emissions.

The low noise evaluation board layout has been shown to meet CISPR 22 Class B limits (and FCC Class B limits, as shown in Figure 19). To reduce emissions, the low noise evaluation board has a layout to both shield the emissions and provide a small high frequency capacitive bypass across the isolated ground planes. Keep in mind that this stitching capacitance is on an inner layer in the PCB to avoid issues of creepage and clearance on the surface of the board. The low noise evaluation board uses a similar 4-layer stack-up as the standard evaluation board, but changes the spacing and position of the ground and power planes. As shown in Figure 27, GND Layer 2, the GND1 plane is extended to cover the gap under the ADuM140x. In Layer 2, GND1 to GND2 has a gap of 0.4 mm in FR4 material, which, according to Table 2, has a dielectric strength of 40 kV/mm (1000 V/mil), providing over 16 kV isolation. Similar to the ground layer, Figure 28 shows that the V_{DD2} plane was extended to go under the ADuM140x, with a gap of 0.4 mm in FR4 material between V_{DD1} and V_{DD2}.

Stitching capacitance can be calculated from the following equation:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

where:
ε_r = 4.5 from Table 2.
$\varepsilon_0 = 8.85 \times 10^{-12}$ Fm^{-1}, the permittivity of free space.
A is the overlap area of the stitching capacitance.
d is the separation between the ground and power planes.

For a separation of 0.1×10^{-3} m and area of 8 mm × 100 mm (0.0008 m^{-2}), the capacitance is about 300 pF. Cross barrier capacitance of at least 150 pF has been shown to be effective in reducing emissions (see Figure 14).

The limiting factor in the isolation voltage is the FR4 dielectric separation between Layer 2 and Layer 3 of 0.1 mm, which provides 4000 V isolation, enough for most applications. If more isolation is required, the dielectric between Layer 2 and Layer 3 can be made thicker, increasing the isolation, with a direct reduction in dielectric capacitance.

Next, the interplane capacitance on the primary side of the evaluation board is calculated. The close proximity of the ground and power planes to each other on the primary side of the application PCB forms this capacitance. In this example, 56 cm^2 ground and power planes form a low inductance capacitor of 2.2 nF. To take advantage of this bypass, the via connections between the part's pads and the power planes must be as large as possible so that there is minimal parasitic inductance between the part and the interplane capacitor.

$$C_{INTERPLANE} = \frac{A_{PRIMARY}(\varepsilon_0 \times \varepsilon_r)}{d}$$

$$C_{INTERPLANE} = \frac{5.6 \times 10^{-3}\,\text{m}^2 (8.854 \times 10^{-12}\,\text{F/m} \times 4.5)}{0.1 \times 10^{-3}\,\text{m}}$$

$$C_{INTERPLANE} = 2.2\ \text{nF}$$

A simplified low noise PCB schematic is shown in Figure 30.

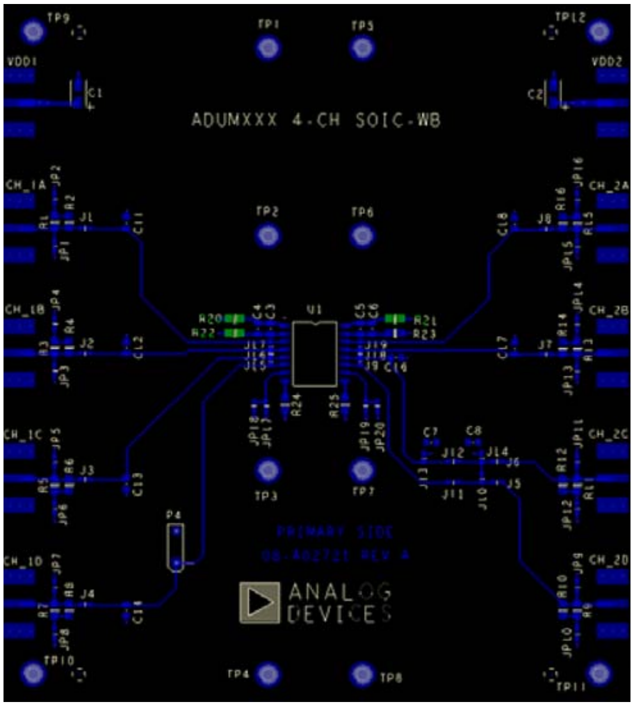

Figure 26. Top Layer 1 of 4-Layer Low Noise PCB Layout

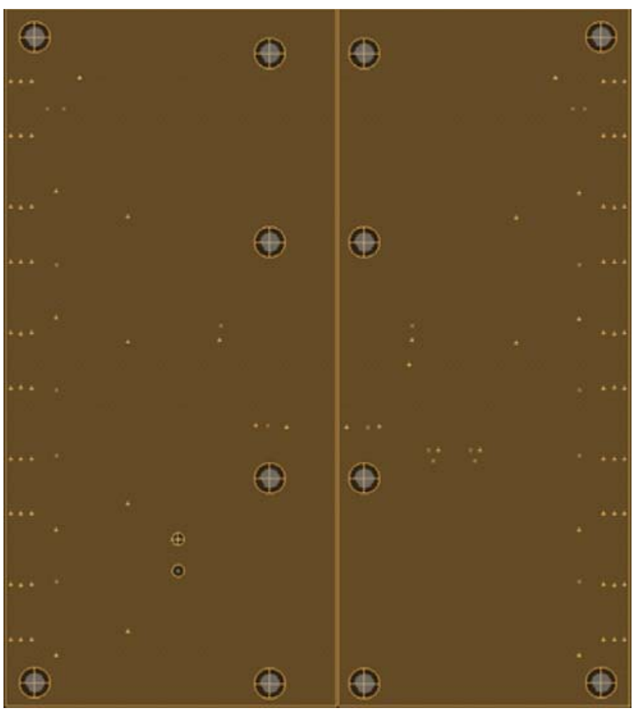

Figure 27. GND Layer 2 of 4-Layer Low Noise PCB Layout

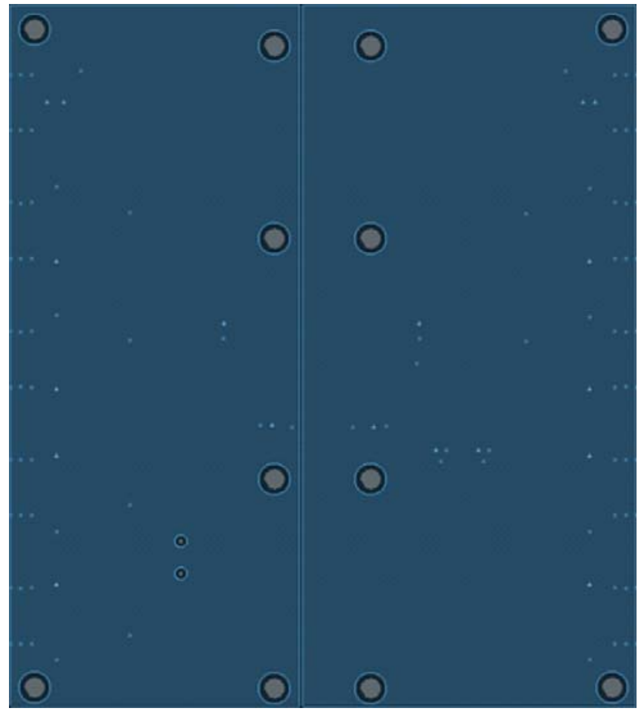

Figure 28. V_{DD} Layer 3 of 4-Layer Low Noise PCB Layout

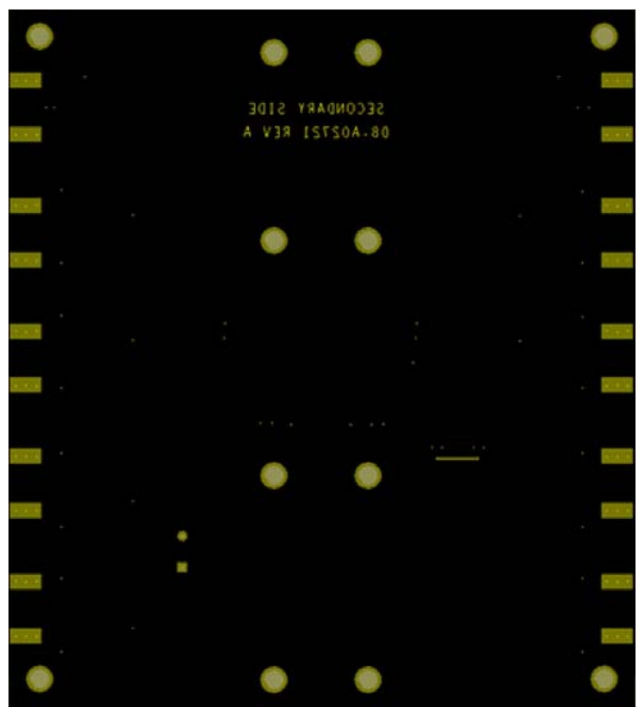

Figure 29. Bottom Layer 4 of 4-Layer Low Noise PCB Layout

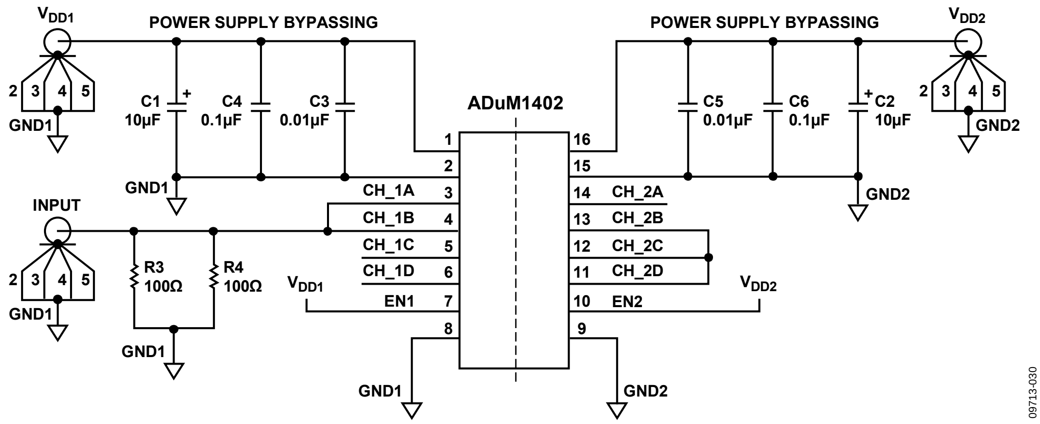

Figure 30. Simplified Low Noise PC Board Schematic

GAP PCB EXAMPLE

As described in the Gap Board Layout Results section, a wider gap layout may be required when the certifying standards of PCBs in an application may require a wider spacing between planes within a PCB layer. This requires a wide section of keep-out area in the internal layers of ground and power used to make the stitching capacitance. The proposed layout, using 150 pF overlap capacitance and allowing for a 4 mm gap in V_{DD} Layer 3, has a recommended FR4 dielectric thickness of 0.15 mm to be used to minimize board area. This proposed layout results in a reasonably sized overlap board space, leaving room for the other components. Calculations of the overlap capacitance and required board area can be made. The limiting factor for how much area is required for the overlap capacitance of 150 pF is the FR4 dielectric separation between Layer 2 and Layer 3. Dielectric capacitance can be calculated from the following equation:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

where:
ε_r = 4.5, the dielectric constant of FR4.
$\varepsilon_0 = 8.854 \times 10^{-12}$ Fm^{-1}, the permittivity of free space.
d is the separation between the ground and power planes.

For a 150 pF overlap capacitance, the area is

$$A = \frac{150\ \text{pF}}{\varepsilon_r \varepsilon_0} d = 3.75 \times 10^3 \times d$$

where d is the dielectric thickness in millimeters (mm).

For Figure 31, where the dielectric thickness is 0.15 mm, the area is calculated to be A = 560 mm^2.

The vertical board dimension is reduced by the two 4 mm keep-outs and the area to connect to the ADuM1xxx, leaving a reduced area to be divided into the two areas, with Width W, as shown in Figure 31.

Figure 32 illustrates the Side 1 and Side 2 locations where components can be placed in the overlap area. It is not recommended to place vias in the overlap area, because they need to be surrounded by a clearance area.

For a PC layout where vias are placed in the overlap area, there needs to be a keep-out area surrounding the vias. See Figure 33 for examples of the clearance areas for vias in the overlap area, where C = clearance spacing (same as the gap spacing) and r = radius of the total via and clearance area.

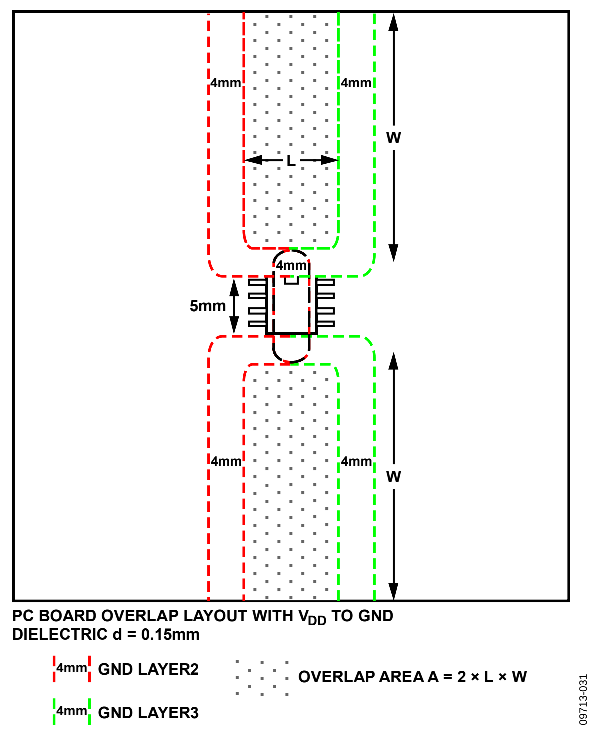

Figure 31. Layout of ADuM1xxx with V_{DD} to GND Dielectric of 0.15 mm

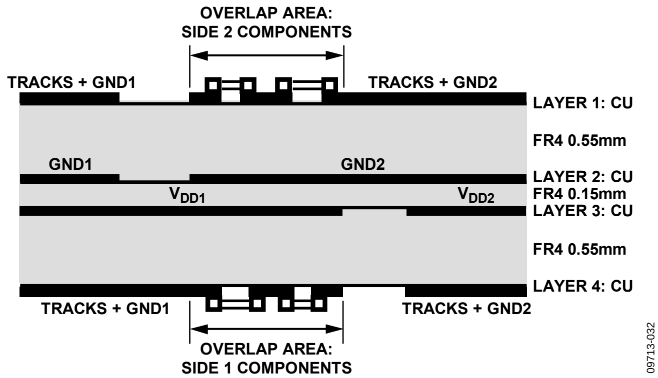

Figure 32. Cross Section of Proposed Layout of ADuM1xxx PCB Illustrating Side 1 and Side 2 Components on Overlap Area with V_{DD} to GND Dielectric of 0.15 mm

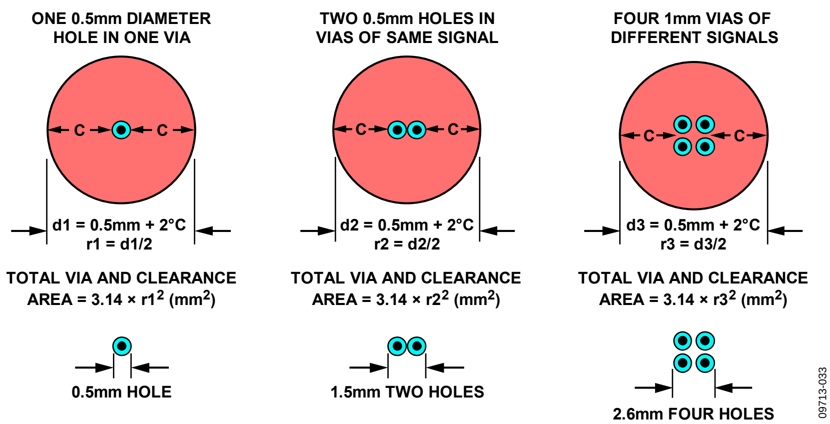

Figure 33. Vias in the Overlap Area Requiring a Clearance Area

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Archambeault, Bruce R. and James Drewniak. 2002. *PCB Design for Real-World EMI Control*. Boston: Kluwer Academic Publishers.

Gisin, Franz and Zorica Pantic-Tanner. 2001. "Minimizing EMI Caused by Radially Propagating Waves Inside High Speed Digital Logic PCBs." *Telecommunications in Modern Satellite, Cable and Broadcasting Service.* Nis, Yugoslavia.

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