CMOS, 80 MHz Monolithic 256 Word Power-Down Color Palette RAM-DACs

ADV477/ADV475

FEATURES

- Personal System/2* and VGA* Compatible
- 80, 66, 50 and 35 MHz Pipelined Operation
- ADV478/ADV471 (ADV®) Pin and Functional Compatible
- Power-Down Mode
- On-Board Voltage Reference
- Antisparkle Circuit
- Analog Output Comparators
- ADV477:
  - Triple 8-Bit D/A Converters
  - 256 × 24 Color Palette RAM
  - 15 × 24 Overlay Registers
- ADV475:
  - Triple 6-Bit D/A Converters
  - 256 × 18 Color Palette RAM
  - 15 × 18 Overlay Registers
- RS-343A/RS-170 Compatible Outputs
- Sync on all Three Channels
- Programmable Pedestal
- +5 V CMOS Monolithic Construction
- 44-Pin PLCC Package

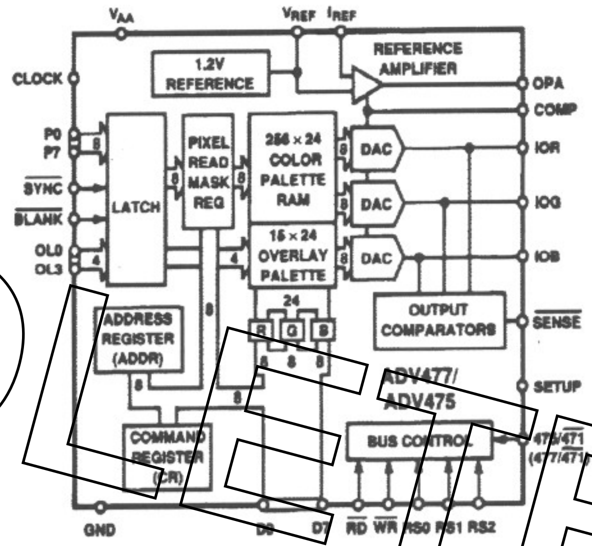
APPLICATIONS

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Laptop Computers
- Desktop Publishing

AVAILABLE CLOCK RATES

- 80 MHz
- 66 MHz
- 50 MHz
- 35 MHz

FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN NAMES IN PARENTHESES DENOTE ADV477

GENERAL DESCRIPTION

The ADV477 and ADV475 are pin-, functional-, and software-compatible RAM-DACs designed specifically for Personal System/2 (PS/2) compatible color graphics. They are a direct plug-in upgrade for the ADV478 and ADV471. Both support the existing 6-bit color VGA standard while also allowing for an upgrade path to 8-bit color resolution.

The ADV477 has a 256 × 24 color lookup table with triple 8-bit video D/A converters. The ADV475 has a 256 × 18 color lookup table with triple 6-bit video D/A converters. New features on the ADV477/ADV475 include an on-board 1.2 V voltage reference, analog output comparators for self diagnostics and debugging as well as a power-down or sleep mode.

The power-down mode allows the ADV477/ADV475 to be put into a sleep mode with significant reduction in power consumption. This is ideal for laptop computers that may occasionally require the optional ability to drive an analog RGB monitor, but whose design is dictated by a desire to minimize power consumption.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference. 15 overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc., at the hardware level. Also supported is a pixel read mask register and the ability to encode sync information on all three channels.

The ADV477/ADV475 generates RS343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

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ADV477/ADV475—SPECIFICATIONS

(V_{AA}[1] = 5 V; SETUP = 477/$\overline{471}$ = V_{AA}; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.)

Parameter	ADV477	ADV475	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution (Each DAC)	8	6	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity	±1	±0.25	LSB max	
Differential Nonlinearity	±1	±0.25	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale	
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	µA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS				
Output High Voltage, V_{OH}	2.4	2.4	V min	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	50	µA max	
Floating-State Leakage Capacitance	7	7	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	20	20	mA max	
Output Current				
White Level Relative to Black	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level Relative to Blank	0.95	0.95	mA min	Typically 1.44 mA, SETUP = V_{AA}
(Pedestal = 7.5 IRE)	1.90	1.90	mA max	
Black Level Relative to Blank	0	0	µA min	Typically 5 µA, SETUP = GND
(Pedestal = 0 IRE)	50	50	µA max	
Blank Level	6.29	6.29	mA min	Typically 7.62 mA
(Sync Enabled)	8.96	8.96	mA max	
Blank Level	0	0	µA min	Typically 5 µA
(Sync Disabled)	50	50	µA max	
Sync Level	0	0	µA min	Typically 5 µA
	50	50	µA max	
LSB size	69.1	279.68	µA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.5	+1.5	V max	
Output Capacitance, C_{OUT}	30	30	pF max	f = 1 MHz, I_{OUT} = 0 mA
Output Impedance, R_{OUT}	10	10	kΩ typ	
VOLTAGE REFERENCE				
Internal Voltage Reference	1.1/1.3	1.1/1.3	V min/V max	Typically 1.235 V
External Voltage Reference Range	1.14/1.26	1.14/1.26	V min/V max	
POWER SUPPLY				
Supply Voltage, V_{AA}	4.75/5.25	4.75/5.25	V min/V max	80 MHz and 66 MHz Parts
	4.50/5.50	4.50/5.50	V min/V max	50 MHz and 35 MHz Parts
Supply Current, I_{AA}				
Normal Operation	200	200	mA max	Typically 160 mA
Power Down Mode[3]	10	10	mA max	Typically 5 mA
Power Supply Rejection Ratio	0.5	0.5	%/% max	f = 1 kHz, COMP = 0.1 µF
DYNAMIC PERFORMANCE				
Clock and Data Feedthrough[4, 5]	−30	−30	dB typ	
Glitch Impulse[4, 5]	75	75	pV secs typ	
DAC to DAC Crosstalk[6]	−23	−23	dB typ	

NOTES

[1]±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.

[2]Temperature Range (T_{MIN} to T_{MAX}): 0°C to + 70°C.

[3]External Voltage/Current Reference disabled. Temperature: +25 °C to +70 °C. All digital inputs at 0.4 V.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.

[5]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.

[6]DAC-to-DAC Crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = 5 V; SETUP = 477/$\overline{471}$ = V_{AA}; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[3], unless otherwise noted.)

Parameter	80 MHz Version	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
f_{max}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	ns min	RS0–RS2 Setup Time
t_2	10	10	10	10	ns min	RS0–RS2 Hold Time
t_3[4]	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	5	ns min	Read Data Hold Time
t_7	10	10	10	10	ns min	Write Data Setup Time
t_8	10	10	10	10	ns min	Write Data Hold Time
t_9	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{10}	$6 \times t_{13}$	$6 \times t_{13}$	$6 \times t_{13}$	$6 \times t_{13}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{11}	3	3	3	3	ns min	Pixel and Control Setup Time
t_{12}	3	3	3	3	ns min	Pixel and Control Hold Time
t_{13}	12.5	15.15	20	28	ns min	Clock Cycle Time
t_{14}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{15}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{16}	30	30	30	30	ns max	Analog Output Delay
t_{17}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{18}[6]	13	13	20	28	ns max	Analog Output Settling Time
t_{19}	1	1	1	1	µs typ	SENSE Output Delay
t_{SK}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	$4 \times t_{13}$	$4 \times t_{13}$	$4 \times t_{13}$	$4 \times t_{13}$	ns min	Pipeline Delay

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 2a.

[2]±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.

[3]Temperature Range (T_{MIN} to T_{MAX}): 0°C to +70°C.

[4]t_3 and t_4 are measured with the load circuit of Figure 3 and are defined as the time required for an output to cross 0.4 V or 2.4 V.

[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and as such are independent of external bus loading capacitances.

[6]Settling time does not include clock and data feedthrough.

Specifications subject to change without notice.

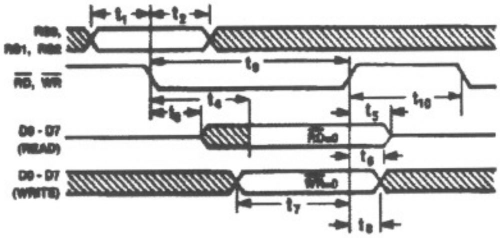


Figure 1. MPU Read/Write Timing

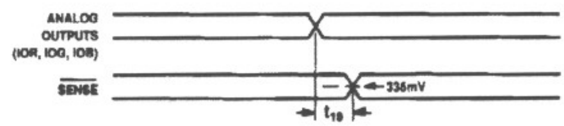
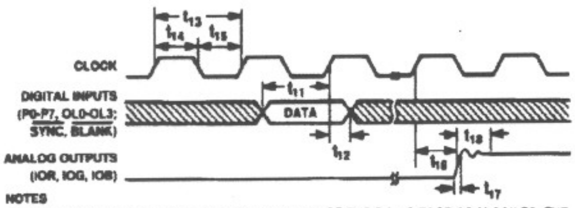


Figure 2b. Video Output vs. SENSE Timing



NOTES
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. SETTLING TIME MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1 LSB (ADV477) AN ±0.25 LSBs (ADV475).
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION

Figure 2a. Video Input/Output Timing

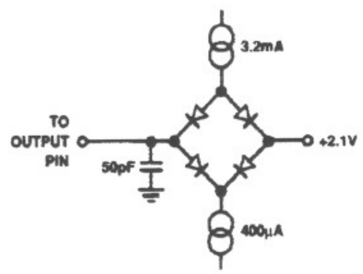


Figure 3. Load Circuit for Bus Access and Relinquish Time

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