AN-551
APPLICATION NOTE

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Power Management of the ADV7172/ADV7173 Video Encoder

INTRODUCTION

This application note describes the different power operating modes of the ADV7172/ADV7173 and how the device should be configured or used in order to use power as efficiently as possible.

THE THREE POWER OPERATING MODES AVAILABLE ON THE ADV7172/ADV7173

The ADV7172/ADV7173 has three power operating modes:

Normal Power Mode at 5 V or 3.3 V

When all DACs are switched on, the current consumed is set by R_{SET1} for the large DACs (DAC A, B, C), R_{SET2} for the small DACs (DAC D, E, F) and V_{REF}. See Tables I and II for the different current settings.

Low Power Mode

Low Power Mode is only available at an operating voltage of 5 V. It only takes effect when the large DACs (A, B, C) are switched on. This facility will reduce the average current consumed by each large DAC (which is powered on) by approximately 40%.

How Does Low Power Mode Work?

Considering each DAC as a group of current sources, when any current source has a DAC code of zero (i.e., off), the DAC current is switched to ground and current is consumed unnecessarily. If the current source is then switched off instead of being switched to ground, the current consumed can be reduced by approximately 40%.

Sleep Mode

Sleep Mode is available at 5 V and 3.3 V operation. The current consumed by the ADV7172/ADV7173 is typically less than 20 µA. This mode can be used while powering up or while configuring the registers.

Two Mode Registers allow control over Sleep Mode: Mode Register 2, "Sleep Mode Control" and Mode Register 6, "Power Up Sleep Mode." In Mode Register 2, Sleep Mode is enabled when the according bit (MR27) "Sleep Mode Control" is set to Logic 1 and disabled when it is set to Logic 0.

When enabled, the current consumption of the ADV7172/ADV7173 is typically less than 20 µA. If the device is set to operate in Sleep Mode and if Sleep Mode is disabled in setting the according bit (MR27) to Logic 0, the device will come out of Sleep Mode and resume normal operation.

Also, if the device is set to operate in Sleep Mode and a reset is applied, the device will come out of Sleep Mode and resume normal operation. This mode will only operate when Mode Register 6, "Power-Up Sleep Mode" is disabled (set to Logic 1), otherwise Sleep Mode is controlled by the PAL_NTSC and SCRESET/RTC pin.

Note that the I^2C interface still operates in Sleep Mode.

Mode Register 6

MR60 "Power-Up in Sleep Mode" allows the user to control powering up the device in Sleep Mode to facilitate low power consumption before the I^2C is initialized. The device will power up in Sleep Mode if the SCRESET/RTC pin and the NTSC_PAL pin are tied high and the "Power-Up Sleep Mode" control (MR60) is set to Enabled (set to a Logic 0). This bit is always set to 0 after powering up or after applying a reset.

When "Power-Up Sleep Mode" is disabled or set to a Logic 1, Sleep Mode control passes to Mode Register 2, "Sleep Mode Enable" control.

THERE ARE SEVERAL METHODS TO REDUCE POWER CONSUMPTION OF THE ADV7172/ADV7173

1. Operating Voltage: 5 V Low Power Mode
2. Operating Voltage: 3.3 V
3. Sleep Mode
4. Turn Off Unused DACs
5. External Buffering
6. TV Autodetect

Operating Voltage: 5 V Low Power Mode

Mode Register 1, Bit 6, "Low Power Mode Control" allows the Low Power Mode to be selected. Note, that Low Power Mode is only available at 5 V operation.

Low Power Mode will reduce the average current consumed by each DAC by approximately 40%.

In normal mode the current consumed is set by R_{SET1}, R_{SET2} and V_{REF}. In Low Power Mode this set current is reduced by approximately 40%. For each DAC the relationship between R_{SET1}/V_{REF} and R_{SET2}/V_{REF} and the output current is unchanged by this.

Operating Voltage: 3.3 V
Ideal or optimum performance is achieved when the device is operated at 3.3 V and DAC A, B, C (large DACs) are set to an output current of:

$$I_{OUT} = 18\ mA$$

where

$R_{SET1} = 300\ \Omega$
$R_{SET2} = 600\ \Omega$
$R_{LOAD} = 75\ \Omega$ (Single Terminated Load)

Sleep Mode
Is available at 5 V and 3.3 V operation.

The current consumption of the ADV7172/ADV7173 is typically less than 20 µA.

As mentioned before, this mode can be used while powering up the device or while configuring the registers. See Sleep Mode section for details on how to operate Sleep Mode.

Turn Off Unused DACs
It is recommended that whenever a DAC is not used, it should be switched off.

This is done in Mode Register 1, where each DAC can be individually powered off. Refer to Table I and Table II for further details.

External Buffering
External buffering is another way to reduce power consumption. Whereas DAC D, E, F (small DACs) always need buffering, buffering on DACs A, B, C is optional (when DAC D, E, F are not used). In the shown configuration the DACs A, B, C are running at 18 mA, which is half of their full current capability. This allows a reduction in power dissipation by 50% in the current that these DACs consume.

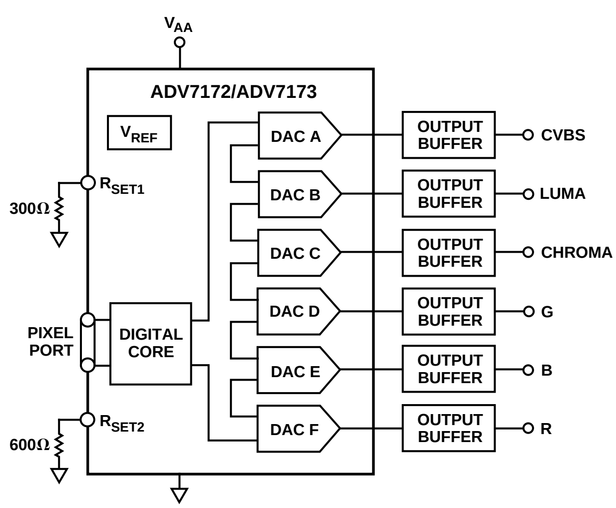

Figure 1. Output DAC Buffering Configuration

The resistors are given the following values:

$R_{SET1} = 300\ \Omega$
$R_{SET2} = 600\ \Omega$
$R_{LOAD} = 75\ \Omega$ Single Terminated

It is further recommended to use this configuration at an operating voltage of 3.3 V. This allows optimum DAC performance and adds extra isolation on the video outputs.

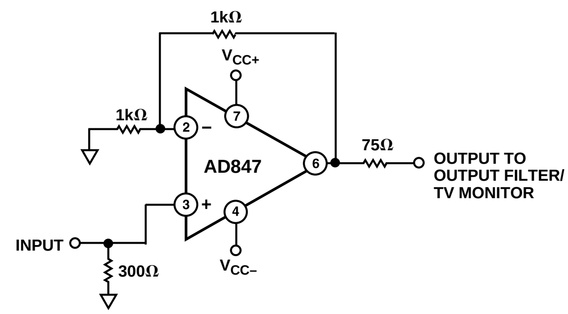

Figure 2. Recommended DAC Output Buffer Using an Op Amp

TV Autodetect
This feature allows the user to determine whether or not the DACs are correctly terminated. This facility is available for DACs A, B, C since unconnected (not used) DACs increase power consumption.

Mode Register 6 allows automatic detection of unterminated DACs:

1. The "DAC Termination Mode" control allows to select between correct 75 Ω or 150 Ω termination.

Note that double terminated 75 Ω becomes 37.5 Ω (i.e., 75 Ω on the DAC end and 75 Ω on the TV end) and 150 Ω becomes 75 Ω. For this reason the Autodetect facility cannot operate if the large DACs are buffered, since buffering results in a fixed termination, regardless if correctly or incorrectly terminated at the buffer output.

Mode Register 6 "DAC Termination Mode" control (Bit 4) allows the user to select between two Autodetect Termination modes:

1 × Mode = 75 Ω Termination (Single-Terminated)
2 × Mode = 150 Ω Termination (Single-Terminated)

Mode Register 6 "Comp Autodetect Mode" control (Bit 3) and "Luma Autodetect" control (Bit 2) allow the choice between two functions:

Mode0
Correct termination of the DAC is checked and indicated with the according Status bit set to "1" or when using the Evaluation Software, Mode Register 6 (Autodetect Status) a green button indicates correct termination.

If not correctly terminated, the user has the choice to power down the DAC or not. This can be done by using Mode Register 1.

Mode1

Correct termination of the DAC is checked and indicated with the according Status bit set to "1" or when using the Evaluation Software, Mode Register 6 (Autodetect Status) a green button indicates correct termination.

If not correctly terminated, the DAC is automatically powered down.

Correct termination is checked at intervals of one frame to decide whether or not the DACs are to be powered down.

SETTINGS FOR R_{SET1}, R_{SET2}, R_{LOAD}

Operating Voltage: 5 V/Normal Mode

The values for R_{SET1} and R_{SET2} determine what current will be consumed by each DAC and, therefore, what power will be consumed.

The current consumed is calculated as:

$I_{OUT} = (V_{REF} \times K)/R_{SET}$
$V_{OUT} = I_{OUT} \times R_{LOAD}$
$V_{REF} = 1.235\ V$
$K = 4.2146$

DAC A, B, C (Large DACs)

R_{SET2} is used for the small DACs and has no effect on the output current of the large DACs.

$I_{OUT} = 34.7$ mA — $R_{SET1} = 150\ \Omega$
$R_{LOAD} = 75\ \Omega$ (Single-Terminated)

$I_{OUT} = 5$ mA — $R_{SET1} = 1041\ \Omega$
$R_{LOAD} = 262.5\ \Omega$
(Buffered, Scaled Output Load)

See Table I and Table II for further details.

DAC D, E, F (Small DACs)

R_{SET1} is used for the large DACs and has no effect on the output current of the small DACs.

$I_{OUT} = 8.66$ mA — $R_{SET2} = 600\ \Omega$
$R_{LOAD} = 150\ \Omega$

$I_{OUT} = 5$ mA — $R_{SET2} = 1041\ \Omega$
$R_{LOAD} = 262.5\ \Omega$
(Buffered, Scaled Output Load)

See Table I and Table II for further details

Operating Voltage: 3.3 V/Normal Mode

The same settings for R_{SET1} and R_{SET2} apply for 3.3 V operation as shown above for 5 V operation.

3.3 V operation will reduce the power dissipation due to the $V \times I = P$ formula, i.e., the current is unchanged while the voltage decreases from 5 V to 3.3 V.

JUNCTION TEMPERATURE

It is important to keep in mind that at no time the maximum junction temperature of 110°C should be exceeded:

Junction Temperature = $[V_{AA}\ (\Sigma \text{ of } I_{OUT} + I_{CCT}) \times \theta_{JA}] + 70°C$

I_{CCT} = Circuit Current or Digital Supply Current
= Continuous Current Required to Drive the Device

I_{CCT} = 78 mA at $V_{AA} = 5$ V

I_{CCT} = 40 mA at $V_{AA} = 3.3$ V

I_{DAC} = Total Current to Drive All DACs
= 10 mA + (Σ of the Average Currents Consumed by Each DAC)
= 10 mA + (Σ of I_{OUT} of Each DAC)

I_{OUT} = Average Current Consumed by DAC

θ_{JA} = Junction-to-Ambient Thermal Resistance 54.6°C/W in Still Air On a Four-Layer PCB

θ_{JC} = Junction-to-Case Thermal Resistance 16.7°C/W in Still Air On a Four-Layer PCB

V_{AA} = Supply Voltage

$P_{TOTAL} = V_{AA} \times I_{Total}$

$I_{TOTAL} = I_{CCT} + \Sigma \text{ of } I_{OUT}$

Table I. DAC Current Consumption

Supply Voltage	DAC Buffering	Low Power ON	I_{OUT} DAC A (mA)	I_{OUT} DAC B (mA)	I_{OUT} DAC C (mA)	I_{OUT} DAC D (mA)	I_{OUT} DAC E (mA)	I_{OUT} DAC F (mA)	Junction Temp Degrees Celsius	DAC Output Configuration	I_{CCT} (mA)	I_{DAC} (mA)	I_{TOTAL} (mA)	P_{TOTAL} (mW)
5 V	No	No	34.7	34.7	34.7	8.66	8.66	8.66	126.8	*Not Allowed*	78	140.08	208.08	1040.4
	No	Yes	20.82	20.82	20.82	OFF	OFF	OFF	108.3	Allowed	78	72.46	140.46	702.3
	Yes	No	5	5	5	5	5	5	99.5	Allowed	78	40	108	540
	Yes	Yes	3	3	3	OFF	OFF	OFF	93.8	Allowed	78	19	87	435
	No	No	OFF	34.7	34.7	8.66	8.66	8.66	117.3	*Not Allowed*	78	105.38	173.38	866.9
	No	Yes	OFF	20.82	20.82	OFF	OFF	OFF	102.7	Allowed	78	51.64	119.64	598.2
	Yes	No	OFF	5	5	5	5	5	98.1	Allowed	78	35	103	515
	Yes	Yes	OFF	3	3	OFF	OFF	OFF	92.9	Allowed	78	16	84	420
	No	No	OFF	OFF	34.7	8.66	8.66	8.66	107.9	Allowed	78	70.68	138.68	693.4
	No	Yes	OFF	OFF	20.82	OFF	OFF	OFF	97	Allowed	78	30.82	98.82	494.1
	Yes	No	OFF	OFF	5	5	5	5	96.8	Allowed	78	30	98	490
	Yes	Yes	OFF	OFF	3	OFF	OFF	OFF	92.1	Allowed	78	13	81	405
	No	No	OFF	OFF	OFF	8.66	8.66	8.66	98.3	Allowed	78	35.98	103.98	519.9
	No	Yes	OFF	OFF	OFF	OFF	OFF	OFF						
	Yes	No	OFF	OFF	OFF	5	5	5	95.4	Allowed	78	25	93	465
	Yes	Yes	OFF	OFF	OFF	OFF	OFF	OFF						
	No	No	OFF	OFF	OFF	OFF	8.66	8.66	96	Allowed	78	27.32	95.32	476.6
	No	Yes	OFF	OFF	OFF	OFF	OFF	OFF						
	Yes	No	OFF	OFF	OFF	OFF	5	5	94	Allowed	78	20	88	440
	Yes	Yes	OFF	OFF	OFF	OFF	OFF	OFF						
	No	No	OFF	OFF	OFF	OFF	OFF	8.66	93.7	Allowed	78	18	86.66	433.3
	No	Yes	OFF	OFF	OFF	OFF	OFF	OFF						
	Yes	No	OFF	OFF	OFF	OFF	OFF	5	92.7	Allowed	78	15	83	415
	Yes	Yes	OFF	OFF	OFF	OFF	OFF	OFF						
	No	No	34.7	34.7	34.7	8.66	8.66	OFF	124.4	*Not Allowed*	78	131.42	199.42	997.1
	No	Yes	20.82	20.82	20.82	OFF	OFF	OFF	108.3	Allowed	78	72.46	140.46	702.3
	Yes	No	5	5	5	5	5	OFF	98.1	Allowed	78	35	103	515
	Yes	Yes	3	3	3	OFF	OFF	OFF	93.8	Allowed	78	19	87	435
	No	No	34.7	34.7	34.7	8.66	OFF	OFF	122.1	*Not Allowed*	78	122.76	190.76	953.8
	No	Yes	20.82	20.82	20.82	OFF	OFF	OFF	102.7	Allowed	78	51.64	119.64	598.2
	Yes	No	5	5	5	5	OFF	OFF	96.8	Allowed	78	30	98	490
	Yes	Yes	3	3	3	OFF	OFF	OFF	93.8	Allowed	78	19	87	435
	No	No	34.7	34.7	34.7	OFF	OFF	OFF	119.7	*Not Allowed*	78	114.1	182.1	910.5
	No	Yes	20.82	20.82	20.82	OFF	OFF	OFF	108.3	Allowed	78	72.46	140.46	702.3
	Yes	No	5	5	5	OFF	OFF	OFF	95.4	Allowed	78	25	93	465
	Yes	Yes	3	3	3	OFF	OFF	OFF	93.8	Allowed	78	19	87	435
	No	No	34.7	34.7	OFF	OFF	OFF	OFF	110.2	Allowed	78	79.4	147.4	737
	No	Yes	20.82	20.82	OFF	OFF	OFF	OFF	102.7	Allowed	78	51.64	119.64	598.2
	Yes	No	5	5	OFF	OFF	OFF	OFF	94	Allowed	78	20	88	440
	Yes	Yes	3	3	OFF	OFF	OFF	OFF	92.9	Allowed	78	16	84	420
	No	No	34.7	OFF	OFF	OFF	OFF	OFF	100.8	Allowed	78	44.7	112.7	563.5
	No	Yes	20.82	OFF	OFF	OFF	OFF	OFF	96.9	Allowed	78	30.82	98.82	494.1
	Yes	No	5	OFF	OFF	OFF	OFF	OFF	92.7	Allowed	78	15	83	415
	Yes	Yes	3	OFF	OFF	OFF	OFF	OFF	92.1	Allowed	78	13	81	405

Table II. DAC Current Consumption

Supply Voltage	DAC Buffering	I_{OUT} DAC A (mA)	I_{OUT} DAC B (mA)	I_{OUT} DAC C (mA)	I_{OUT} DAC D (mA)	I_{OUT} DAC E (mA)	I_{OUT} DAC F (mA)	Junction Temp Degrees Celsius	I_{CCT} (mA)	I_{DAC} (mA)	I_{TOTAL} (mA)	P_{TOTAL} (mW)
3.3 V	No	34.7	34.7	34.7	8.66	8.66	8.66	100.6	40	140.08	170.08	561.3
	Yes	5	5	5	5	5	5	82.6	40	40	70	231
	No	OFF	34.7	34.7	8.66	8.66	8.66	94.4	40	105.38	135.4	446.8
	Yes	OFF	5	5	5	5	5	81.7	40	35	65	214.5
	No	OFF	OFF	34.7	8.66	8.66	8.66	88.1	40	70.68	100.7	332.3
	Yes	OFF	OFF	5	5	5	5	80.8	40	30	60	198
	No	OFF	OFF	OFF	8.66	8.66	8.66	81.9	40	35.98	65.9	217.5
	Yes	OFF	OFF	OFF	5	5	5	79.9	40	25	55	181.5
	No	OFF	OFF	OFF	OFF	8.66	8.66	80.3	40	27.32	57.32	189.2
	Yes	OFF	OFF	OFF	OFF	5	5	79	40	20	50	165
	No	OFF	OFF	OFF	OFF	OFF	8.66	78.8	40	18.66	48.66	160.6
	Yes	OFF	OFF	OFF	OFF	OFF	5	78.1	40	15	45	148.5
	No	34.7	34.7	34.7	8.66	8.66	OFF	99.1	40	131.42	161.42	532.7
	Yes	5	5	5	5	5	OFF	81.7	40	35	65	214.5
	No	34.7	34.7	34.7	8.66	OFF	OFF	97.5	40	122.76	152.8	504.2
	Yes	5	5	5	5	OFF	OFF	80.8	40	30	60	198
	No	34.7	34.7	34.7	OFF	OFF	OFF	95.9	40	114.1	144.1	475.5
	Yes	5	5	5	OFF	OFF	OFF	79.9	40	25	55	181.5
	No	34.7	34.7	OFF	OFF	OFF	OFF	89.7	40	79.4	109.4	361.02
	Yes	5	5	OFF	OFF	OFF	OFF	79	40	20	50	165

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