AN-862
APPLICATION NOTE

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SD RGB Processing Using the ADV7181B

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INTRODUCTION

The Analog Devices, Inc., ADV7181B decoder was designed primarily for support of standard definition composite, S-Video, and component video input formats. All PAL, SECAM, and NTSC formats are supported. The part does not support the European SCART RGB standard with fast blanking. European SCART RGB requires the simultaneous digitization of RGB and CVBS inputs with the ability to process data from either input, dependent on the level of the fast blank signal that has been applied. The fast blank is used as the control signal used to switch processing on a pixel by pixel basis. In this mode, synchronization information is always extracted from the CVBS input. This form of RGB support is termed dynamic fast blank; when SD RGB support is required without the need for pixel by pixel switching, this is termed static fast blank. The ADV7181B can be configured to support standard definition RGB input modes with static fast blank.

HARDWARE CONFIGURATION

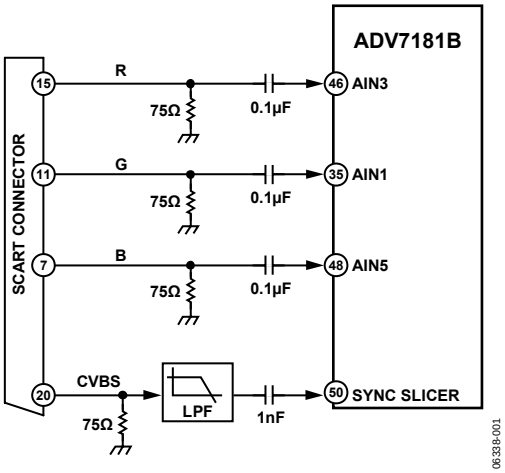

Figure 1. Hardware Configuration

Figure 1 shows a recommended hardware configuration. Recommended inputs are AIN3 (Pin 46) for red, AIN1 (Pin 35) for green, and AIN5 (Pin 48) for blue. The script configuration uses manual muxing of these inputs to the appropriate ADC; alternative input configurations are possible but not advised, and subsequent processing paths in the color space converted block would also require reconfiguration. Synchronization needs to be extracted from the synchronous CVBS input. Note that the CVBS input most likely contains color burst and active video data. In this case, the only requirement is the extraction of the synchronization data; some aspects of the CVBS signal, if present at the sync slicer, may cause false or incorrect extraction. In particular, color burst information extending below the blanking level causes issues. For that reason, the insertion of a low-pass filter is advised to attenuate the color burst and any other active video elements that may cause sync extraction issues. Figure 2 shows a graphical representation of the filter operation. A basic single order filter with a 3 dB point at 100 kHz should be sufficient to perform this function. The filtered CVBS input is fed to the internal sync slicer via Pin 50 (shown in the data sheet as a no connect). Output data from the decoder is available in 8-bit or 16-bit output formats with embedded and/or external synchronization. In some circumstances, the synchronization information is present in the green channel; in these cases, a configuration as shown in Figure 3 can be implemented.

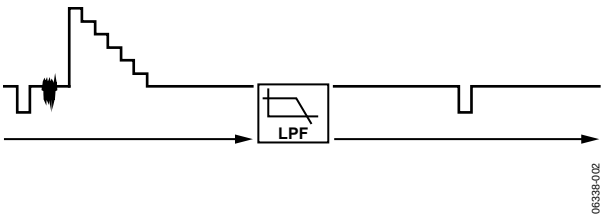

Figure 2. Low-Pass Filter Removing Color Burst and Active Video Data

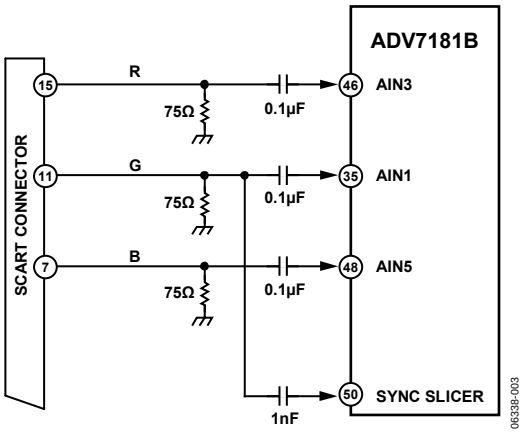

Figure 3. Hardware Configuration Where Synchronization is Embedded on the G Input

INTERNAL PROCESSING

Manual muxing routes the input RGB signals to the individual ADCs and then to the special RGB processing block. User controls allow for individual gain and offset adjustments. The block includes a programmable color space converter where the RGB inputs are converted to component YPrPb format and subsequently to the back end output formatter. The filtered CVBS input with synchronization is processed through the special RGB mode sync slicer block. Sync inputs are sampled on the falling edge; adjustments on the slice level are available, but for nominal noise free inputs, this should not be a requirement. Figure 4 outlines the slice level adjustment control.

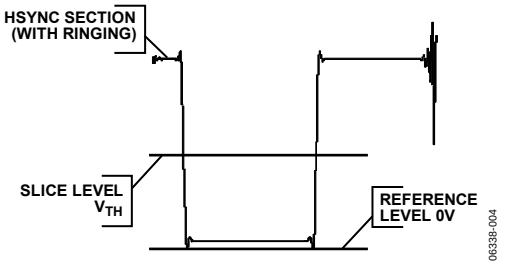

Figure 4. Sync Slice Level Adjustment

SOFTWARE CONFIGURATION

An example of a fixed function control script is provided in this section. All values provided are in hexadecimal, the first value is the device ID, in this case 0x42 for the decoder. The next value represents the subaddress within the decoder and, finally, the value to be programmed; the write sequence must be implemented as shown.

Sample Script

ADV7181B SCART RGB 8-bit 422 out (625i) using 28.6363 MHz Xtal

42 01 88;	Disable HS PLL, providing faster response for high quality timebase inputs
42 05 00;	Enable the special SD RGB processing block
42 06 0F;	Set the input standard for 625i with 2× input oversampling
42 1D 40;	Enable 28 MHz crystal
42 0F 40;	TRAQ (reset the internal timing blocks)
42 31 02;	Clear NEWAV_MODE, SAV/EAV to suit ADV video encoders (only required when back-to-back with encoder)
42 3A 10;	Set latch clock (optimized ADC latch clock setting for special mode)
42 3D C3;	MWE enable manual window (allow manual control of the blank and burst sample windows)
42 3F E4;	BGB to 36 (adjust the sampling window for blank and burst)
42 52 00;	Enable the special mode color space converter
42 53 00;	Convert from SD RGB to SD YPrPb
42 54 07;	Convert from SD RGB to SD YPrPb
42 55 0C;	Convert from SD RGB to SD YPrPb
42 56 94;	Convert from SD RGB to SD YPrPb
42 57 89;	Convert from SD RGB to SD YPrPb
42 58 48;	Convert from SD RGB to SD YPrPb
42 59 08;	Convert from SD RGB to SD YPrPb
42 5A 00;	Convert from SD RGB to SD YPrPb
42 5B 7A;	Convert from SD RGB to SD YPrPb
42 5C E1;	Convert from SD RGB to SD YPrPb
42 5D 00;	Convert from SD RGB to SD YPrPb
42 5E 19;	Convert from SD RGB to SD YPrPb
42 5F 48;	Convert from SD RGB to SD YPrPb
42 60 08;	Convert from SD RGB to SD YPrPb
42 61 00;	Convert from SD RGB to SD YPrPb
42 62 20;	Convert from SD RGB to SD YPrPb
42 63 03;	Convert from SD RGB to SD YPrPb
42 64 A9;	Convert from SD RGB to SD YPrPb
42 65 1A;	Convert from SD RGB to SD YPrPb
42 66 B8;	Convert from SD RGB to SD YPrPb
42 67 03;	Convert from SD RGB to SD YPrPb
42 68 00;	Convert from SD RGB to SD YPrPb
42 6A 80;	Enable 27 MHz LLC output
42 6B C3;	Select the 8-bit YPrPb from the special mode output formatter
42 73 D0;	Manual gain control
42 74 B4;	GAIN setting
42 7B 06;	Special mode write to ensure 656 compliant SAV/EAV codes
42 C3 C9;	Mux AIN1 to ADC0; mux AIN3 to ADC1
42 C4 8D;	Set adc_sw_man_en to 1, mux AIN5 to ADC2
42 85 1A;	Enable the sync input mode on Pin 50
42 86 02;	Enable the internal special mode sync slicer block
42 B3 FE;	SCART RGB write
42 C9 0C;	Enable DDR Mode, enable DDR_I2C_RC_First (writing this sequence ensures a 27 MHz output clock)
42 0E 80;	Enable design block tweak mode
42 58 ED;	Internal timing optimization, not user adjustable
42 90 C9;	Internal timing optimization, not user adjustable
42 91 40;	internal timing optimization, not user adjustable
42 92 3C;	Internal timing optimization, not user adjustable
42 93 CA;	Internal timing optimization, not user adjustable
42 94 D5;	Internal timing optimization, not user adjustable
42 CF 7C;	Internal timing optimization, not user adjustable
42 D0 4E;	Internal timing optimization, not user adjustable
42 D6 DD;	Internal timing optimization, not user adjustable
42 E5 51;	Internal timing optimization, not user adjustable
42 0E 00;	Close design block

USER CONTROLS

This section of the application note outlines the special mode user controls that are not documented within the open market data sheet.

GAIN_MAN Manual Gain Control Enable, Address 0x73, [7]

Table 1.

GAIN_MAN	Description
0 (default)	
1	The gains for the three channels are set by A_GAIN[9:0], B_GAIN[9:0], and C_GAIN[9:0]

A_GAIN[9:0] Manual Gain Value for Channel A, Address 0x73, [5:0]; Address 0x74, [7:4]

Table 2.

A_GAIN[9:0]	Description
xx xxxx xxxx	Sets the manual gain for the signal in Channel A

B_GAIN[9:0] Manual Gain Value for Channel B, Address 0x74, [3:0]; Address 0x75, [7:0]

Table 3.

B_GAIN[9:0]	Description
xx xxxx xxxx	Sets the manual gain for the signal in Channel B

C_GAIN[9:0] Manual Gain Value for Channel C, Address 0x75, [1:0]; Address 0x76, [7:0]

Table 4.

C_GAIN[9:0]	Description
xx xxxx xxxx	Sets the manual gain for the signal in Channel C

A_OFFSET[9:0] Channel A Offset, Address 0x77, [5:0]; Address 0x78, [7:4]

Table 5.

A_OFFSET[9:0]	Description
0x3FF	Adds value to digital data. Double buffering and I²C® sequencing applies by default.

Note: To change the A_OFFSET[9:0] value, Register 0x77 and Register 0x78 must be written to in this order with no other I²C access in between.

B_OFFSET[9:0] Channel B Offset, Address 0x78, [3:0]; Address 0x79, [7:2]

Table 6.

B_OFFSET[9:0]	Description
0x3FF	Adds value to digital data. Double buffering and I²C sequencing applies by default.

Note: To change the B_OFFSET[9:0] value, Register 0x78 and Register 0x79 must be written to in this order with no other I²C access in between.

C_OFFSET[9:0] Channel C Offset, Address 0x79, [1:0]; Address 0x7A, [7:0]

Table 7.

C_OFFSET[9:0]	Description
0x3FF	Adds value to digital data. Double buffering and I²C sequencing applies by default.

Note: To change the C_OFFSET[9:0] value, Register 0x79 and Register 0x7A must be written to in this order with no other I²C access in between.

SOG_SYNC_LEV[4:0] Embedded Sync Trigger Level, Address 0x3C, [7:4]

The SOG_SYNC_LEV[4:0] bits allow the user to set the analog trigger threshold for the sync detection.

$$V_{TH} = 300\,\text{mV} \times \frac{SOG\_SYNC\_LEV[4:0]}{32} \quad (1)$$

The trigger voltage is measured relative to the lowest analog voltage level of the incoming video signal. For standard video signals, this is the bottom of the horizontal sync.

VID_STD[3:0], Video Standard, Address 0x06, [3:0]

Table 8.

Code	Input Video	Output Resolution	Comment
1110	SD 2×1 525i	720 × 480	SD RGB NTSC
1111	SD 2×1 625i	720 × 526	SD RGB PAL/SECAM

OUTPUT FORMAT SELECTION

8-bit/16-bit, 656-/601-compliant output formats are available. Standard output configuration controls are not available when working in the special SD RGB support mode. The available controls are detailed in this section.

CLK_2X_SEL at Address 0x6A (Bit 7) should always be set high to enable 27 MHz clock.

SPOP[3:0] at Address 0x6B (Bit 0 to Bit 3) should always be set to 0x03, enabling 16-bit output.

If 8-bit output is required, the following writes need to be implemented in addition to those described above:

- DDR_EN at Address 0xC9 (Bit 3) should be set to one.
- DDR_I2C_RC at Address 0xC9 (Bit 2) should be set to one.