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APPLICATION NOTE

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Manual Scaling in the ADV7186

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INTRODUCTION

Video decoders capable of video signal processing are in high demand with video product consumers for three reasons. The first reason is the ability to produce output resolution that is completely different from the input resolution provided at source. The second reason is the ability of the signal to pass through the input video resolution unaltered. The third reason for this high demand is the ability to eliminate ringing or blurring in the output video data.

Scaling is the technique used to alter video resolution input at the output. Changing to a much higher video output resolution using a low video input resolution is upscaling.

Downscaling is the ability to modify high video input resolution to a lower output video resolution to satisfy the backend device, such as panels (like LCDs, for example), without the need for external memory.

This application note describes the automatic and manual scaling algorithm in the ADV7186 focusing primarily on manual scaling. This application note only considers standard input video formats.

HOW DOES SCALING WORK?

The ADV7186 is a video decoder with video signal processing capability that offers upscaling/downscaling of the input video resolution while eliminating ringing and blurring of video data. The ADV7186 includes an Analog Devices, Inc., Scaler Algorithm that provides very high quality video at the output using only internal memory.

The scaling of the input video to the desired output resolution is shown in the block diagram in Figure 1. The input video could be NTSC or PAL video input or possibly a progressive video input fed to the scaler block in the ADV7186. For the NTSC/PAL input, the de-interlacer block provides the video data to the scaler block. For the progressive video input, the de-interlacer block is not used; instead, the path of the video data is through the scaler block.

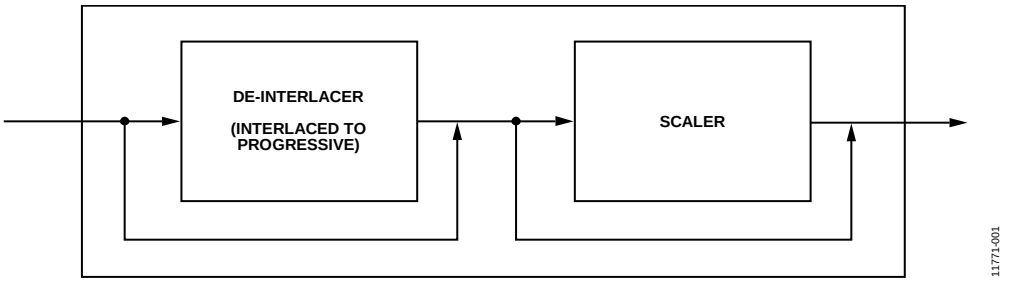

Figure 1. ADV7186 Video Signal Processing Simplified Schematic

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REVISION HISTORY

9/13—Revision 0: Initial Version

THE STANDARD INPUT VIDEO FORMATS

Table 1 lists some of the standard input video formats. The VID_STD register and the PRIM_MODE register both define the standard input video format (VID_STD, Bits[5:0] in VFE Map Address 0x00, Bits[5:0] and PRIM_MODE, Bits[3:0] in VFE Map Address 0x01, Bits[3:0]).

Table 1. Standard Input Video Formats

VID_STD	PRIM_MODE	Standard Input	Resolution Type
0x01	0x00	0x01	CVBS (720 × 480i at 60 Hz)
0x0C	0x01	0x0C	480p (720 × 480p at 60 Hz)
0x0D	0x01	0x0D	576p (720 × 576p at 50 Hz)
0x13	0x01	0x13	720p (1280 × 720p at 60 Hz)
0x01	0x02	0x01	SVGA (800 × 600p at 60 Hz)
0x08	0x02	0x08	VGA (640 × 480p at 60 Hz)

TYPES OF SCALING CONFIGURATION

There are two scaling configurations provided by the ADV7186: automatic scaling and manual scaling. Both configurations involve the use of the scaler block when a different output video data resolution is required, one that is completely different from the input video data resolution.

Automatic scaling of the input video data resolution to a different video data resolution at the output is automatic when the desired output resolution has a defined OUTPUT_VID in the ADV7186 core. The OUTPUT_VID is an 8-bit register represented in hexadecimal notation. The hexadecimal value 0xFF written to the OUTPUT_VID register signifies that the scaler block within the ADV7186 core is not used. This is essentially a pass through of the input video data resolution to the output; thus, the de-interlacer block and the scaler block are not used.

Automatic Scaling Configuration

When the OUTPUT_VID has a defined output resolution in the ADV7186 core, the scaling configuration in the ADV7186 is automatic. The defined output resolutions listed in Table 2 are present in the ADV7186 core.

From Table 2, when entering any of the hexadecimal values under the Output Resolution column into the OUTPUT_VID Register (Address 0x00 in the VPP Map), the standard input resolution scales correspondingly to the desired output resolution. Consider, for example, a CVBS input, a standard input with a hexadecimal value of 0x01 where the desired output is a WXGA (1366p × 768p at 60 Hz) resolution. Enter the hexadecimal value 0x93 (found in Column 2 of Table 2] into the OUTPUT_VID Register.

Table 2. Defined Output Video Standard Resolution

OUTPUT_VID	Output Resolution	Resolution Type
0x00	0x93	WXGA (1366 × 768p at 60 Hz)
0x00	0x9E	WVGA (800 × 480p at 60 Hz)
0x00	0x0C	480p (720 × 480p at 60 Hz)
0x00	0x0D	576p (720 × 576p at 50 Hz)
0x00	0x13	720p (1280 × 720p at 60 Hz)
0x00	0x81	SVGA (800 × 600p at 60 Hz)
0x00	0x88	VGA (640 × 480p at 60 Hz)
0x00	0x8C	XGA (1024 × 768p at 60 Hz)

Manual Scaling Configuration

When the OUTPUT_VID register does not have a defined output resolution in the ADV7186 core, then the manual scaling configuration is used to provide the necessary scaling of the input resolution to the output resolution. To achieve this, the timing parameters of the backend device are used. The timing parameters can be determined from the appropriate data sheet for the backend device (LCDs panels are an example of a backend device).

Timing Parameters

Horizontal Total Lines (HTotal)

Horizontal Active Lines (HActive)

Horizontal Sync (HSYNC)

Horizontal Back Porch (HBack Porch)

Horizontal Front Porch (HFront Porch)

Horizontal Blanking (HBlanking)

End of Active Video (EAV)

Start of Active Video, (SAV)

Vertical Total Lines (VTotal)

Vertical Active Lines (VActive)

Vertical Front Porch (VFront Porch)

Vertical Blanking Interval (VBI)

Vertical Back Porch (VBack Porch)

Vertical Blanking (VBlanking)

Example of Manual Scaling Configuration

The ADV7186 has several register controls that, when programmed, manually provide the timing adjustments to the backend devices, such as panels. The timing parameters for the backend device are used.

Figure 2 shows the input VGA resolution, which is a standard input to the ADV7186, and the desired output resolution, WSVGA. The WSVGA output resolution is not defined in the ADV7186 core; thus, the timing parameters of the WSVGA panel are used to program the ADV7186 register controls responsible for scaling the input resolution to the desired output resolution. Manual scaling requires that the output of the scaler block is programmed and the output timing set accordingly.

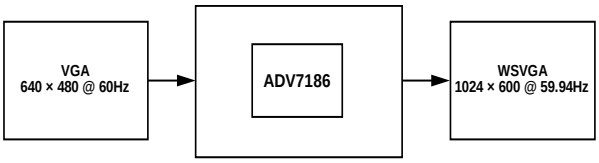

Figure 2. VGA Input Scaled to WSVGA Output Resolution

The registers to program the ADV7186 are located in the VPP map. The scaler output registers are located in Address 0xCD to Address 0xE4.

The output timing registers to set are Register Address 0x70 to Register Address 0x8D with the exclusion of Address 0x8A. I2C_OP_LINE_LENGTH, Bits[12:0] is Address 0x88 and Address 0x89 where the horizontal total lines are programmed. OP_LCOUNT_MAX, Bit[11:0] is Address 0x86 and Address 0x87 where the vertical total lines are programmed. Note that I2C_OP_LINE_LENGTH, Bits[12:0] is the same as OP_LINE_LENGTH, Bits[12:0].

SCALER BLOCK ERRORS

The scaler block may report errors due to the inability to scale the input resolution to the output resolution. The error flags are located in the VSP map, Address 0xD0. The clear error flag is located at Address 0x96, Bit 0. The toggling of Bit 0 clears the error flags register if manual scaling is achievable. If, after toggling, one of the four scaler errors is set, then this signals that manual scaling is not possible.

Table 3. Timing Parameters for WSVGA Panel

Timing Parameters	Value	VPP Map Registers
Pixel Clock	50.4 MHz	—
Horizontal Frequency	37.46 kHz	—
Vertical Frequency	59.94 Hz	—
Horizontal Total Lines (HTotal)	1344	SCAL_LINE_LENGTH, Bits[12:0], 0xE3 and 0xE4
Horizontal Active Lines (HActive)	1024	OP_HRES, Bits[11:0], 0x8B and 0x8C
Horizontal Sync (HSYNC)	136	SCAL_END_HS, Bits[12:0], 0xCF and 0xD0
Horizontal Back Porch (HBP)	160	—
Start of Active Video (SAV)	HSYNC + HBP – 4	SCAL_START_SAV, Bits[12:0], 0xD1 and 0xD2
Horizontal Front Porch (HFP)	24	—
Horizontal Blanking (HBlanking)	HTotal – HActive	—
End of Active Video (EAV)	HActive + SAV + 4	SCAL_START_EAV, Bits[12:0], 0xD3 and 0xD4
Vertical Total Lines (VTotal)	625	SCAL_LCOUNT_MAX, Bits[11:0], 0xE1 and 0xE2
Vertical Active Lines (VActive)	600	OP_VRES, Bits[11:0], 0x8C and 0x8D
Vertical Front Porch (VFP)	1	—
Vertical Sync (VSYNC)	3	SCAL_END_VS, Bits[10:0], 0xD6 and 0xD7
Vertical Back Porch (VBP)	21	—
Vertical Blanking (VBlanking)	VTotal – VActive	SCAL_END_VBI, Bits[11:0], 0xDC and 0xDD
VBI	625	SCAL_START_VBI, Bits[11:0], 0xDB and 0xDC

CONCLUSION

This application note discusses automatic and manual scaling configurations in the ADV7186.

The manual scaling configuration, which is described in depth, is used in the absence of a defined output video resolution in the ADV7186 core. To achieve manual scaling, the timing parameters required by the backend device need to be programmed or written to the control registers in the ADV7186.

The VPP map address register provides the control registers used for manual scaling. The control register provides for the output of the scaler block set and for the output timing registers set accordingly. The scaler block may or may not report errors after clearing the clear error flag bit.