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Design Considerations for Connecting Analog Devices Video Decoders to MIPI CSI-2 Receivers

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INTRODUCTION

Use this application note as a guide to help design mobile industry processor interface (MIPI®) Camera Serial Interface 2 (CSI-2) receiver systems that receive video data from Analog Devices, Inc., video decoders. This application note is based on the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M models. However, it also applies to the ADV7480, ADV7481, and ADV7482 models.

The MIPI CSI-2 is a high speed video data link. Video data is transmitted over one to four data lanes. The data is clocked using a clock lane. Each clock or data lane consists of a positive and negative clock or data line.

The MIPI CSI-2 transmitter and receiver both contain D-PHY physical layers. All termination is performed in the D-PHY layers. Note that the ADV7280-M, ADV7281-M, ADV7281-MA, ADV7282-M, ADV7480, ADV7481, and ADV7482 do not contain C-PHY physical layers.

D-PHY TERMINATION

The D-PHY layers of the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M can enter various modes of operation. These modes of operation include high speed (HS) mode, low power (LP) mode, and ultralow power state (ULPS). The output termination of the transmitter device (ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M) D-PHY changes depending on the mode in which it is operating. The transmitter device enters and exits different modes quickly. For example, the data lane on the transmitter device can switch from LP mode to HS mode up to eight times per line of video (one line of analog video is approximately 64 μs). Figure 1 shows an LP to HS to LP mode transition sequence. A 50 mV offset was added to the negative data line to differentiate between positive and negative data lines.

The MIPI CSI-2 receiver must be able to detect which operation mode the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device is in and modify its input impedance accordingly. If the MIPI CSI-2 receiver does not modify its input impedance correctly, the MIPI CSI-2 transmission becomes corrupted (Figure 3).
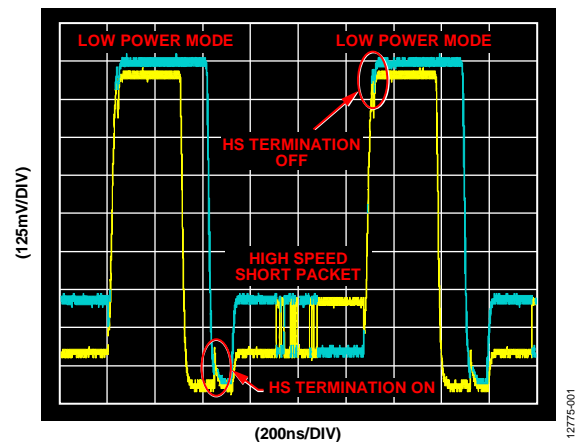

Figure 1. Capture of D0P/D0N Data Lines of the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M Transmitter Devices Exiting and Entering LP Mode (Yellow is Positive Data Line; Blue is Negative Data Line)

Voltage Level Test

The voltage level test determines whether the MIPI CSI-2 receiver D-PHY has correctly terminated the MIPI CSI-2 output from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device. Program the transmitter device into free run mode to output a test pattern over the MIPI CSI-2 link. Details on programming the transmitter device into free run mode are available in the ADV7280/ADV7281/ADV7282/ADV7283 hardware reference manual, *ADV7280/ADV7281/ADV7282/ADV7283 Functionality and Features*. Program the MIPI CSI-2 receiver to receive the MIPI data from the transmitter device.

Use a high speed oscilloscope to probe the MIPI CSI-2 lines from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M.

When properly terminated, the data lines switch between HS and LP modes, as shown in Figure 2. In LP mode, the data lines have a logic high voltage of approximately 1.2 V and a logic low voltage of approximately 0 V. In HS mode, the data lines have a logic high voltage of approximately 0.3 V and a logic low voltage of approximately 0.1 V.

If any logic level other than 1.2 V, 0.3 V, 0.1 V, or 0 V appears, the D-PHY layer of the MIPI CSI-2 receiver is not correctly terminating the output from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device. Figure 3

shows an example of the MIPI CSI-2 positive data line output from the transmitter device for a poorly terminated receiver.

When the transmitter device (ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M) is programmed, the MIPI CSI-2 clock lane exits LP mode and enters HS mode. Unless the transmitter device is manually programmed to enter LP mode or is reset, the clock lane remains in HS mode. If any logic level other than 0.3 V or 0.1 V appears on the MIPI CSI-2 clock lines, the D-PHY layer of the MIPI CSI-2 receiver does not correctly terminate the output from the transmitter device.

Capture of Positive Data Line in High Speed and Low Power Modes

Figure 2 and Figure 3 show the difference between a correct and an incorrect termination of the MIPI CSI-2 signal by the D-PHY layer in the MIPI CSI-2 receiver.
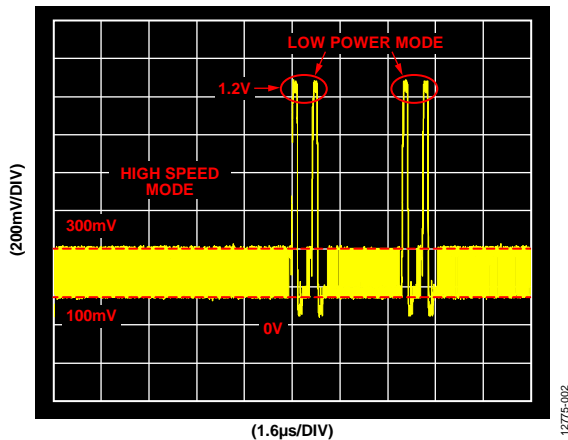

Figure 2. Positive Data Line (D0P) Output from the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M Transmitter Devices; Correct MIPI CSI-2 Receiver Termination
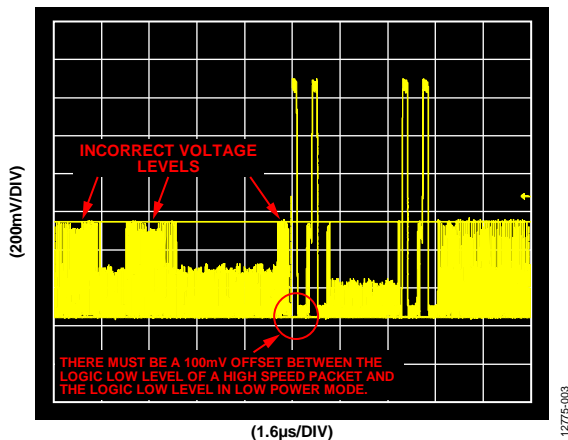

Figure 3. Positive Data Line (D0P) Output from the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M Transmitter Devices; Incorrect MIPI CSI-2 Receiver Termination

D-PHY Mode Detection Test

To test that the MIPI CSI-2 receiver can detect each operation mode, manually program the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device to enter HS mode, LP mode, and ULPS. Then, test the MIPI CSI-2 receiver

to verify that it can correctly detect the operation mode of the transmitter device.

Refer to the ADV7280/ADV7281/ADV7282/ADV7283 hardware reference manual, *ADV7280/ADV7281/ADV7282/ ADV7283 Functionality and Features*, for details on manually programming the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M to enter HS mode, LP mode, and ULPS.

Clock Lane Low Power to High Speed Transition

Some MIPI CSI-2 receivers wait for an LP to HS mode transition on the MIPI CSI-2 clock lane before starting video capture. However, the LP to HS mode transition on the MIPI CSI-2 clock lane occurs only once on the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M immediately after they are initially programmed.

If the MIPI CSI-2 receiver is initialized after the transmitter device is initialized, the MIPI CSI-2 may never detect the LP to HS mode transition on the clock lane from the transmitter device. If the MIPI CSI-2 receiver does not detect the LP to HS mode transition, it may never start video capture.

To overcome this issue, manually program the clock lane of the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M to enter and then exit LP mode. The easiest way to do this is by toggling the CSITX_PWRDN bit (Address 0x00, Bit 7).

The MIPI CSI-2 receiver then recognizes an LP to HS mode transition and begins video capture.

DESIGN OF MIPI CSI-2 RECEIVER SYSTEM

The following sections provide tips on debugging issues with the MIPI CSI-2 receiver system that is receiving video data from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M.

Lock Status

When an analog video source is connected to the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M video decoder, it can take the video decoder a period of time before it locks to the incoming analog video. This period of time can take up to 250 ms in fast switch mode and more than 500 ms in autodetect mode. The ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M outputs spurious data over the MIPI CSI-2 link until the device locks to the incoming analog video.

It is recommended that the MIPI CSI-2 receiver system be set to ignore the output from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M until the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M has locked to the analog video.

The FSC_LOCK, LOST_LOCK, and IN_LOCK bits (Register 0x10, Bits[2:0]) indicate whether the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device has locked to the analog video source.

Use the INTRQ hardware interrupt pin in conjunction with the FSC_LOCK, LOST_LOCK, and IN_LOCK bits to verify when a lock event has occurred. Using the INTRQ hardware interrupt

pin saves the MIPI CSI-2 receiver from constantly polling the FSC_LOCK, LOST_LOCK, and IN_LOCK bits.

Use the CSITX_PWRDN bit to stop the MIPI CSI-2 output from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M. Stop the MIPI CSI-2 output until the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M has locked to the analog video source, as indicated by the INTRQ hardware interrupt pin.

For more information on the CSITX_PWRDN, FSC_LOCK, LOST_LOCK, and IN_LOCK bits and on the INTRQ hardware interrupt pin, see the ADV7280/ADV7281/ADV7282/ADV7283 hardware reference manual, *ADV7280/ADV7281/ADV7282/ADV7283 Functionality and Features*.

Deinterlacer

By default, the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M transmitter devices output video data in an interlaced format in the YCbCr 4:2:2 color space. In most applications, the MIPI CSI-2 receiver system requires a deinterlacing function. The most common way of performing this function is by using a frame buffer. For example, an odd field and an even field of video are transmitted into a memory buffer in the MIPI CSI-2 receiver system. The data stored in the memory buffer is then analyzed as a complete progressive frame of video by the MIPI CSI-2 receiver system.

Alternatively, the ADV7280-M and ADV7282-M transmitter devices have an integrated deinterlacer. This is referred to as the interlaced to progressive (I2P) core in the ADV7280-M and ADV7282-M data sheets and in the hardware reference manual, *ADV7280/ADV7281/ADV7282/ADV7283 Functionality and Features*. Using the I2P cores on the ADV7280-M and the ADV7282-M transmitter devices and programming them to output in progressive mode eliminates the need for deinterlacing in the MIPI CSI-2 receiver system.

The I2P core of the ADV7280-M and ADV7282-M interpolates between two lines of video. An algorithm is used to smooth the resulting image to minimize low angle artifacts.

Odd and Even Fields of Different Lengths

The ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M video decoders output video over the MIPI CSI-2 stream. However, the video timing is based on the ITU-R BT.656-3 or ITU-R BT.656-4 standard.

In interlaced mode, an NTSC video source results in the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M transmitter devices outputting video where the odd fields are one line longer than the even fields. This difference occurs with NTSC sources only. PAL sources result in even and odd fields of the same length.

When designing video frame buffers in the MIPI CSI-2 receiver system, the even and odd fields can be of different length.

However, the ADV7280-M and ADV7282-M models with I2P cores can be programmed to output progressive video. In progressive mode, all fields output by the transmitter devices are the same length.

For more information on the video output timing or the I2P core, see the ADV7280/ADV7281/ADV7282/ADV7283 hardware reference manual, *ADV7280/ADV7281/ADV7282/ADV7283 Functionality and Features*.

Video Frame Buffer Overflows

Most MIPI CSI-2 receivers contain a video frame buffer. Each video frame from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device is stored in a memory buffer before being analyzed by the MIPI CSI-2 receiver.

Under certain circumstances (if the analog video source is disconnected, for example), the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device can output video frames with a nonstandard number of lines because the transmitter device is designed to be effective at processing poor video sources.

When the CVBS source is not present, the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device continues to output MIPI CSI-2 video data and enters a search mode. When the device is in search mode, any noise on the CVBS input is tested to determine whether it is an analog video signal. When in search mode, the transmitter device outputs frames that are much longer than standard.

The ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device remains in search mode for approximately 1 sec in autodetect mode. In fast switch mode, the transmitter device remains in search mode for approximately six fields of video.

If a valid analog video source is not detected after the period where the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M is in search mode, the device determines that no video source is present. The device then exits search mode and enters free run mode. In free run mode, the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device outputs test pattern video frames with standard timing.

These nonstandard video frames output during search mode can cause a buffer overflow event in the MIPI CSI-2 receiver. One of the best solutions to prevent a buffer overflow is to use a line counter.

The line counter is a control loop in the MIPI CSI-2 receiver that counts the number of lines being output per frame by the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device. If the number of lines output per frame exceeds a limit, the MIPI CSI-2 receiver ignores the output from the transmitter device until the next frame start packet.

Choose the line number limit so that the video buffer memory of the MIPI CSI-2 receiver does not overflow and so that standard video sources are not attenuated.

By default, the MIPI CSI-2 frame start/end packets and the MIPI line start/end packets are output by the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device.

Free Run Mode

When the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device is programmed into free run mode, the device ignores the analog video input and outputs a fixed test pattern. Free run mode can help customers debug issues with their MIPI CSI-2 receiver systems. A number of test patterns are available. For more information, see the ADV7280/ ADV7281/ADV7282/ADV7283 hardware reference manual, *ADV7280/ADV7281/ADV7282/ADV7283 Functionality and Features*.

LAYOUT OF MIPI CSI-2 TRACES

MIPI CSI-2 is designed as a chip to chip interface; therefore, it does not transmit over long distances. The D-PHY specification defines the maximum lane flight time to 2 ns. Using standard printed circuit board (PCB) materials and design rules (for example, transmitting MIPI CSI-2 through a microstripline on a standard FR4 PCB), results in a maximum trace length of 25 cm to 30 cm. Therefore, keep the MIPI CSI-2 traces from the ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device to the MIPI CSI-2 receiver under 30 cm in length.

MIPI CSI-2 line traces must have a characteristic impedance of 50 Ω single-ended and 100 Ω differential.

Loosely couple the positive and negative lines of each lane (for example, Data Line 0 positive; Data Line 0 negative) because the positive and negative lines are differential in HS mode but are single-ended in LP mode. As a general rule, space apart the line

traces by a distance equal to twice the thickness of the PCB dielectric.

Connect MIPI CSI-2 traces from one ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter device to one MIPI CSI-2 receiver. It is not possible to daisy-chain multiple ADV7280-M, ADV7281-M, ADV7281-MA, or ADV7282-M transmitter devices to one MIPI CSI-2 receiver.

All filtering and termination is performed in the D-PHY layer of the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M transmitter devices and in the D-PHY layer of the MIPI CSI-2 receiver. Do not place additional components, such as resistors, electrostatic discharge (ESD) diodes, capacitors, or common-mode chokes on the MIPI CSI-2 traces.

REFERENCES

MIPI® Alliance Specification for D-PHY, Version 1.00.00, Mobile Industry Processor Industry Alliance, 2009.

MIPI® Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.01.00, Mobile Industry Processor Industry Alliance, 2010.

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