Software User Guide
UG-206

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ADV7842 I²C Register Maps

This software user guide documents the I²C register maps for the ADV7842. The ADV7842 is a dual HDMI® fast switching receiver with a 12-bit, 170 MHz video and graphics digitizer and a 3D comb filter decoder.

This user guide consists of three sections. The first section provides detailed register tables for the register maps of twelve functional blocks. The second section provides detailed signal documentation for each register. The third section consists of a detailed index.

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REVISION HISTORY

11/10-Revision 0: Initial Version

1 REGISTER TABLES

1.1 IO MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x08	VIDEO STANDARD	rw	-	-	VID_STD[5]	VID_STD[4]	VID_STD[3]	VID_STD[2]	VID_STD[1]	VID_STD[0]
0x01	0x06	PRIMARY MODE	rw	ADC_HDMI_SIMULT_MODE	V_FREQ[2]	V_FREQ[1]	V_FREQ[0]	PRIM_MODE[3]	PRIM_MODE[2]	PRIM_MODE[1]	PRIM_MODE[0]
0x02	0xF0	IO_REG_02	rw	INP_COLOR_SPACE[3]	INP_COLOR_SPACE[2]	INP_COLOR_SPACE[1]	INP_COLOR_SPACE[0]	ALT_GAMMA	OP_656_RANGE	RGB_OUT	ALT_DATA_SAT
0x03	0x00	IO_REG_03	rw	OP_FORMAT_SEL[7]	OP_FORMAT_SEL[6]	OP_FORMAT_SEL[5]	OP_FORMAT_SEL[4]	OP_FORMAT_SEL[3]	OP_FORMAT_SEL[2]	OP_FORMAT_SEL[1]	OP_FORMAT_SEL[0]
0x04	0x62		rw	OP_CH_SEL[2]	OP_CH_SEL[1]	OP_CH_SEL[0]	-	-	-	-	-
0x05	0x2C	IO_REG_05	rw	-	-	-	F_OUT_SEL	DATA_BLANK_EN	AVCODE_INSERT_EN	REPL_AV_CODE	OP_SWAP_CB_CR
0x06	0xA0	IO_REG_06	rw	VS_OUT_SEL	HS_OUT_SEL[1]	HS_OUT_SEL[0]	INV_SYNC_OUT_POL	INV_F_POL	INV_VS_POL	INV_HS_POL	INV_LLC_POL
0x07	0x40	IO_REG_07	rw	SYNC_CH_AUTO_MODE	SYNC_CH1_PRIORITY	SYNC_CH1_HS_SEL[1]	SYNC_CH1_HS_SEL[0]	SYNC_CH1_VS_SEL[1]	SYNC_CH1_VS_SEL[0]	SYNC_CH1_EMB_SYNC_SEL[1]	SYNC_CH1_EMB_SYNC_SEL[0]
0x08	0x14	IO_REG_08	rw	-	-	SYNC_CH2_HS_SEL[1]	SYNC_CH2_HS_SEL[0]	SYNC_CH2_VS_SEL[1]	SYNC_CH2_VS_SEL[0]	SYNC_CH2_EMB_SYNC_SEL[1]	SYNC_CH2_EMB_SYNC_SEL[0]
0x0B	0x44	IO_REG_0B	rw	-	SEL_RAW_CS	-	-	-	-	CORE_PDN	XTAL_PDN
0x0C	0x62	IO_REG_0C	rw	-	-	POWER_DOWN	-	-	CP_PWRDN	VDP_PDN	PADS_PDN
0x12	0x00	IO_REG_12	r	SEL_SYNC_CHANNEL	-	-	CP_STDI_INTERLACED	CP_INTERLACED	CP_PROG_PARM_FOR_INT	CP_FORCE_INTERLACED	CP_NON_STD_VIDEO
0x13	0x00	IO_REG_13	r	-	-	-	-	-	-	CP_CURRENT_SYNC_SRC[1]	CP_CURRENT_SYNC_SRC[0]
0x14	0x6A	IO_REG_14	rw	-	-	DR_STR[1]	DR_STR[0]	DR_STR_CLK[1]	DR_STR_CLK[0]	DR_STR_SYNC[1]	DR_STR_SYNC[0]
0x15	0xBE	IO_REG_15	rw	-	-	TRI_SYNC_OUT	TRI_AUDIO	TRI_SYNCS	TRI_LLC	TRI_PIX	-
0x16	0x43	IO_REG_16	rw	PLL_DIV_MAN_EN	-	-	PLL_DIV_RATIO[12]	PLL_DIV_RATIO[11]	PLL_DIV_RATIO[10]	PLL_DIV_RATIO[9]	PLL_DIV_RATIO[8]
0x17	0x5A		rw	PLL_DIV_RATIO[7]	PLL_DIV_RATIO[6]	PLL_DIV_RATIO[5]	PLL_DIV_RATIO[4]	PLL_DIV_RATIO[3]	PLL_DIV_RATIO[2]	PLL_DIV_RATIO[1]	PLL_DIV_RATIO[0]
0x19	0x00	LLC_DLL	rw	LLC_DLL_EN	LLC_DLL_DOUBLE	-	LLC_DLL_PHASE[4]	LLC_DLL_PHASE[3]	LLC_DLL_PHASE[2]	LLC_DLL_PHASE[1]	LLC_DLL_PHASE[0]
0x1A	0x02	SUB_I2C_CONTROL	rw	-	-	-	-	-	-	SUBI2C_EN	VDP_ON_SUB_I2C
0x20	0xF0	HPA_REG1	rw	-	-	HPA_MAN_VALUE_A	HPA_MAN_VALUE_B	-	-	HPA_TRISTATE_A	HPA_TRISTATE_B
0x21	0x00	HPA_REG2	r	-	-	-	-	-	-	HPA_STATUS_PORT_A	HPA_STATUS_PORT_B
0x30	0x88	IO_REG_30	rw	-	-	-	PIXBUS_MSB_TO_LSB_REORDER	-	-	-	-
0x33	0x00	IO_REG_33	rw	-	LLC_DLL_MUX	-	-	-	-	-	-
0x3F	0x00	INT STATUS	r	-	-	-	-	-	-	INTRQ_RAW	INTRQ2_RAW
0x40	0x20	INT1_CONFIGURATION	rw	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	-	STORE_UNMASKED_IRQS	EN_MUTE_OUT_INTRQ	MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x41	0x30	INT2_CONFIGURATION	rw	INTRQ2_DUR_SEL[1]	INTRQ2_DUR_SEL[0]	CP_LOCK_UNLOCK_EDGE_SEL	STDI_DATA_VALID_EDGE_SEL	EN_MUTE_OUT_INTRQ2	INT2_EN	INTRQ2_OP_SEL[1]	INTRQ2_OP_SEL[0]
0x42	0x00	RAW_STATUS_1	r	SSPD_RSLT_CHNGD_RAW	MV_PS_DET_RAW	-	STDI_DATA_VALID_RAW	CP_UNLOCK_RAW	CP_LOCK_RAW	-	AFE_INTERRUPT_RAW
0x43	0x00	INTERRUPT_STATUS_1	r	SSPD_RSLT_CHNGD_ST	MV_PS_DET_ST	-	STDI_DATA_VALID_ST	CP_UNLOCK_ST	CP_LOCK_ST	-	AFE_INTERRUPT_ST
0x44	0x00	INTERRUPT_CLEAR_1	sc	SSPD_RSLT_CHNGD_CLR	MV_PS_DET_CLR	-	STDI_DATA_VALID_CLR	CP_UNLOCK_CLR	CP_LOCK_CLR	-	AFE_INTERRUPT_CLR
0x45	0x00	INTERRUPT2_MASKB_1	rw	SSPD_RSLT_CHNGD_MB2	MV_PS_DET_MB2	-	STDI_DATA_VALID_MB2	CP_UNLOCK_MB2	CP_LOCK_MB2	-	AFE_INTERRUPT_MB2
0x46	0x00	INTERRUPT_MASKB_1	rw	SSPD_RSLT_CHNGD_MB1	MV_PS_DET_MB1	-	STDI_DATA_VALID_MB1	CP_UNLOCK_MB1	CP_LOCK_MB1	-	AFE_INTERRUPT_MB1
0x47	0x00	RAW_STATUS_2	r	MPU_STIM_INTRQ_RAW	MV_AGC_DET_RAW	MV_CS_DET_RAW	-	-	CP_CGMS_CHNGD_RAW	-	-
0x48	0x00	INTERRUPT_STATUS_2	r	MPU_STIM_INTRQ_ST	MV_AGC_DET_ST	MV_CS_DET_ST	-	-	CP_CGMS_CHNGD_ST	-	-
0x49	0x00	INTERRUPT_CLEAR_2	sc	MPU_STIM_INTRQ_CLR	MV_AGC_DET_CLR	MV_CS_DET_CLR	-	-	CP_CGMS_CHNGD_CLR	-	-
0x4A	0x00	INTERRUPT2_MASKB_2	rw	MPU_STIM_INTRQ_MB2	MV_AGC_DET_MB2	MV_CS_DET_MB2	-	-	CP_CGMS_CHNGD_MB2	-	-
0x4B	0x00	INTERRUPT_MASKB_2	rw	MPU_STIM_INTRQ_MB1	MV_AGC_DET_MB1	MV_CS_DET_MB1	-	-	CP_CGMS_CHNGD_MB1	-	-
0x4C	0x00	AVLINK_RAW_STATUS	r	-	-	-	-	AVLINK_RX_READY_RAW	AVLINK_TX_RETRY_TIMEOUT_RAW	AVLINK_TX_ARBITRATION_LOST_RAW	AVLINK_TX_READY_RAW
0x4D	0x00	INTERRUPT_STATUS_3	r	-	-	-	-	AVLINK_RX_READY_ST	AVLINK_TX_RETRY_TIMEOUT_ST	AVLINK_TX_ARBITRATION_LOST_ST	AVLINK_TX_READY_ST
0x4E	0x00	INTERRUPT_CLEAR_3	sc	-	-	-	-	AVLINK_RX_READY_CLR	AVLINK_TX_RETRY_TIMEOUT_CLR	AVLINK_TX_ARBITRATION_LOST_CLR	AVLINK_TX_READY_CLR
0x4F	0x00	INTERRUPT2_MASKB_3	rw	-	-	-	-	AVLINK_RX_READY_MB2	AVLINK_TX_RETRY_TIMEOUT_MB2	AVLINK_TX_ARBITRATION_LOST_MB2	AVLINK_TX_READY_MB2
0x50	0x00	INTERRUPT_MASKB_3	rw	-	-	-	-	AVLINK_RX_READY_MB1	AVLINK_TX_RETRY_TIMEOUT_MB1	AVLINK_TX_ARBITRATION_LOST_MB1	AVLINK_TX_READY_MB1
0x51	0x00	RAW_STATUS_4	r	TTXT_AVL_RAW	VITC_AVL_RAW	GS_DATA_TYPE_RAW	GS_PDC_VPS_UTC_AVL_RAW	FASTI2C_DATA_RDY_RAW	CGMS_WSS_AVL_RAW	CCAP_EVEN_FIELD_RAW	CCAP_AVL_RAW
0x52	0x00	INTERRUPT_STATUS_4	r	TTXT_AVL_ST	VITC_AVL_ST	GS_DATA_TYPE_ST	GS_PDC_VPS_UTC_AVL_ST	FASTI2C_DATA_RDY_ST	CGMS_WSS_AVL_ST	CCAP_EVEN_FIELD_ST	CCAP_AVL_ST
0x53	0x00	INTERRUPT_CLEAR_4	sc	TTXT_AVL_CLR	VITC_AVL_CLR	GS_DATA_TYPE_CLR	GS_PDC_VPS_UTC_AVL_CLR	FASTI2C_DATA_RDY_CLR	CGMS_WSS_AVL_CLR	CCAP_EVEN_FIELD_CLR	CCAP_AVL_CLR
0x54	0x00	INTERRUPT2_MASKB_4	rw	TTXT_AVL_MB2	VITC_AVL_MB2	GS_DATA_TYPE_MB2	GS_PDC_VPS_UTC_AVL_MB2	FASTI2C_DATA_RDY_MB2	CGMS_WSS_AVL_MB2	CCAP_EVEN_FIELD_MB2	CCAP_AVL_MB2
0x55	0x00	INTERRUPT_MASKB_4	rw	TTXT_AVL_MB1	VITC_AVL_MB1	GS_DATA_TYPE_MB1	GS_PDC_VPS_UTC_AVL_MB1	FASTI2C_DATA_RDY_MB1	CGMS_WSS_AVL_MB1	CCAP_EVEN_FIELD_MB1	CCAP_AVL_MB1
0x56	0x00	RAW_STATUS_5	r	SDP_PROGRESSIVE_RAW	SDP_PR_DET_RAW	SDP_SD_DET_RAW	SDP_50HZ_DET_RAW	-	-	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x57	0x00	INTERRUPT_STATUS_5	r	SDP_PROGRESSIVE_ST	SDP_PR_DET_ST	SDP_SD_DET_ST	SDP_50HZ_DET_ST	-	-	-	-
0x58	0x00	INTERRUPT_CLEAR_5	sc	SDP_PROGRESSIVE_CLR	SDP_PR_DET_CLR	SDP_SD_DET_CLR	SDP_50HZ_DET_CLR	-	-	-	-
0x59	0x00	INTERRUPT2_MASKB_5	rw	SDP_PROGRESSIVE_MB2	SDP_PR_DET_MB2	SDP_SD_DET_MB2	SDP_50HZ_DET_MB2	-	-	-	-
0x5A	0x00	INTERRUPT_MASKB_5	rw	SDP_PROGRESSIVE_MB1	SDP_PR_DET_MB1	SDP_SD_DET_MB1	SDP_50HZ_DET_MB1	-	-	-	-
0x5B	0x00	RAW_STATUS_6	r	CP_LOCK_CH2_RAW	CP_UNLOCK_CH2_RAW	STDI_DVALID_CH2_RAW	SSPD_RSLT_CHNGD_CH2_RAW	CP_LOCK_CH1_RAW	CP_UNLOCK_CH1_RAW	STDI_DVALID_CH1_RAW	SSPD_RSLT_CHNGD_CH1_RAW
0x5C	0x00	INTERRUPT_STATUS_6	r	CP_LOCK_CH2_ST	CP_UNLOCK_CH2_ST	STDI_DVALID_CH2_ST	SSPD_RSLT_CHNGD_CH2_ST	CP_LOCK_CH1_ST	CP_UNLOCK_CH1_ST	STDI_DVALID_CH1_ST	SSPD_RSLT_CHNGD_CH1_ST
0x5D	0x00	INTERRUPT_CLEAR_6	sc	CP_LOCK_CH2_CLR	CP_UNLOCK_CH2_CLR	STDI_DVALID_CH2_CLR	SSPD_RSLT_CHNGD_CH2_CLR	CP_LOCK_CH1_CLR	CP_UNLOCK_CH1_CLR	STDI_DVALID_CH1_CLR	SSPD_RSLT_CHNGD_CH1_CLR
0x5E	0x00	INTERRUPT2_MASKB_6	rw	CP_LOCK_CH2_MB2	CP_UNLOCK_CH2_MB2	STDI_DVALID_CH2_MB2	SSPD_RSLT_CHNGD_CH2_MB2	CP_LOCK_CH1_MB2	CP_UNLOCK_CH1_MB2	STDI_DVALID_CH1_MB2	SSPD_RSLT_CHNGD_CH1_MB2
0x5F	0x00	INTERRUPT_MASKB_6	rw	CP_LOCK_CH2_MB1	CP_UNLOCK_CH2_MB1	STDI_DVALID_CH2_MB1	SSPD_RSLT_CHNGD_CH2_MB1	CP_LOCK_CH1_MB1	CP_UNLOCK_CH1_MB1	STDI_DVALID_CH1_MB1	SSPD_RSLT_CHNGD_CH1_MB1
0x60	0x00	HDMI LVL RAW STATUS 1	r	ISRC2_PCKT_RAW	ISRC1_PCKT_RAW	ACP_PCKT_RAW	VS_INFO_RAW	MS_INFO_RAW	SPD_INFO_RAW	AUDIO_INFO_RAW	AVI_INFO_RAW
0x61	0x00	HDMI LVL INT STATUS 1	r	ISRC2_PCKT_ST	ISRC1_PCKT_ST	ACP_PCKT_ST	VS_INFO_ST	MS_INFO_ST	SPD_INFO_ST	AUDIO_INFO_ST	AVI_INFO_ST
0x62	0x00	HDMI LVL INT CLR 1	sc	ISRC2_PCKT_CLR	ISRC1_PCKT_CLR	ACP_PCKT_CLR	VS_INFO_CLR	MS_INFO_CLR	SPD_INFO_CLR	AUDIO_INFO_CLR	AVI_INFO_CLR
0x63	0x00	HDMI LVL INT2 MASKB 1	rw	ISRC2_PCKT_MB2	ISRC1_PCKT_MB2	ACP_PCKT_MB2	VS_INFO_MB2	MS_INFO_MB2	SPD_INFO_MB2	AUDIO_INFO_MB2	AVI_INFO_MB2
0x64	0x00	HDMI LVL INT MASKB 1	rw	ISRC2_PCKT_MB1	ISRC1_PCKT_MB1	ACP_PCKT_MB1	VS_INFO_MB1	MS_INFO_MB1	SPD_INFO_MB1	AUDIO_INFO_MB1	AVI_INFO_MB1
0x65	0x00	HDMI LVL RAW STATUS 2	r	CS_DATA_VALID_RAW	INTERNAL_MUTE_RAW	AV_MUTE_RAW	AUDIO_CH_MD_RAW	HDMI_MODE_RAW	GEN_CTL_PCKT_RAW	AUDIO_C_PCKT_RAW	GAMUT_MDATA_RAW
0x66	0x00	HDMI LVL INT STATUS 2	r	CS_DATA_VALID_ST	INTERNAL_MUTE_ST	AV_MUTE_ST	AUDIO_CH_MD_ST	HDMI_MODE_ST	GEN_CTL_PCKT_ST	AUDIO_C_PCKT_ST	GAMUT_MDATA_ST
0x67	0x00	HDMI LVL INT CLR 2	sc	CS_DATA_VALID_CLR	INTERNAL_MUTE_CLR	AV_MUTE_CLR	AUDIO_CH_MD_CLR	HDMI_MODE_CLR	GEN_CTL_PCKT_CLR	AUDIO_C_PCKT_CLR	GAMUT_MDATA_CLR
0x68	0x00	HDMI LVL INT2 MASKB 2	rw	CS_DATA_VALID_MB2	INTERNAL_MUTE_MB2	AV_MUTE_MB2	AUDIO_CH_MD_MB2	HDMI_MODE_MB2	GEN_CTL_PCKT_MB2	AUDIO_C_PCKT_MB2	GAMUT_MDATA_MB2
0x69	0x00	HDMI LVL INT MASKB 2	rw	CS_DATA_VALID_MB1	INTERNAL_MUTE_MB1	AV_MUTE_MB1	AUDIO_CH_MD_MB1	HDMI_MODE_MB1	GEN_CTL_PCKT_MB1	AUDIO_C_PCKT_MB1	GAMUT_MDATA_MB1
0x6A	0x00	HDMI LVL RAW STATUS 3	r	-	-	TMDSPLL_LCK_A_RAW	TMDSPLL_LCK_B_RAW	-	-	TMDS_CLK_A_RAW	TMDS_CLK_B_RAW
0x6B	0x00	HDMI LVL INT STATUS 3	r	-	-	TMDSPLL_LCK_A_ST	TMDSPLL_LCK_B_ST	-	-	TMDS_CLK_A_ST	TMDS_CLK_B_ST
0x6C	0x00	HDMI LVL INT CLR 3	sc	-	-	TMDSPLL_LCK_A_CLR	TMDSPLL_LCK_B_CLR	-	-	TMDS_CLK_A_CLR	TMDS_CLK_B_CLR
0x6D	0x00	HDMI LVL INT2 MASKB 3	rw	-	-	TMDSPLL_LCK_A_MB2	TMDSPLL_LCK_B_MB2	-	-	TMDS_CLK_A_MB2	TMDS_CLK_B_MB2
0x6E	0x00	HDMI LVL INT MASKB 3	rw	-	-	TMDSPLL_LCK_A_MB1	TMDSPLL_LCK_B_MB1	-	-	TMDS_CLK_A_MB1	TMDS_CLK_B_MB1

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6F	0x00	HDMI LVL RAW STATUS 4	r	-	-	HDMI_ENCRPT_A_RAW	HDMI_ENCRPT_B_RAW	-	-	CABLE_DET_A_RAW	CABLE_DET_B_RAW
0x70	0x00	HDMI LVL INT STATUS 4	r	-	-	HDMI_ENCRPT_A_ST	HDMI_ENCRPT_B_ST	-	-	CABLE_DET_A_ST	CABLE_DET_B_ST
0x71	0x00	HDMI LVL INT CLR 4	sc	-	-	HDMI_ENCRPT_A_CLR	HDMI_ENCRPT_B_CLR	-	-	CABLE_DET_A_CLR	CABLE_DET_B_CLR
0x72	0x00	HDMI LVL INT2 MASKB 4	rw	-	-	HDMI_ENCRPT_A_MB2	HDMI_ENCRPT_B_MB2	-	-	CABLE_DET_A_MB2	CABLE_DET_B_MB2
0x73	0x00	HDMI LVL INT MASKB 4	rw	-	-	HDMI_ENCRPT_A_MB1	HDMI_ENCRPT_B_MB1	-	-	CABLE_DET_A_MB1	CABLE_DET_B_MB1
0x74	0x00	HDMI LVL RAW STATUS 5	r	-	-	-	-	-	VIDEO_3D_RAW	V_LOCKED_RAW	DE_REGEN_LCK_RAW
0x75	0x00	HDMI LVL INT STATUS 5	r	-	-	-	-	-	VIDEO_3D_ST	V_LOCKED_ST	DE_REGEN_LCK_ST
0x76	0x00	HDMI LVL INT CLR 5	sc	-	-	-	-	-	VIDEO_3D_CLR	V_LOCKED_CLR	DE_REGEN_LCK_CLR
0x77	0x00	HDMI LVL INT2 MASKB 5	rw	-	-	-	-	-	VIDEO_3D_MB2	V_LOCKED_MB2	DE_REGEN_LCK_MB2
0x78	0x00	HDMI LVL INT MASKB 5	rw	-	-	-	-	-	VIDEO_3D_MB1	V_LOCKED_MB1	DE_REGEN_LCK_MB1
0x79	0x00	HDMI EDG RAW STATUS 1	r	NEW_ISRC2_PCKT_RAW	NEW_ISRC1_PCKT_RAW	NEW_ACP_PCKT_RAW	NEW_VS_INFO_RAW	NEW_MS_INFO_RAW	NEW_SPD_INFO_RAW	NEW_AUDIO_INFO_RAW	NEW_AVI_INFO_RAW
0x7A	0x00	HDMI EDG INT STATUS 1	r	NEW_ISRC2_PCKT_ST	NEW_ISRC1_PCKT_ST	NEW_ACP_PCKT_ST	NEW_VS_INFO_ST	NEW_MS_INFO_ST	NEW_SPD_INFO_ST	NEW_AUDIO_INFO_ST	NEW_AVI_INFO_ST
0x7B	0x00	HDMI EDG INT CLR 1	sc	NEW_ISRC2_PCKT_CLR	NEW_ISRC1_PCKT_CLR	NEW_ACP_PCKT_CLR	NEW_VS_INFO_CLR	NEW_MS_INFO_CLR	NEW_SPD_INFO_CLR	NEW_AUDIO_INFO_CLR	NEW_AVI_INFO_CLR
0x7C	0x00	HDMI EDG INT2 MASKB 1	rw	NEW_ISRC2_PCKT_MB2	NEW_ISRC1_PCKT_MB2	NEW_ACP_PCKT_MB2	NEW_VS_INFO_MB2	NEW_MS_INFO_MB2	NEW_SPD_INFO_MB2	NEW_AUDIO_INFO_MB2	NEW_AVI_INFO_MB2
0x7D	0x00	HDMI EDG INT MASKB 1	rw	NEW_ISRC2_PCKT_MB1	NEW_ISRC1_PCKT_MB1	NEW_ACP_PCKT_MB1	NEW_VS_INFO_MB1	NEW_MS_INFO_MB1	NEW_SPD_INFO_MB1	NEW_AUDIO_INFO_MB1	NEW_AVI_INFO_MB1
0x7E	0x00	HDMI EDG RAW STATUS 2	r	FIFO_NEAR_OVFL_RAW	FIFO_UNDERFLO_RAW	FIFO_OVERFLO_RAW	CTS_PASS_THRSH_RAW	CHANGE_N_RAW	PACKET_ERROR_RAW	AUDIO_PCKT_ERR_RAW	NEW_GAMUT_MDATA_RAW
0x7F	0x00	HDMI EDG INT STATUS 2	r	FIFO_NEAR_OVFL_ST	FIFO_UNDERFLO_ST	FIFO_OVERFLO_ST	CTS_PASS_THRSH_ST	CHANGE_N_ST	PACKET_ERROR_ST	AUDIO_PCKT_ERR_ST	NEW_GAMUT_MDATA_ST
0x80	0x00	HDMI EDG INT CLR 2	sc	FIFO_NEAR_OVFL_CLR	FIFO_UNDERFLO_CLR	FIFO_OVERFLO_CLR	CTS_PASS_THRSH_CLR	CHANGE_N_CLR	PACKET_ERROR_CLR	AUDIO_PCKT_ERR_CLR	NEW_GAMUT_MDATA_CLR
0x81	0x00	HDMI EDG INT2 MASKB 2	rw	FIFO_NEAR_OVFL_MB2	FIFO_UNDERFLO_MB2	FIFO_OVERFLO_MB2	CTS_PASS_THRSH_MB2	CHANGE_N_MB2	PACKET_ERROR_MB2	AUDIO_PCKT_ERR_MB2	NEW_GAMUT_MDATA_MB2
0x82	0x00	HDMI EDG INT MASKB 2	rw	FIFO_NEAR_OVFL_MB1	FIFO_UNDERFLO_MB1	FIFO_OVERFLO_MB1	CTS_PASS_THRSH_MB1	CHANGE_N_MB1	PACKET_ERROR_MB1	AUDIO_PCKT_ERR_MB1	NEW_GAMUT_MDATA_MB1
0x83	0x00	HDMI EDG RAW STATUS 3	r	DEEP_COLOR_CHNG_RAW	VCLK_CHNG_RAW	AUDIO_MODE_CHNG_RAW	PARITY_ERROR_RAW	NEW_SAMP_RT_RAW	AUDIO_FLT_LINE_RAW	NEW_TMDS_FRQ_RAW	FIFO_NEAR_UFLO_RAW
0x84	0x00	HDMI EDG STATUS 3	r	DEEP_COLOR_CHNG_ST	VCLK_CHNG_ST	AUDIO_MODE_CHNG_ST	PARITY_ERROR_ST	NEW_SAMP_RT_ST	AUDIO_FLT_LINE_ST	NEW_TMDS_FRQ_ST	FIFO_NEAR_UFLO_ST
0x85	0x00	HDMI EDG INT CLR 3	sc	DEEP_COLOR_CHNG_CLR	VCLK_CHNG_CLR	AUDIO_MODE_CHNG_CLR	PARITY_ERROR_CLR	NEW_SAMP_RT_CLR	AUDIO_FLT_LINE_CLR	NEW_TMDS_FRQ_CLR	FIFO_NEAR_UFLO_CLR
0x86	0x00	HDMI EDG INT2 MASKB 3	rw	DEEP_COLOR_CHNG_MB2	VCLK_CHNG_MB2	AUDIO_MODE_CHNG_MB2	PARITY_ERROR_MB2	NEW_SAMP_RT_MB2	AUDIO_FLT_LINE_MB2	NEW_TMDS_FRQ_MB2	FIFO_NEAR_UFLO_MB2

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x87	0x00	HDMI EDG INT MASKB 3	rw	DEEP_COLOR_CHNG_MB1	VCLK_CHNG_MB1	AUDIO_MODE_CHNG_MB1	PARITY_ERROR_MB1	NEW_SAMP_RT_MB1	AUDIO_FLT_LINE_MB1	NEW_TMDS_FRQ_MB1	FIFO_NEAR_UFLO_MB1
0x88	0x00	HDMI EDG RAW STATUS 4	r	MS_INF_CKS_ERR_RAW	SPD_INF_CKS_ERR_RAW	AUD_INF_CKS_ERR_RAW	AVI_INF_CKS_ERR_RAW	-	-	AKSV_UPDATE_A_RAW	AKSV_UPDATE_B_RAW
0x89	0x00	HDMI EDG STATUS 4	r	MS_INF_CKS_ERR_ST	SPD_INF_CKS_ERR_ST	AUD_INF_CKS_ERR_ST	AVI_INF_CKS_ERR_ST	-	-	AKSV_UPDATE_A_ST	AKSV_UPDATE_B_ST
0x8A	0x00	HDMI EDG INT CLR 4	sc	MS_INF_CKS_ERR_CLR	SPD_INF_CKS_ERR_CLR	AUD_INF_CKS_ERR_CLR	AVI_INF_CKS_ERR_CLR	-	-	AKSV_UPDATE_A_CLR	AKSV_UPDATE_B_CLR
0x8B	0x00	HDMI EDG INT2 MASKB 4	rw	MS_INF_CKS_ERR_MB2	SPD_INF_CKS_ERR_MB2	AUD_INF_CKS_ERR_MB2	AVI_INF_CKS_ERR_MB2	-	-	AKSV_UPDATE_A_MB2	AKSV_UPDATE_B_MB2
0x8C	0x00	HDMI EDG INT MASKB 4	rw	MS_INF_CKS_ERR_MB1	SPD_INF_CKS_ERR_MB1	AUD_INF_CKS_ERR_MB1	AVI_INF_CKS_ERR_MB1	-	-	AKSV_UPDATE_A_MB1	AKSV_UPDATE_B_MB1
0x8D	0x00	HDMI EDG RAW STATUS 5	r	-	-	-	-	-	-	BG_MEAS_DONE_RAW	VS_INF_CKS_ERR_RAW
0x8E	0x00	HDMI EDG STATUS 5	r	-	-	-	-	-	-	BG_MEAS_DONE_ST	VS_INF_CKS_ERR_ST
0x8F	0x00	HDMI EDG INT CLR 5	sc	-	-	-	-	-	-	BG_MEAS_DONE_CLR	VS_INF_CKS_ERR_CLR
0x90	0x00	HDMI EDG INT2 MASKB 5	rw	-	-	-	-	-	-	BG_MEAS_DONE_MB2	VS_INF_CKS_ERR_MB2
0x91	0x00	HDMI EDG INT MASKB 5	rw	-	-	-	-	-	-	BG_MEAS_DONE_MB1	VS_INF_CKS_ERR_MB1
0x92	0x00	CEC_STATUS1_RAW	r	-	-	CEC_RX_RDY2_RAW	CEC_RX_RDY1_RAW	CEC_RX_RDY0_RAW	CEC_TX_RETRY_TIMEOUT_RAW	CEC_TX_ARBITRATION_LOST_RAW	CEC_TX_READY_RAW
0x93	0x00	CEC_STATUS1_INT_STATUS	r	-	-	CEC_RX_RDY2_ST	CEC_RX_RDY1_ST	CEC_RX_RDY0_ST	CEC_TX_RETRY_TIMEOUT_ST	CEC_TX_ARBITRATION_LOST_ST	CEC_TX_READY_ST
0x94	0x00	CEC_STATUS1_INT_CLEAR	sc	-	-	CEC_RX_RDY2_CLR	CEC_RX_RDY1_CLR	CEC_RX_RDY0_CLR	CEC_TX_RETRY_TIMEOUT_CLR	CEC_TX_ARBITRATION_LOST_CLR	CEC_TX_READY_CLR
0x95	0x00	CEC_STATUS1_INT2_MASKB	rw	-	-	CEC_RX_RDY2_MB2	CEC_RX_RDY1_MB2	CEC_RX_RDY0_MB2	CEC_TX_RETRY_TIMEOUT_MB2	CEC_TX_ARBITRATION_LOST_MB2	CEC_TX_READY_MB2
0x96	0x00	CEC_STATUS1_INT1_MASKB	rw	-	-	CEC_RX_RDY2_MB1	CEC_RX_RDY1_MB1	CEC_RX_RDY0_MB1	CEC_TX_RETRY_TIMEOUT_MB1	CEC_TX_ARBITRATION_LOST_MB1	CEC_TX_READY_MB1
0x97	0x00	CEC_STATUS2_RAW	r	CEC_INT_WAKE_OPCODE7_RAW	CEC_INT_WAKE_OPCODE6_RAW	CEC_INT_WAKE_OPCODE5_RAW	CEC_INT_WAKE_OPCODE4_RAW	CEC_INT_WAKE_OPCODE3_RAW	CEC_INT_WAKE_OPCODE2_RAW	CEC_INT_WAKE_OPCODE1_RAW	CEC_INT_WAKE_OPCODE0_RAW
0x98	0x00	CEC_STATUS2_INT_STATUS	r	CEC_INT_WAKE_OPCODE7_ST	CEC_INT_WAKE_OPCODE6_ST	CEC_INT_WAKE_OPCODE5_ST	CEC_INT_WAKE_OPCODE4_ST	CEC_INT_WAKE_OPCODE3_ST	CEC_INT_WAKE_OPCODE2_ST	CEC_INT_WAKE_OPCODE1_ST	CEC_INT_WAKE_OPCODE0_ST
0x99	0x00	CEC_STATUS2_INT_CLEAR	sc	CEC_INT_WAKE_OPCODE7_CLR	CEC_INT_WAKE_OPCODE6_CLR	CEC_INT_WAKE_OPCODE5_CLR	CEC_INT_WAKE_OPCODE4_CLR	CEC_INT_WAKE_OPCODE3_CLR	CEC_INT_WAKE_OPCODE2_CLR	CEC_INT_WAKE_OPCODE1_CLR	CEC_INT_WAKE_OPCODE0_CLR
0x9A	0x00	CEC_STATUS_INT2_MASKB	rw	CEC_INT_WAKE_OPCODE7_MB2	CEC_INT_WAKE_OPCODE6_MB2	CEC_INT_WAKE_OPCODE5_MB2	CEC_INT_WAKE_OPCODE4_MB2	CEC_INT_WAKE_OPCODE3_MB2	CEC_INT_WAKE_OPCODE2_MB2	CEC_INT_WAKE_OPCODE1_MB2	CEC_INT_WAKE_OPCODE0_MB2
0x9B	0x00	CEC_STATUS_INT1_MASKB	rw	CEC_INT_WAKE_OPCODE7_MB1	CEC_INT_WAKE_OPCODE6_MB1	CEC_INT_WAKE_OPCODE5_MB1	CEC_INT_WAKE_OPCODE4_MB1	CEC_INT_WAKE_OPCODE3_MB1	CEC_INT_WAKE_OPCODE2_MB1	CEC_INT_WAKE_OPCODE1_MB1	CEC_INT_WAKE_OPCODE0_MB1
0x9C	0x00	SDP_RAW_STATUS	r	-	-	-	-	SDP_STD_CHANGED_RAW	-	SDP_BURST_LOCKED_RAW	SDP_VIDEO_DETECTED_RAW
0x9D	0x00	SDP_INTERRUPT_STATUS	r	-	-	-	-	SDP_STD_CHANGED_ST	-	SDP_BURST_LOCKED_ST	SDP_VIDEO_DETECTED_ST
0x9E	0x00	SDP_INTERRUPT_CLEAR	sc	-	-	-	-	SDP_STD_CHANGED_CLR	-	SDP_BURST_LOCKED_CLR	SDP_VIDEO_DETECTED_CLR

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9F	0x00	SDP_INTERRUPT2_MASKB	rw	-	-	-	-	SDP_STD_CHANGED_MB2	-	SDP_BURST_LOCKED_MB2	SDP_VIDEO_DETECTED_MB2
0xA0	0x00	SDP_INTERRUPT_MASKB	rw	-	-	-	-	SDP_STD_CHANGED_MB1	SDP_FIFO_CRISIS_MB1	SDP_BURST_LOCKED_MB1	SDP_VIDEO_DETECTED_MB1
0xD6	0x00	IO_REG_D6	rw	-	-	-	-	-	-	-	PIN_CHECKER_EN
0xD7	0x00	IO_REG_D7	rw	PIN_CHECKER_VAL[7]	PIN_CHECKER_VAL[6]	PIN_CHECKER_VAL[5]	PIN_CHECKER_VAL[4]	PIN_CHECKER_VAL[3]	PIN_CHECKER_VAL[2]	PIN_CHECKER_VAL[1]	PIN_CHECKER_VAL[0]
0xDD	0x00		rw	MAN_OP_CLK_SEL_EN	MAN_OP_CLK_SEL[2]	MAN_OP_CLK_SEL[1]	MAN_OP_CLK_SEL[0]	-	-	-	-
0xE0	0x00	IO_REG_E0	rw	DS_WITHOUT_FILTER	-	-	-	-	-	-	-
0xE7	0x00	IO_REG_E7	rw	-	-	DPP_LUMA_HBW_SEL	DPP_CHROMA_LOW_EN	-	-	-	-
0xEA	0x00		r	RD_INFO[15]	RD_INFO[14]	RD_INFO[13]	RD_INFO[12]	RD_INFO[11]	RD_INFO[10]	RD_INFO[9]	RD_INFO[8]
0xEB	0x00		r	RD_INFO[7]	RD_INFO[6]	RD_INFO[5]	RD_INFO[4]	RD_INFO[3]	RD_INFO[2]	RD_INFO[1]	RD_INFO[0]
0xF1	0x00	SDP SLAVE ADDRESS	rw	SDP_SLAVE_ADDR[6]	SDP_SLAVE_ADDR[5]	SDP_SLAVE_ADDR[4]	SDP_SLAVE_ADDR[3]	SDP_SLAVE_ADDR[2]	SDP_SLAVE_ADDR[1]	SDP_SLAVE_ADDR[0]	-
0xF2	0x00	SDP_IO SLAVE ADDRESS	rw	SDP_IO_SLAVE_ADDR[6]	SDP_IO_SLAVE_ADDR[5]	SDP_IO_SLAVE_ADDR[4]	SDP_IO_SLAVE_ADDR[3]	SDP_IO_SLAVE_ADDR[2]	SDP_IO_SLAVE_ADDR[1]	SDP_IO_SLAVE_ADDR[0]	-
0xF3	0x00	AVLINK SLAVE ADDRESS	rw	AVLINK_SLAVE_ADDR[6]	AVLINK_SLAVE_ADDR[5]	AVLINK_SLAVE_ADDR[4]	AVLINK_SLAVE_ADDR[3]	AVLINK_SLAVE_ADDR[2]	AVLINK_SLAVE_ADDR[1]	AVLINK_SLAVE_ADDR[0]	-
0xF4	0x00	CEC SLAVE ADDRESS	rw	CEC_SLAVE_ADDR[6]	CEC_SLAVE_ADDR[5]	CEC_SLAVE_ADDR[4]	CEC_SLAVE_ADDR[3]	CEC_SLAVE_ADDR[2]	CEC_SLAVE_ADDR[1]	CEC_SLAVE_ADDR[0]	-
0xF5	0x00	INFOFRAME SLAVE ADDRESS	rw	INFOFRAME_SLAVE_ADDR[6]	INFOFRAME_SLAVE_ADDR[5]	INFOFRAME_SLAVE_ADDR[4]	INFOFRAME_SLAVE_ADDR[3]	INFOFRAME_SLAVE_ADDR[2]	INFOFRAME_SLAVE_ADDR[1]	INFOFRAME_SLAVE_ADDR[0]	-
0xF8	0x00	AFE SLAVE ADDRESS	rw	AFE_SLAVE_ADDR[6]	AFE_SLAVE_ADDR[5]	AFE_SLAVE_ADDR[4]	AFE_SLAVE_ADDR[3]	AFE_SLAVE_ADDR[2]	AFE_SLAVE_ADDR[1]	AFE_SLAVE_ADDR[0]	-
0xF9	0x00	KSV SLAVE ADDRESS	rw	KSV_SLAVE_ADDR[6]	KSV_SLAVE_ADDR[5]	KSV_SLAVE_ADDR[4]	KSV_SLAVE_ADDR[3]	KSV_SLAVE_ADDR[2]	KSV_SLAVE_ADDR[1]	KSV_SLAVE_ADDR[0]	-
0xFA	0x00	EDID SLAVE ADDRESS	rw	EDID_SLAVE_ADDR[6]	EDID_SLAVE_ADDR[5]	EDID_SLAVE_ADDR[4]	EDID_SLAVE_ADDR[3]	EDID_SLAVE_ADDR[2]	EDID_SLAVE_ADDR[1]	EDID_SLAVE_ADDR[0]	-
0xFB	0x00	HDMI SLAVE ADDRESS	rw	HDMI_SLAVE_ADDR[6]	HDMI_SLAVE_ADDR[5]	HDMI_SLAVE_ADDR[4]	HDMI_SLAVE_ADDR[3]	HDMI_SLAVE_ADDR[2]	HDMI_SLAVE_ADDR[1]	HDMI_SLAVE_ADDR[0]	-
0xFD	0x00	CP SLAVE ADDRESS	rw	CP_SLAVE_ADDR[6]	CP_SLAVE_ADDR[5]	CP_SLAVE_ADDR[4]	CP_SLAVE_ADDR[3]	CP_SLAVE_ADDR[2]	CP_SLAVE_ADDR[1]	CP_SLAVE_ADDR[0]	-
0xFE	0x00	VDP SLAVE ADDRESS	rw	VDP_SLAVE_ADDR[6]	VDP_SLAVE_ADDR[5]	VDP_SLAVE_ADDR[4]	VDP_SLAVE_ADDR[3]	VDP_SLAVE_ADDR[2]	VDP_SLAVE_ADDR[1]	VDP_SLAVE_ADDR[0]	-
0xFF	0x00	IO_REG_FF	sc	MAIN_RESET	-	VDP_RESET	-	SDP_RESET	SDP_MEM_RESET	-	-

1.2 CP MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x0B	0x00	CSC_COEFF_RB_1	r	RB_CSC_SCALE[1]	RB_CSC_SCALE[0]	-	RB_A4[12]	RB_A4[11]	RB_A4[10]	RB_A4[9]	RB_A4[8]
0x0C	0x00	CSC_COEFF_RB_2	r	RB_A4[7]	RB_A4[6]	RB_A4[5]	RB_A4[4]	RB_A4[3]	RB_A4[2]	RB_A4[1]	RB_A4[0]
0x0D	0x00	CSC_COEFF_RB_3	r	-	RB_A3[12]	RB_A3[11]	RB_A3[10]	RB_A3[9]	RB_A3[8]	RB_A3[7]	RB_A3[6]
0x0E	0x00	CSC_COEFF_RB_4	r	RB_A3[5]	RB_A3[4]	RB_A3[3]	RB_A3[2]	RB_A3[1]	RB_A3[0]	RB_A2[12]	RB_A2[11]
0x0F	0x00	CSC_COEFF_RB_5	r	RB_A2[10]	RB_A2[9]	RB_A2[8]	RB_A2[7]	RB_A2[6]	RB_A2[5]	RB_A2[4]	RB_A2[3]
0x10	0x00	CSC_COEFF_RB_6	r	RB_A2[2]	RB_A2[1]	RB_A2[0]	RB_A1[12]	RB_A1[11]	RB_A1[10]	RB_A1[9]	RB_A1[8]
0x11	0x00	CSC_COEFF_RB_7	r	RB_A1[7]	RB_A1[6]	RB_A1[5]	RB_A1[4]	RB_A1[3]	RB_A1[2]	RB_A1[1]	RB_A1[0]
0x12	0x00	CSC_COEFF_RB_8	r	-	-	-	RB_B4[12]	RB_B4[11]	RB_B4[10]	RB_B4[9]	RB_B4[8]
0x13	0x00	CSC_COEFF_RB_9	r	RB_B4[7]	RB_B4[6]	RB_B4[5]	RB_B4[4]	RB_B4[3]	RB_B4[2]	RB_B4[1]	RB_B4[0]
0x14	0x00	CSC_COEFF_RB_10	r	-	RB_B3[12]	RB_B3[11]	RB_B3[10]	RB_B3[9]	RB_B3[8]	RB_B3[7]	RB_B3[6]
0x15	0x00	CSC_COEFF_RB_11	r	RB_B3[5]	RB_B3[4]	RB_B3[3]	RB_B3[2]	RB_B3[1]	RB_B3[0]	RB_B2[12]	RB_B2[11]
0x16	0x00	CSC_COEFF_RB_12	r	RB_B2[10]	RB_B2[9]	RB_B2[8]	RB_B2[7]	RB_B2[6]	RB_B2[5]	RB_B2[4]	RB_B2[3]
0x17	0x00	CSC_COEFF_RB_13	r	RB_B2[2]	RB_B2[1]	RB_B2[0]	RB_B1[12]	RB_B1[11]	RB_B1[10]	RB_B1[9]	RB_B1[8]
0x18	0x00	CSC_COEFF_RB_14	r	RB_B1[7]	RB_B1[6]	RB_B1[5]	RB_B1[4]	RB_B1[3]	RB_B1[2]	RB_B1[1]	RB_B1[0]
0x19	0x00	CSC_COEFF_RB_15	r	-	-	-	RB_C4[12]	RB_C4[11]	RB_C4[10]	RB_C4[9]	RB_C4[8]
0x1A	0x00	CSC_COEFF_RB_16	r	RB_C4[7]	RB_C4[6]	RB_C4[5]	RB_C4[4]	RB_C4[3]	RB_C4[2]	RB_C4[1]	RB_C4[0]
0x1B	0x00	CSC_COEFF_RB_17	r	-	RB_C3[12]	RB_C3[11]	RB_C3[10]	RB_C3[9]	RB_C3[8]	RB_C3[7]	RB_C3[6]
0x1C	0x00	CSC_COEFF_RB_18	r	RB_C3[5]	RB_C3[4]	RB_C3[3]	RB_C3[2]	RB_C3[1]	RB_C3[0]	RB_C2[12]	RB_C2[11]
0x1D	0x00	CSC_COEFF_RB_19	r	RB_C2[10]	RB_C2[9]	RB_C2[8]	RB_C2[7]	RB_C2[6]	RB_C2[5]	RB_C2[4]	RB_C2[3]
0x1E	0x00	CSC_COEFF_RB_20	r	RB_C2[2]	RB_C2[1]	RB_C2[0]	RB_C1[12]	RB_C1[11]	RB_C1[10]	RB_C1[9]	RB_C1[8]
0x1F	0x00	CSC_COEFF_RB_21	r	RB_C1[7]	RB_C1[6]	RB_C1[5]	RB_C1[4]	RB_C1[3]	RB_C1[2]	RB_C1[1]	RB_C1[0]
0x22	0x00	HS_POS_CNTRL_1	rw	-	-	-	CP_START_HS[12]	CP_START_HS[11]	CP_START_HS[10]	CP_START_HS[9]	CP_START_HS[8]
0x23	0x00	HS_POS_CNTRL_2	rw	CP_START_HS[7]	CP_START_HS[6]	CP_START_HS[5]	CP_START_HS[4]	CP_START_HS[3]	CP_START_HS[2]	CP_START_HS[1]	CP_START_HS[0]
0x24	0x00	HS_POS_CNTRL_3	rw	-	-	-	CP_END_HS[12]	CP_END_HS[11]	CP_END_HS[10]	CP_END_HS[9]	CP_END_HS[8]
0x25	0x00	HS_POS_CNTRL_4	rw	CP_END_HS[7]	CP_END_HS[6]	CP_END_HS[5]	CP_END_HS[4]	CP_END_HS[3]	CP_END_HS[2]	CP_END_HS[1]	CP_END_HS[0]
0x26	0x00	DE_POS_CNTRL_1	rw	-	-	-	CP_START_SAV[12]	CP_START_SAV[11]	CP_START_SAV[10]	CP_START_SAV[9]	CP_START_SAV[8]
0x27	0x00	DE_POS_CNTRL_2	rw	CP_START_SAV[7]	CP_START_SAV[6]	CP_START_SAV[5]	CP_START_SAV[4]	CP_START_SAV[3]	CP_START_SAV[2]	CP_START_SAV[1]	CP_START_SAV[0]
0x28	0x00	DE_POS_CNTRL_3	rw	-	-	-	CP_START_EAV[12]	CP_START_EAV[11]	CP_START_EAV[10]	CP_START_EAV[9]	CP_START_EAV[8]
0x29	0x00	DE_POS_CNTRL_4	rw	CP_START_EAV[7]	CP_START_EAV[6]	CP_START_EAV[5]	CP_START_EAV[4]	CP_START_EAV[3]	CP_START_EAV[2]	CP_START_EAV[1]	CP_START_EAV[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2A	0x00	DE_POS_CNTRL_5	rw	CP_START_VBI_R[11]	CP_START_VBI_R[10]	CP_START_VBI_R[9]	CP_START_VBI_R[8]	CP_START_VBI_R[7]	CP_START_VBI_R[6]	CP_START_VBI_R[5]	CP_START_VBI_R[4]
0x2B	0x00	DE_POS_CNTRL_6	rw	CP_START_VBI_R[3]	CP_START_VBI_R[2]	CP_START_VBI_R[1]	CP_START_VBI_R[0]	CP_END_VBI_R[11]	CP_END_VBI_R[10]	CP_END_VBI_R[9]	CP_END_VBI_R[8]
0x2C	0x00	DE_POS_CNTRL_7	rw	CP_END_VBI_R[7]	CP_END_VBI_R[6]	CP_END_VBI_R[5]	CP_END_VBI_R[4]	CP_END_VBI_R[3]	CP_END_VBI_R[2]	CP_END_VBI_R[1]	CP_END_VBI_R[0]
0x2D	0x00	DE_POS_CNTRL_8	rw	CP_START_VBI_EVEN_R[11]	CP_START_VBI_EVEN_R[10]	CP_START_VBI_EVEN_R[9]	CP_START_VBI_EVEN_R[8]	CP_START_VBI_EVEN_R[7]	CP_START_VBI_EVEN_R[6]	CP_START_VBI_EVEN_R[5]	CP_START_VBI_EVEN_R[4]
0x2E	0x00	DE_POS_CNTRL_9	rw	CP_START_VBI_EVEN_R[3]	CP_START_VBI_EVEN_R[2]	CP_START_VBI_EVEN_R[1]	CP_START_VBI_EVEN_R[0]	CP_END_VBI_EVEN_R[11]	CP_END_VBI_EVEN_R[10]	CP_END_VBI_EVEN_R[9]	CP_END_VBI_EVEN_R[8]
0x2F	0x00	DE_POS_CNTRL_10	rw	CP_END_VBI_EVEN_R[7]	CP_END_VBI_EVEN_R[6]	CP_END_VBI_EVEN_R[5]	CP_END_VBI_EVEN_R[4]	CP_END_VBI_EVEN_R[3]	CP_END_VBI_EVEN_R[2]	CP_END_VBI_EVEN_R[1]	CP_END_VBI_EVEN_R[0]
0x30	0x00	DE_POS_ADJ_1	rw	DE_V_START_R[3]	DE_V_START_R[2]	DE_V_START_R[1]	DE_V_START_R[0]	DE_V_END_R[3]	DE_V_END_R[2]	DE_V_END_R[1]	DE_V_END_R[0]
0x31	0x00	DE_POS_ADJ_2	rw	DE_V_START_EVEN_R[3]	DE_V_START_EVEN_R[2]	DE_V_START_EVEN_R[1]	DE_V_START_EVEN_R[0]	DE_V_END_EVEN_R[3]	DE_V_END_EVEN_R[2]	DE_V_END_EVEN_R[1]	DE_V_END_EVEN_R[0]
0x36	0x00	BIT_REDUCTION_DITHER	rw	-	-	BR_NOISE_SHAPING_EN	BR_NOISE_SHAPING_MODE	BR_NOISE_SHAPING_GAIN[1]	BR_NOISE_SHAPING_GAIN[0]	-	TEN_TO_EIGHT_CONV
0x3A	0x80	CONTRAST_CNTRL	rw	CP_CONTRAST[7]	CP_CONTRAST[6]	CP_CONTRAST[5]	CP_CONTRAST[4]	CP_CONTRAST[3]	CP_CONTRAST[2]	CP_CONTRAST[1]	CP_CONTRAST[0]
0x3B	0x80	SATURATION_CNTRL	rw	CP_SATURATION[7]	CP_SATURATION[6]	CP_SATURATION[5]	CP_SATURATION[4]	CP_SATURATION[3]	CP_SATURATION[2]	CP_SATURATION[1]	CP_SATURATION[0]
0x3C	0x00	BRIGHTNESS_CNTRL	rw	CP_BRIGHTNESS[7]	CP_BRIGHTNESS[6]	CP_BRIGHTNESS[5]	CP_BRIGHTNESS[4]	CP_BRIGHTNESS[3]	CP_BRIGHTNESS[2]	CP_BRIGHTNESS[1]	CP_BRIGHTNESS[0]
0x3D	0x00	HUE_CNTRL	rw	CP_HUE[7]	CP_HUE[6]	CP_HUE[5]	CP_HUE[4]	CP_HUE[3]	CP_HUE[2]	CP_HUE[1]	CP_HUE[0]
0x3E	0x04		rw	VID_ADJ_EN	-	CP_UV_ALIGN_SEL[1]	CP_UV_ALIGN_SEL[0]	CP_UV_DVAL_INV	CP_MODE_GAIN_ADJ_EN	ALT_SAT_UV_MAN	ALT_SAT_UV
0x40	0x5C	CP_PRE_GAIN_CNTRL	rw	CP_MODE_GAIN_ADJ[7]	CP_MODE_GAIN_ADJ[6]	CP_MODE_GAIN_ADJ[5]	CP_MODE_GAIN_ADJ[4]	CP_MODE_GAIN_ADJ[3]	CP_MODE_GAIN_ADJ[2]	CP_MODE_GAIN_ADJ[1]	CP_MODE_GAIN_ADJ[0]
0x41	0x02	SYNC_DET_CNTRL_CH2_1	rw	CH2_POL_MAN_EN	CH2_POL_VS	CH2_POL_HSCS	CH2_SYNC_SRC[1]	CH2_SYNC_SRC[0]	CH2_TRIG_SSPD	CH2_SSPD_CONT	CH2_SSPD_PP_EN
0x42	0x3B	SYNC_DET_CNTRL_CH2_2	rw	-	-	-	-	-	CH2_TRIG_STDI	CH2_STDI_CONT	-
0x43	0xD4	SYNC_DET_CNTRL_CH2_3	rw	-	-	CH2_FL_FR_THRESHOLD[2]	CH2_FL_FR_THRESHOLD[1]	CH2_FL_FR_THRESHOLD[0]	CH2_F_RUN_THR[2]	CH2_F_RUN_THR[1]	CH2_F_RUN_THR[0]
0x46	0x00	SYNC_DET_CNTRL_CH2_6	rw	CH2_FR_FIELD_LENGTH[10]	CH2_FR_FIELD_LENGTH[9]	CH2_FR_FIELD_LENGTH[8]	CH2_FR_FIELD_LENGTH[7]	CH2_FR_FIELD_LENGTH[6]	CH2_FR_FIELD_LENGTH[5]	CH2_FR_FIELD_LENGTH[4]	CH2_FR_FIELD_LENGTH[3]
0x47	0x00	SYNC_DET_CNTRL_CH2_7	rw	CH2_FR_FIELD_LENGTH[2]	CH2_FR_FIELD_LENGTH[1]	CH2_FR_FIELD_LENGTH[0]	-	-	CH2_FR_LL[10]	CH2_FR_LL[9]	CH2_FR_LL[8]
0x48	0x00	SYNC_DET_CNTRL_CH2_8	rw	CH2_FR_LL[7]	CH2_FR_LL[6]	CH2_FR_LL[5]	CH2_FR_LL[4]	CH2_FR_LL[3]	CH2_FR_LL[2]	CH2_FR_LL[1]	CH2_FR_LL[0]
0x49	0x00	SYNC_DET_CNTRL_CH2_RB_1	r	CH2_STDI_DVALID	CH2_STDI_INTLCD	CH2_BL[13]	CH2_BL[12]	CH2_BL[11]	CH2_BL[10]	CH2_BL[9]	CH2_BL[8]
0x4A	0x00	SYNC_DET_CNTRL_CH2_RB_2	r	CH2_BL[7]	CH2_BL[6]	CH2_BL[5]	CH2_BL[4]	CH2_BL[3]	CH2_BL[2]	CH2_BL[1]	CH2_BL[0]
0x4B	0x00	SYNC_DET_CNTRL_CH2_RB_3	r	CH2_LCVS[4]	CH2_LCVS[3]	CH2_LCVS[2]	CH2_LCVS[1]	CH2_LCVS[0]	CH2_LCF[10]	CH2_LCF[9]	CH2_LCF[8]
0x4C	0x00	SYNC_DET_CNTRL_CH2_RB_4	r	CH2_LCF[7]	CH2_LCF[6]	CH2_LCF[5]	CH2_LCF[4]	CH2_LCF[3]	CH2_LCF[2]	CH2_LCF[1]	CH2_LCF[0]
0x4D	0x00	SYNC_DET_CNTRL_CH2_RB_5	r	-	-	-	CH2_FCL[12]	CH2_FCL[11]	CH2_FCL[10]	CH2_FCL[9]	CH2_FCL[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x4E	0x00	SYNC_DET_CNTRL_CH2_RB_6	r	CH2_FCL[7]	CH2_FCL[6]	CH2_FCL[5]	CH2_FCL[4]	CH2_FCL[3]	CH2_FCL[2]	CH2_FCL[1]	CH2_FCL[0]
0x4F	0x00	SYNC_DET_CNTRL_CH2_RB_7	r	CH2_SSPD_DVALID	CH2_VS_ACT	CH2_CUR_POL_VS	CH2_HS_ACT	CH2_CUR_POL_HS	CH2_RS_ACTIVE	CH2_CUR_SYNC_SRC[1]	CH2_CUR_SYNC_SRC[0]
0x52	0x40	CSC_COEFFS_1	rw	CSC_SCALE[1]	CSC_SCALE[0]	-	A4[12]	A4[11]	A4[10]	A4[9]	A4[8]
0x53	0x00	CSC_COEFFS_2	rw	A4[7]	A4[6]	A4[5]	A4[4]	A4[3]	A4[2]	A4[1]	A4[0]
0x54	0x00	CSC_COEFFS_3	rw	-	A3[12]	A3[11]	A3[10]	A3[9]	A3[8]	A3[7]	A3[6]
0x55	0x00	CSC_COEFFS_4	rw	A3[5]	A3[4]	A3[3]	A3[2]	A3[1]	A3[0]	A2[12]	A2[11]
0x56	0x00	CSC_COEFFS_5	rw	A2[10]	A2[9]	A2[8]	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]
0x57	0x08	CSC_COEFFS_6	rw	A2[2]	A2[1]	A2[0]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
0x58	0x00	CSC_COEFFS_7	rw	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
0x59	0x00	CSC_COEFFS_8	rw	-	-	-	B4[12]	B4[11]	B4[10]	B4[9]	B4[8]
0x5A	0x00	CSC_COEFFS_9	rw	B4[7]	B4[6]	B4[5]	B4[4]	B4[3]	B4[2]	B4[1]	B4[0]
0x5B	0x00	CSC_COEFFS_10	rw	-	B3[12]	B3[11]	B3[10]	B3[9]	B3[8]	B3[7]	B3[6]
0x5C	0x01	CSC_COEFFS_11	rw	B3[5]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	B2[12]	B2[11]
0x5D	0x00	CSC_COEFFS_12	rw	B2[10]	B2[9]	B2[8]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]
0x5E	0x00	CSC_COEFFS_13	rw	B2[2]	B2[1]	B2[0]	B1[12]	B1[11]	B1[10]	B1[9]	B1[8]
0x5F	0x00	CSC_COEFFS_14	rw	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
0x60	0x00	CSC_COEFFS_15	rw	-	-	-	C4[12]	C4[11]	C4[10]	C4[9]	C4[8]
0x61	0x00	CSC_COEFFS_16	rw	C4[7]	C4[6]	C4[5]	C4[4]	C4[3]	C4[2]	C4[1]	C4[0]
0x62	0x20	CSC_COEFFS_17	rw	-	C3[12]	C3[11]	C3[10]	C3[9]	C3[8]	C3[7]	C3[6]
0x63	0x00	CSC_COEFFS_18	rw	C3[5]	C3[4]	C3[3]	C3[2]	C3[1]	C3[0]	C2[12]	C2[11]
0x64	0x00	CSC_COEFFS_19	rw	C2[10]	C2[9]	C2[8]	C2[7]	C2[6]	C2[5]	C2[4]	C2[3]
0x65	0x00	CSC_COEFFS_20	rw	C2[2]	C2[1]	C2[0]	C1[12]	C1[11]	C1[10]	C1[9]	C1[8]
0x66	0x00	CSC_COEFFS_21	rw	C1[7]	C1[6]	C1[5]	C1[4]	C1[3]	C1[2]	C1[1]	C1[0]
0x67	0x00		rw	-	-	EMB_SYNC_ON_ALL	-	-	-	-	-
0x68	0xF0	CSC_DECIM_CNTRL	rw	CSC_COEFF_SEL[3]	CSC_COEFF_SEL[2]	CSC_COEFF_SEL[1]	CSC_COEFF_SEL[0]	CP_CHROMA_LOW_EN	-	-	-
0x69	0x04		rw	-	-	-	MAN_CP_CSC_EN	-	EIA_861_COMPLIANCE	-	-
0x6C	0x10	CLMP_CNTRL_1	rw	CLMP_A_MAN	CLMP_BC_MAN	CLMP_FREEZE	-	CLMP_A[11]	CLMP_A[10]	CLMP_A[9]	CLMP_A[8]
0x6D	0x00	CLMP_CNTRL_2	rw	CLMP_A[7]	CLMP_A[6]	CLMP_A[5]	CLMP_A[4]	CLMP_A[3]	CLMP_A[2]	CLMP_A[1]	CLMP_A[0]
0x6E	0x00	CLMP_CNTRL_3	rw	CLMP_B[11]	CLMP_B[10]	CLMP_B[9]	CLMP_B[8]	CLMP_B[7]	CLMP_B[6]	CLMP_B[5]	CLMP_B[4]
0x6F	0x00	CLMP_CNTRL_4	rw	CLMP_B[3]	CLMP_B[2]	CLMP_B[1]	CLMP_B[0]	CLMP_C[11]	CLMP_C[10]	CLMP_C[9]	CLMP_C[8]
0x70	0x00	CLMP_CNTRL_5	rw	CLMP_C[7]	CLMP_C[6]	CLMP_C[5]	CLMP_C[4]	CLMP_C[3]	CLMP_C[2]	CLMP_C[1]	CLMP_C[0]
0x71	0x00	GAIN_CNTRL_1	rw	AGC_TAR[9]	AGC_TAR[8]	AGC_TAR_MAN	AGC_FREEZE	HS_NORM	AGC_TIM[2]	AGC_TIM[1]	AGC_TIM[0]
0x72	0x00	GAIN_CNTRL_2	rw	AGC_TAR[7]	AGC_TAR[6]	AGC_TAR[5]	AGC_TAR[4]	AGC_TAR[3]	AGC_TAR[2]	AGC_TAR[1]	AGC_TAR[0]
0x73	0x10	GAIN_CNTRL_3	rw	GAIN_MAN	AGC_MODE_MAN	A_GAIN[9]	A_GAIN[8]	A_GAIN[7]	A_GAIN[6]	A_GAIN[5]	A_GAIN[4]
0x74	0x04	GAIN_CNTRL_4	rw	A_GAIN[3]	A_GAIN[2]	A_GAIN[1]	A_GAIN[0]	B_GAIN[9]	B_GAIN[8]	B_GAIN[7]	B_GAIN[6]
0x75	0x01	GAIN_CNTRL_5	rw	B_GAIN[5]	B_GAIN[4]	B_GAIN[3]	B_GAIN[2]	B_GAIN[1]	B_GAIN[0]	C_GAIN[9]	C_GAIN[8]
0x76	0x00	GAIN_CNTRL_6	rw	C_GAIN[7]	C_GAIN[6]	C_GAIN[5]	C_GAIN[4]	C_GAIN[3]	C_GAIN[2]	C_GAIN[1]	C_GAIN[0]
0x77	0xFF	OFFSET_CNTRL_1	rw	CP_PREC[1]	CP_PREC[0]	A_OFFSET[9]	A_OFFSET[8]	A_OFFSET[7]	A_OFFSET[6]	A_OFFSET[5]	A_OFFSET[4]
0x78	0xFF	OFFSET_CNTRL_2	rw	A_OFFSET[3]	A_OFFSET[2]	A_OFFSET[1]	A_OFFSET[0]	B_OFFSET[9]	B_OFFSET[8]	B_OFFSET[7]	B_OFFSET[6]
0x79	0xFF	OFFSET_CNTRL_3	rw	B_OFFSET[5]	B_OFFSET[4]	B_OFFSET[3]	B_OFFSET[2]	B_OFFSET[1]	B_OFFSET[0]	C_OFFSET[9]	C_OFFSET[8]
0x7A	0xFF	OFFSET_CNTRL_4	rw	C_OFFSET[7]	C_OFFSET[6]	C_OFFSET[5]	C_OFFSET[4]	C_OFFSET[3]	C_OFFSET[2]	C_OFFSET[1]	C_OFFSET[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x7B	0x05	AVCODE_CNTRL	rw	AV_INV_F	AV_INV_V	-	-	-	AV_POS_SEL	-	DE_WITH_AVCODE
0x7C	0xC0	SYNC_CNTRL_1	rw	-	-	-	-	START_HS[9]	START_HS[8]	END_HS[9]	END_HS[8]
0x7D	0x00	SYNC_CNTRL_2	rw	END_HS[7]	END_HS[6]	END_HS[5]	END_HS[4]	END_HS[3]	END_HS[2]	END_HS[1]	END_HS[0]
0x7E	0x00	SYNC_CNTRL_3	rw	START_HS[7]	START_HS[6]	START_HS[5]	START_HS[4]	START_HS[3]	START_HS[2]	START_HS[1]	START_HS[0]
0x7F	0x00	SYNC_CNTRL_4	rw	START_VS[3]	START_VS[2]	START_VS[1]	START_VS[0]	END_VS[3]	END_VS[2]	END_VS[1]	END_VS[0]
0x80	0x00	SYNC_CNTRL_5	rw	START_FE[3]	START_FE[2]	START_FE[1]	START_FE[0]	START_FO[3]	START_FO[2]	START_FO[1]	START_FO[0]
0x81	0xC0	NOISE_CALIB_1	rw	MEAS_WL[1]	MEAS_WL[0]	-	GR_AV_BL_EN	MEAS_WS[11]	MEAS_WS[10]	MEAS_WS[9]	MEAS_WS[8]
0x82	0x04	NOISE_CALIB_2	rw	MEAS_WS[7]	MEAS_WS[6]	MEAS_WS[5]	MEAS_WS[4]	MEAS_WS[3]	MEAS_WS[2]	MEAS_WS[1]	MEAS_WS[0]
0x83	0x00	CP_REG_83	rw	ISD_THR[7]	ISD_THR[6]	ISD_THR[5]	ISD_THR[4]	ISD_THR[3]	ISD_THR[2]	ISD_THR[1]	ISD_THR[0]
0x84	0x0C	SYNC_DET_CNTRL_CH1_1	rw	CP_GAIN_FILT[3]	CP_GAIN_FILT[2]	CP_GAIN_FILT[1]	CP_GAIN_FILT[0]	-	-	CH1_SSPD_PP_EN	IFSD_AVG
0x85	0x03	SYNC_DET_CNTRL_CH1_2	rw	CH1_POL_MAN_EN	CH1_POL_VS	CH1_POL_HSCS	CH1_SYNC_SRC[1]	CH1_SYNC_SRC[0]	CH1_TRIG_SSPD	CH1_SSPD_CONT	DS_OUT
0x86	0x0B	SYNC_DET_CNTRL_CH1_3	rw	-	-	-	-	-	CH1_TRIG_STDI	CH1_STDI_CONT	-
0x88	0x00	DE_POS_ADJ_3	rw	DE_V_START_EVEN[3]	DE_V_START_EVEN[2]	DE_V_START_EVEN[1]	DE_V_START_EVEN[0]	DE_V_END_EVEN[3]	DE_V_END_EVEN[2]	DE_V_END_EVEN[1]	DE_V_END_EVEN[0]
0x89	0x00	SYNC_CNTRL_6	rw	START_VS_EVEN[3]	START_VS_EVEN[2]	START_VS_EVEN[1]	START_VS_EVEN[0]	END_VS_EVEN[3]	END_VS_EVEN[2]	END_VS_EVEN[1]	END_VS_EVEN[0]
0x8A	0x20	CLMP_CNTRL_6	rw	IGNR_CLMP_VS_MAR_END[4]	IGNR_CLMP_VS_MAR_END[3]	IGNR_CLMP_VS_MAR_END[2]	IGNR_CLMP_VS_MAR_END[1]	IGNR_CLMP_VS_MAR_END[0]	-	-	IGNR_CLMP_VS_MAR_START[4]
0x8B	0x40	DE_POS_ADJ_4	rw	IGNR_CLMP_VS_MAR_START[3]	IGNR_CLMP_VS_MAR_START[2]	IGNR_CLMP_VS_MAR_START[1]	IGNR_CLMP_VS_MAR_START[0]	DE_H_START[9]	DE_H_START[8]	DE_H_END[9]	DE_H_END[8]
0x8C	0x00	DE_POS_ADJ_5	rw	DE_H_END[7]	DE_H_END[6]	DE_H_END[5]	DE_H_END[4]	DE_H_END[3]	DE_H_END[2]	DE_H_END[1]	DE_H_END[0]
0x8D	0x00	DE_POS_ADJ_6	rw	DE_H_START[7]	DE_H_START[6]	DE_H_START[5]	DE_H_START[4]	DE_H_START[3]	DE_H_START[2]	DE_H_START[1]	DE_H_START[0]
0x8E	0x00	DE_POS_ADJ_7	rw	DE_V_START[3]	DE_V_START[2]	DE_V_START[1]	DE_V_START[0]	DE_V_END[3]	DE_V_END[2]	DE_V_END[1]	DE_V_END[0]
0x8F	0x40	SYNC_DET_CNTRL_CH1_4_1	rw	-	-	-	-	-	CH1_FR_LL[10]	CH1_FR_LL[9]	CH1_FR_LL[8]
0x90	0x00	SYNC_DET_CNTRL_CH1_4_2	rw	CH1_FR_LL[7]	CH1_FR_LL[6]	CH1_FR_LL[5]	CH1_FR_LL[4]	CH1_FR_LL[3]	CH1_FR_LL[2]	CH1_FR_LL[1]	CH1_FR_LL[0]
0x91	0x40		rw	-	INTERLACED	-	-	-	-	-	-
0x9A	0x00	VS_POS_CNTRL_1	rw	-	-	-	CP_START_VS[5]	CP_START_VS[4]	CP_START_VS[3]	CP_START_VS[2]	CP_START_VS[1]
0x9B	0x00	VS_POS_CNTRL_2	rw	CP_START_VS[0]	CP_END_VS[5]	CP_END_VS[4]	CP_END_VS[3]	CP_END_VS[2]	CP_END_VS[1]	CP_END_VS[0]	-
0x9C	0x00	VS_POS_CNTRL_3	rw	CP_START_VS_EVEN[10]	CP_START_VS_EVEN[9]	CP_START_VS_EVEN[8]	CP_START_VS_EVEN[7]	CP_START_VS_EVEN[6]	CP_START_VS_EVEN[5]	CP_START_VS_EVEN[4]	CP_START_VS_EVEN[3]
0x9D	0x00	VS_POS_CNTRL_4	rw	CP_START_VS_EVEN[2]	CP_START_VS_EVEN[1]	CP_START_VS_EVEN[0]	CP_END_VS_EVEN[10]	CP_END_VS_EVEN[9]	CP_END_VS_EVEN[8]	CP_END_VS_EVEN[7]	CP_END_VS_EVEN[6]
0x9E	0x00	VS_POS_CNTRL_5	rw	CP_END_VS_EVEN[5]	CP_END_VS_EVEN[4]	CP_END_VS_EVEN[3]	CP_END_VS_EVEN[2]	CP_END_VS_EVEN[1]	CP_END_VS_EVEN[0]	-	-
0x9F	0x00	FLD_POS_CNTRL_1	rw	CP_START_F_ODD[10]	CP_START_F_ODD[9]	CP_START_F_ODD[8]	CP_START_F_ODD[7]	CP_START_F_ODD[6]	CP_START_F_ODD[5]	CP_START_F_ODD[4]	CP_START_F_ODD[3]
0xA0	0x00	FLD_POS_CNTRL_2	rw	CP_START_F_ODD[2]	CP_START_F_ODD[1]	CP_START_F_ODD[0]	CP_START_F_EVEN[10]	CP_START_F_EVEN[9]	CP_START_F_EVEN[8]	CP_START_F_EVEN[7]	CP_START_F_EVEN[6]
0xA1	0x00	FLD_POS_CNTRL_3	rw	CP_START_F_EVEN[5]	CP_START_F_EVEN[4]	CP_START_F_EVEN[3]	CP_START_F_EVEN[2]	CP_START_F_EVEN[1]	CP_START_F_EVEN[0]	-	-
0xA5	0x00	VBI_POS_CNTRL_1	rw	CP_START_VBI[11]	CP_START_VBI[10]	CP_START_VBI[9]	CP_START_VBI[8]	CP_START_VBI[7]	CP_START_VBI[6]	CP_START_VBI[5]	CP_START_VBI[4]
0xA6	0x00	VBI_POS_CNTRL_2	rw	CP_START_VBI[3]	CP_START_VBI[2]	CP_START_VBI[1]	CP_START_VBI[0]	CP_END_VBI[11]	CP_END_VBI[10]	CP_END_VBI[9]	CP_END_VBI[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xA7	0x00	VBI_POS_CNTRL_3	rw	CP_END_VBI[7]	CP_END_VBI[6]	CP_END_VBI[5]	CP_END_VBI[4]	CP_END_VBI[3]	CP_END_VBI[2]	CP_END_VBI[1]	CP_END_VBI[0]
0xA8	0x00	VBI_POS_CNTRL_4	rw	CP_START_VBI_EVEN[11]	CP_START_VBI_EVEN[10]	CP_START_VBI_EVEN[9]	CP_START_VBI_EVEN[8]	CP_START_VBI_EVEN[7]	CP_START_VBI_EVEN[6]	CP_START_VBI_EVEN[5]	CP_START_VBI_EVEN[4]
0xA9	0x00	VBI_POS_CNTRL_5	rw	CP_START_VBI_EVEN[3]	CP_START_VBI_EVEN[2]	CP_START_VBI_EVEN[1]	CP_START_VBI_EVEN[0]	CP_END_VBI_EVEN[11]	CP_END_VBI_EVEN[10]	CP_END_VBI_EVEN[9]	CP_END_VBI_EVEN[8]
0xAA	0x00	VBI_POS_CNTRL_6	rw	CP_END_VBI_EVEN[7]	CP_END_VBI_EVEN[6]	CP_END_VBI_EVEN[5]	CP_END_VBI_EVEN[4]	CP_END_VBI_EVEN[3]	CP_END_VBI_EVEN[2]	CP_END_VBI_EVEN[1]	CP_END_VBI_EVEN[0]
0xAB	0x00	SYNC_DET_CNTRL_CH1_4	rw	CP_LCOUNT_MAX[11]	CP_LCOUNT_MAX[10]	CP_LCOUNT_MAX[9]	CP_LCOUNT_MAX[8]	CP_LCOUNT_MAX[7]	CP_LCOUNT_MAX[6]	CP_LCOUNT_MAX[5]	CP_LCOUNT_MAX[4]
0xAC	0x00	SYNC_DET_CNTRL_CH1_5	rw	CP_LCOUNT_MAX[3]	CP_LCOUNT_MAX[2]	CP_LCOUNT_MAX[1]	CP_LCOUNT_MAX[0]	-	-	-	-
0xB1	0x00	SYNC_DET_CNTRL_CH1_RB_1	r	CH1_STDI_DVALID	CH1_STDI_INTLCD	CH1_BL[13]	CH1_BL[12]	CH1_BL[11]	CH1_BL[10]	CH1_BL[9]	CH1_BL[8]
0xB2	0x00	SYNC_DET_CNTRL_CH1_RB_2	r	CH1_BL[7]	CH1_BL[6]	CH1_BL[5]	CH1_BL[4]	CH1_BL[3]	CH1_BL[2]	CH1_BL[1]	CH1_BL[0]
0xB3	0x00	SYNC_DET_CNTRL_CH1_RB_3	r	CH1_LCVS[4]	CH1_LCVS[3]	CH1_LCVS[2]	CH1_LCVS[1]	CH1_LCVS[0]	CH1_LCF[10]	CH1_LCF[9]	CH1_LCF[8]
0xB4	0x00	SYNC_DET_CNTRL_CH1_RB_4	r	CH1_LCF[7]	CH1_LCF[6]	CH1_LCF[5]	CH1_LCF[4]	CH1_LCF[3]	CH1_LCF[2]	CH1_LCF[1]	CH1_LCF[0]
0xB5	0x00	SYNC_DET_CNTRL_CH1_RB_5	r	CH1_SSPD_DVALID	CH1_VS_ACT	CH1_CUR_POL_VS	CH1_HS_ACT	CH1_CUR_POL_HS	CH1_RS_ACTIVE	CH1_CUR_SYNC_SRC[1]	CH1_CUR_SYNC_SRC[0]
0xB8	0x00	SYNC_DET_CNTRL_CH1_RB_6_1	r	-	-	-	CH1_FCL[12]	CH1_FCL[11]	CH1_FCL[10]	CH1_FCL[9]	CH1_FCL[8]
0xB9	0x00	SYNC_DET_CNTRL_CH1_RB_6_2	r	CH1_FCL[7]	CH1_FCL[6]	CH1_FCL[5]	CH1_FCL[4]	CH1_FCL[3]	CH1_FCL[2]	CH1_FCL[1]	CH1_FCL[0]
0xBA	0x01	HDMI_CP_CNTRL_1	rw	-	-	-	-	-	-	HDMI_FRUN_MODE	HDMI_FRUN_EN
0xBD	0x18	COAST_CNTRL_1	rw	-	-	-	DPP_BYPASS_EN	-	-	-	-
0xBE	0x00		rw	DLY_A	DLY_B	DLY_C	-	-	-	HCOUNT_ALIGN_ADJ[4]	HCOUNT_ALIGN_ADJ[3]
0xBF	0x12	FR_COLOR_SEL_1	rw	HCOUNT_ALIGN_ADJ[2]	HCOUNT_ALIGN_ADJ[1]	HCOUNT_ALIGN_ADJ[0]	-	-	CP_DEF_COL_MAN_VAL	CP_DEF_COL_AUTO	CP_FORCE_FREERUN
0xC0	0x00	FR_COLOR_SEL_2	rw	DEF_COL_CHA[7]	DEF_COL_CHA[6]	DEF_COL_CHA[5]	DEF_COL_CHA[4]	DEF_COL_CHA[3]	DEF_COL_CHA[2]	DEF_COL_CHA[1]	DEF_COL_CHA[0]
0xC1	0x00	FR_COLOR_SEL_3	rw	DEF_COL_CHB[7]	DEF_COL_CHB[6]	DEF_COL_CHB[5]	DEF_COL_CHB[4]	DEF_COL_CHB[3]	DEF_COL_CHB[2]	DEF_COL_CHB[1]	DEF_COL_CHB[0]
0xC2	0x00	FR_COLOR_SEL_4	rw	DEF_COL_CHC[7]	DEF_COL_CHC[6]	DEF_COL_CHC[5]	DEF_COL_CHC[4]	DEF_COL_CHC[3]	DEF_COL_CHC[2]	DEF_COL_CHC[1]	DEF_COL_CHC[0]
0xC5	0x91	DFC_CLMP_CNTRL	rw	CLAMP_AVG_FCTR[1]	CLAMP_AVG_FCTR[0]	-	-	-	-	-	-
0xC6	0x00	CLMP_POS_CNTRL_1	rw	CP_ANVC_POS_START[7]	CP_ANVC_POS_START[6]	CP_ANVC_POS_START[5]	CP_ANVC_POS_START[4]	CP_ANVC_POS_START[3]	CP_ANVC_POS_START[2]	CP_ANVC_POS_START[1]	CP_ANVC_POS_START[0]
0xC7	0x00	CLMP_POS_CNTRL_2	rw	CP_ANVC_POS_DURATION[7]	CP_ANVC_POS_DURATION[6]	CP_ANVC_POS_DURATION[5]	CP_ANVC_POS_DURATION[4]	CP_ANVC_POS_DURATION[3]	CP_ANVC_POS_DURATION[2]	CP_ANVC_POS_DURATION[1]	CP_ANVC_POS_DURATION[0]
0xC8	0x00	CLMP_POS_CNTRL_3	rw	CP_DFC_POS_START[7]	CP_DFC_POS_START[6]	CP_DFC_POS_START[5]	CP_DFC_POS_START[4]	CP_DFC_POS_START[3]	CP_DFC_POS_START[2]	CP_DFC_POS_START[1]	CP_DFC_POS_START[0]
0xC9	0x2C	CLMP_POS_CNTRL_4	rw	CP_ANVC_POS_START[12]	CP_DFC_POS_START[12]	-	-	-	SWAP_SPLIT_AV	-	DIS_AUTO_PARAM_BUFF
0xCA	0x00	CLMP_POS_CNTRL_5	rw	CP_ANVC_POS_START[11]	CP_ANVC_POS_START[10]	CP_ANVC_POS_START[9]	CP_ANVC_POS_START[8]	CP_DFC_POS_START[11]	CP_DFC_POS_START[10]	CP_DFC_POS_START[9]	CP_DFC_POS_START[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xCB	0x60	HDMI_CP_CNTRL_2	rw	-	-	AUTO_SL_FILTER_FREEZE_EN	-	-	-	HDMI_CP_LOCK_THRESHOLD[1]	HDMI_CP_LOCK_THRESHOLD[0]
0xDA	0x00	PEAK_WHITE_AGC_CNTRL_1	rw	-	-	-	-	-	-	PW_WIN_MAN	PW_SHOW_WIN
0xDB	0x19	PEAK_WHITE_AGC_CNTRL_2	rw	PW_VB[7]	PW_VB[6]	PW_VB[5]	PW_VB[4]	PW_VB[3]	PW_VB[2]	PW_VB[1]	PW_VB[0]
0xDC	0x64	PEAK_WHITE_AGC_CNTRL_3	rw	PW_VL[7]	PW_VL[6]	PW_VL[5]	PW_VL[4]	PW_VL[3]	PW_VL[2]	PW_VL[1]	PW_VL[0]
0xDD	0x12	PEAK_WHITE_AGC_CNTRL_4	rw	PW_HB[11]	PW_HB[10]	PW_HB[9]	PW_HB[8]	PW_HB[7]	PW_HB[6]	PW_HB[5]	PW_HB[4]
0xDE	0xC5	PEAK_WHITE_AGC_CNTRL_5	rw	PW_HB[3]	PW_HB[2]	PW_HB[1]	PW_HB[0]	PW_HL[11]	PW_HL[10]	PW_HL[9]	PW_HL[8]
0xDF	0x78	PEAK_WHITE_AGC_CNTRL_6	rw	PW_HL[7]	PW_HL[6]	PW_HL[5]	PW_HL[4]	PW_HL[3]	PW_HL[2]	PW_HL[1]	PW_HL[0]
0xE0	0x00		r	-	HDMI_CP_AUTOPARM_LOCKED	HDMI_AUTOPARM_STS[1]	HDMI_AUTOPARM_STS[0]	-	-	CP_AGC_GAIN[9]	CP_AGC_GAIN[8]
0xE1	0x00		r	CP_AGC_GAIN[7]	CP_AGC_GAIN[6]	CP_AGC_GAIN[5]	CP_AGC_GAIN[4]	CP_AGC_GAIN[3]	CP_AGC_GAIN[2]	CP_AGC_GAIN[1]	CP_AGC_GAIN[0]
0xE2	0x00	NOISE_CALIB_RB	r	NOISE[7]	NOISE[6]	NOISE[5]	NOISE[4]	NOISE[3]	NOISE[2]	NOISE[1]	NOISE[0]
0xE3	0x00	CP_REG_E3	r	-	-	-	CALIB[10]	CALIB[9]	CALIB[8]	IFSD[8]	ISD[8]
0xE4	0x00		r	ISD[7]	ISD[6]	ISD[5]	ISD[4]	ISD[3]	ISD[2]	ISD[1]	ISD[0]
0xE5	0x00	CP_REG_E5	r	IFSD[7]	IFSD[6]	IFSD[5]	IFSD[4]	IFSD[3]	IFSD[2]	IFSD[1]	IFSD[0]
0xE6	0x00	CP_REG_E6	r	CALIB[7]	CALIB[6]	CALIB[5]	CALIB[4]	CALIB[3]	CALIB[2]	CALIB[1]	CALIB[0]
0xE7	0x00	HSYNC_DEPTH_RB_1	r	-	-	HSD_CHC[9]	HSD_CHC[8]	HSD_CHB[9]	HSD_CHB[8]	HSD_CHA[9]	HSD_CHA[8]
0xE8	0x00	HSYNC_DEPTH_RB_2	r	HSD_CHA[7]	HSD_CHA[6]	HSD_CHA[5]	HSD_CHA[4]	HSD_CHA[3]	HSD_CHA[2]	HSD_CHA[1]	HSD_CHA[0]
0xE9	0x00	HSYNC_DEPTH_RB_3	r	HSD_CHB[7]	HSD_CHB[6]	HSD_CHB[5]	HSD_CHB[4]	HSD_CHB[3]	HSD_CHB[2]	HSD_CHB[1]	HSD_CHB[0]
0xEA	0x00	HSYNC_DEPTH_RB_4	r	HSD_CHC[7]	HSD_CHC[6]	HSD_CHC[5]	HSD_CHC[4]	HSD_CHC[3]	HSD_CHC[2]	HSD_CHC[1]	HSD_CHC[0]
0xEB	0x00	HSYNC_DEPTH_RB_5	r	-	-	-	-	HSD_FB[11]	HSD_FB[10]	HSD_FB[9]	HSD_FB[8]
0xEC	0x00	HSYNC_DEPTH_RB_6	r	HSD_FB[7]	HSD_FB[6]	HSD_FB[5]	HSD_FB[4]	HSD_FB[3]	HSD_FB[2]	HSD_FB[1]	HSD_FB[0]
0xED	0x00	PEAK_WHITE_RB_1	r	-	-	PKV_CHA[9]	PKV_CHA[8]	PKV_CHB[9]	PKV_CHB[8]	PKV_CHC[9]	PKV_CHC[8]
0xEE	0x00	PEAK_WHITE_RB_2	r	PKV_CHA[7]	PKV_CHA[6]	PKV_CHA[5]	PKV_CHA[4]	PKV_CHA[3]	PKV_CHA[2]	PKV_CHA[1]	PKV_CHA[0]
0xEF	0x00	PEAK_WHITE_RB_3	r	PKV_CHB[7]	PKV_CHB[6]	PKV_CHB[5]	PKV_CHB[4]	PKV_CHB[3]	PKV_CHB[2]	PKV_CHB[1]	PKV_CHB[0]
0xF0	0x00	PEAK_WHITE_RB_4	r	PKV_CHC[7]	PKV_CHC[6]	PKV_CHC[5]	PKV_CHC[4]	PKV_CHC[3]	PKV_CHC[2]	PKV_CHC[1]	PKV_CHC[0]
0xF3	0xD4	SYNC_DET_CNTRL_CH1_6	rw	-	-	CH1_FL_FR_THRESHOLD[2]	CH1_FL_FR_THRESHOLD[1]	CH1_FL_FR_THRESHOLD[0]	CH1_F_RUN_THR[2]	CH1_F_RUN_THR[1]	CH1_F_RUN_THR[0]
0xF4	0x00	CSC_COEFF_SEL_RB	r	CSC_COEFF_SEL_RB[3]	CSC_COEFF_SEL_RB[2]	CSC_COEFF_SEL_RB[1]	CSC_COEFF_SEL_RB[0]	-	-	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xF5	0x00		rw	-	-	-	WD_TIMER_DIS	DIG_SYNC_DEGLITCH_REDUCE	DIG_SYNC_DEGLITCH_REDUCE_MAN	BYPASS_STDI1_LOCKING	BYPASS_STDI2_LOCKING
0xFF	0x00	CP_REG_FF	r	MV_PS_DET	MV_AGC_DET	-	CP_FREE_RUN	-	-	-	-

1.3 VDP MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x3C	0x00	VDP_CGMS_TYPE B_DATA_1	r	VDP_CGMS_TYPE B_DATA[7]	VDP_CGMS_TYPE B_DATA[6]	VDP_CGMS_TYPE B_DATA[5]	VDP_CGMS_TYPE B_DATA[4]	VDP_CGMS_TYPE B_DATA[3]	VDP_CGMS_TYPE B_DATA[2]	VDP_CGMS_TYPE B_DATA[1]	VDP_CGMS_TYPE B_DATA[0]
0x3D	0x00	VDP_CGMS_TYPE B_DATA_2	r	VDP_CGMS_TYPE B_DATA[15]	VDP_CGMS_TYPE B_DATA[14]	VDP_CGMS_TYPE B_DATA[13]	VDP_CGMS_TYPE B_DATA[12]	VDP_CGMS_TYPE B_DATA[11]	VDP_CGMS_TYPE B_DATA[10]	VDP_CGMS_TYPE B_DATA[9]	VDP_CGMS_TYPE B_DATA[8]
0x3E	0x00	VDP_CGMS_TYPE B_DATA_3	r	VDP_CGMS_TYPE B_DATA_3[23]	VDP_CGMS_TYPE B_DATA_3[22]	VDP_CGMS_TYPE B_DATA_3[21]	VDP_CGMS_TYPE B_DATA_3[20]	VDP_CGMS_TYPE B_DATA_3[19]	VDP_CGMS_TYPE B_DATA_3[18]	VDP_CGMS_TYPE B_DATA_3[17]	VDP_CGMS_TYPE B_DATA_3[16]
0x3F	0x00	VDP_CGMS_TYPE B_DATA_4	r	VDP_CGMS_TYPE B_DATA_4[31]	VDP_CGMS_TYPE B_DATA_4[30]	VDP_CGMS_TYPE B_DATA_4[29]	VDP_CGMS_TYPE B_DATA_4[28]	VDP_CGMS_TYPE B_DATA_4[27]	VDP_CGMS_TYPE B_DATA_4[26]	VDP_CGMS_TYPE B_DATA_4[25]	VDP_CGMS_TYPE B_DATA_4[24]
0x40	0x00	VDP_STATUS	r	VDP_STATUS_TTX T	VDP_STATUS_VITC	VDP_STATUS_GEM S_TYPE	VDP_STATUS_GS_ VPS_PDC_UTC_CG MSTB	VDP_STATUS_FAS T_I2C	VDP_STATUS_WSS _CGMS	VDP_STATUS_CCA P_EVEN_FIELD	VDP_STATUS_CCA P
0x41	0x00	VDP_CCAP_DATA_ 1	r	VDP_CCAP_DATA[7]	VDP_CCAP_DATA[6]	VDP_CCAP_DATA[5]	VDP_CCAP_DATA[4]	VDP_CCAP_DATA[3]	VDP_CCAP_DATA[2]	VDP_CCAP_DATA[1]	VDP_CCAP_DATA[0]
0x42	0x00	VDP_CCAP_DATA_ 2	r	VDP_CCAP_DATA[15]	VDP_CCAP_DATA[14]	VDP_CCAP_DATA[13]	VDP_CCAP_DATA[12]	VDP_CCAP_DATA[11]	VDP_CCAP_DATA[10]	VDP_CCAP_DATA[9]	VDP_CCAP_DATA[8]
0x43	0x00	VDP_CGMS_WSS_ DATA_1	r	VDP_CGMS_WSS_ DATA[23]	VDP_CGMS_WSS_ DATA[22]	VDP_CGMS_WSS_ DATA[21]	VDP_CGMS_WSS_ DATA[20]	VDP_CGMS_WSS_ DATA[19]	VDP_CGMS_WSS_ DATA[18]	VDP_CGMS_WSS_ DATA[17]	VDP_CGMS_WSS_ DATA[16]
0x44	0x00	VDP_CGMS_WSS_ DATA_2	r	VDP_CGMS_WSS_ DATA[15]	VDP_CGMS_WSS_ DATA[14]	VDP_CGMS_WSS_ DATA[13]	VDP_CGMS_WSS_ DATA[12]	VDP_CGMS_WSS_ DATA[11]	VDP_CGMS_WSS_ DATA[10]	VDP_CGMS_WSS_ DATA[9]	VDP_CGMS_WSS_ DATA[8]
0x45	0x00	VDP_CGMS_WSS_ DATA_3	r	VDP_CGMS_WSS_ DATA[7]	VDP_CGMS_WSS_ DATA[6]	VDP_CGMS_WSS_ DATA[5]	VDP_CGMS_WSS_ DATA[4]	VDP_CGMS_WSS_ DATA[3]	VDP_CGMS_WSS_ DATA[2]	VDP_CGMS_WSS_ DATA[1]	VDP_CGMS_WSS_ DATA[0]
0x47	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_1	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[7]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[6]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[5]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[4]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[3]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[2]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[1]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[0]
0x48	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_2	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[15]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[14]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[13]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[12]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[11]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[10]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[9]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[8]
0x49	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_3	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[23]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[22]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[21]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[20]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[19]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[18]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[17]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[16]
0x4A	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_4	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[31]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[30]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[29]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[28]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[27]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[26]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[25]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[24]
0x4B	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_5	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[39]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[38]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[37]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[36]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[35]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[34]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[33]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[32]
0x4C	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_6	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[47]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[46]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[45]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[44]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[43]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[42]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[41]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[40]
0x4D	0x00	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA_7	r	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[55]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[54]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[53]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[52]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[51]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[50]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[49]	VDP_GS_VPS_PDC _UTC_CGMSTB_D ATA[48]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x4E	0x00	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA_8	r	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[63]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[62]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[61]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[60]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[59]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[58]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[57]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[56]
0x4F	0x00	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA_9	r	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[71]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[70]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[69]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[68]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[67]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[66]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[65]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[64]
0x50	0x00	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA_10	r	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[79]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[78]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[77]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[76]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[75]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[74]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[73]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[72]
0x51	0x00	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA_11	r	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[87]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[86]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[85]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[84]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[83]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[82]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[81]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[80]
0x52	0x00	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA_12	r	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[95]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[94]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[93]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[92]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[91]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[90]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[89]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[88]
0x53	0x00	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA_13	r	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[103]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[102]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[101]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[100]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[99]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[98]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[97]	VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[96]
0x55	0x00	VDP_VITC_DATA_1	r	VDP_VITC_DATA[7]	VDP_VITC_DATA[6]	VDP_VITC_DATA[5]	VDP_VITC_DATA[4]	VDP_VITC_DATA[3]	VDP_VITC_DATA[2]	VDP_VITC_DATA[1]	VDP_VITC_DATA[0]
0x56	0x00	VDP_VITC_DATA_2	r	VDP_VITC_DATA[15]	VDP_VITC_DATA[14]	VDP_VITC_DATA[13]	VDP_VITC_DATA[12]	VDP_VITC_DATA[11]	VDP_VITC_DATA[10]	VDP_VITC_DATA[9]	VDP_VITC_DATA[8]
0x57	0x00	VDP_VITC_DATA_3	r	VDP_VITC_DATA[23]	VDP_VITC_DATA[22]	VDP_VITC_DATA[21]	VDP_VITC_DATA[20]	VDP_VITC_DATA[19]	VDP_VITC_DATA[18]	VDP_VITC_DATA[17]	VDP_VITC_DATA[16]
0x58	0x00	VDP_VITC_DATA_4	r	VDP_VITC_DATA[31]	VDP_VITC_DATA[30]	VDP_VITC_DATA[29]	VDP_VITC_DATA[28]	VDP_VITC_DATA[27]	VDP_VITC_DATA[26]	VDP_VITC_DATA[25]	VDP_VITC_DATA[24]
0x59	0x00	VDP_VITC_DATA_5	r	VDP_VITC_DATA[39]	VDP_VITC_DATA[38]	VDP_VITC_DATA[37]	VDP_VITC_DATA[36]	VDP_VITC_DATA[35]	VDP_VITC_DATA[34]	VDP_VITC_DATA[33]	VDP_VITC_DATA[32]
0x5A	0x00	VDP_VITC_DATA_6	r	VDP_VITC_DATA[47]	VDP_VITC_DATA[46]	VDP_VITC_DATA[45]	VDP_VITC_DATA[44]	VDP_VITC_DATA[43]	VDP_VITC_DATA[42]	VDP_VITC_DATA[41]	VDP_VITC_DATA[40]
0x5B	0x00	VDP_VITC_DATA_7	r	VDP_VITC_DATA[55]	VDP_VITC_DATA[54]	VDP_VITC_DATA[53]	VDP_VITC_DATA[52]	VDP_VITC_DATA[51]	VDP_VITC_DATA[50]	VDP_VITC_DATA[49]	VDP_VITC_DATA[48]
0x5C	0x00	VDP_VITC_DATA_8	r	VDP_VITC_DATA[63]	VDP_VITC_DATA[62]	VDP_VITC_DATA[61]	VDP_VITC_DATA[60]	VDP_VITC_DATA[59]	VDP_VITC_DATA[58]	VDP_VITC_DATA[57]	VDP_VITC_DATA[56]
0x5D	0x00	VDP_VITC_DATA_9	r	VDP_VITC_DATA[71]	VDP_VITC_DATA[70]	VDP_VITC_DATA[69]	VDP_VITC_DATA[68]	VDP_VITC_DATA[67]	VDP_VITC_DATA[66]	VDP_VITC_DATA[65]	VDP_VITC_DATA[64]
0x5E	0x00	VDP_VITC_CALC_CRC	r	VDP_VITC_CALC_CRC[7]	VDP_VITC_CALC_CRC[6]	VDP_VITC_CALC_CRC[5]	VDP_VITC_CALC_CRC[4]	VDP_VITC_CALC_CRC[3]	VDP_VITC_CALC_CRC[2]	VDP_VITC_CALC_CRC[1]	VDP_VITC_CALC_CRC[0]
0x60	0x08	VDP_CONFIG_1	rw	-	-	-	-	EN_FC_WINDOW_AFTER_CRI_DET	VDP_TTXT_TYPE_MAN_EN	VDP_TTXT_TYPE[1]	VDP_TTXT_TYPE[0]
0x61	0x18	VDP_CONFIG_2	rw	VDP_CP_CLMP_AVG	-	NOISE_CLK_DISABLE	AUTO_DETECT_GEM	-	-	VITC_STRIP_SYNC_DISABLE	BIPHASE_DECODE_DISABLE
0x62	0x15	VDP_ADF_CONFIG_1	rw	ADF_EN	ADF_MODE[1]	ADF_MODE[0]	ADF_DID[4]	ADF_DID[3]	ADF_DID[2]	ADF_DID[1]	ADF_DID[0]
0x63	0x2A	VDP_ADF_CONFIG_2	rw	TOGGLE_ADF	-	ADF_SDID[5]	ADF_SDID[4]	ADF_SDID[3]	ADF_SDID[2]	ADF_SDID[1]	ADF_SDID[0]
0x64	0x00	VDP_MAN_LINE_1_21	rw	VDP_MAN_LINE_1_21[7]	VDP_MAN_LINE_1_21[6]	VDP_MAN_LINE_1_21[5]	VDP_MAN_LINE_1_21[4]	VDP_MAN_LINE_1_21[3]	VDP_MAN_LINE_1_21[2]	VDP_MAN_LINE_1_21[1]	VDP_MAN_LINE_1_21[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x65	0x00	VDP_MAN_LINE_22	rw	VDP_MAN_LINE_22[7]	VDP_MAN_LINE_22[6]	VDP_MAN_LINE_22[5]	VDP_MAN_LINE_22[4]	VDP_MAN_LINE_22[3]	VDP_MAN_LINE_22[2]	VDP_MAN_LINE_22[1]	VDP_MAN_LINE_22[0]
0x66	0x00	VDP_MAN_LINE_23	rw	VDP_MAN_LINE_23[7]	VDP_MAN_LINE_23[6]	VDP_MAN_LINE_23[5]	VDP_MAN_LINE_23[4]	VDP_MAN_LINE_23[3]	VDP_MAN_LINE_23[2]	VDP_MAN_LINE_23[1]	VDP_MAN_LINE_23[0]
0x67	0x00	VDP_MAN_LINE_24	rw	VDP_MAN_LINE_24[7]	VDP_MAN_LINE_24[6]	VDP_MAN_LINE_24[5]	VDP_MAN_LINE_24[4]	VDP_MAN_LINE_24[3]	VDP_MAN_LINE_24[2]	VDP_MAN_LINE_24[1]	VDP_MAN_LINE_24[0]
0x68	0x00	VDP_MAN_LINE_25	rw	VDP_MAN_LINE_25[7]	VDP_MAN_LINE_25[6]	VDP_MAN_LINE_25[5]	VDP_MAN_LINE_25[4]	VDP_MAN_LINE_25[3]	VDP_MAN_LINE_25[2]	VDP_MAN_LINE_25[1]	VDP_MAN_LINE_25[0]
0x69	0x00	VDP_MAN_LINE_26	rw	VDP_MAN_LINE_26[7]	VDP_MAN_LINE_26[6]	VDP_MAN_LINE_26[5]	VDP_MAN_LINE_26[4]	VDP_MAN_LINE_26[3]	VDP_MAN_LINE_26[2]	VDP_MAN_LINE_26[1]	VDP_MAN_LINE_26[0]
0x6A	0x00	VDP_MAN_LINE_27	rw	VDP_MAN_LINE_27[7]	VDP_MAN_LINE_27[6]	VDP_MAN_LINE_27[5]	VDP_MAN_LINE_27[4]	VDP_MAN_LINE_27[3]	VDP_MAN_LINE_27[2]	VDP_MAN_LINE_27[1]	VDP_MAN_LINE_27[0]
0x6B	0x00	VDP_MAN_LINE_28	rw	VDP_MAN_LINE_28[7]	VDP_MAN_LINE_28[6]	VDP_MAN_LINE_28[5]	VDP_MAN_LINE_28[4]	VDP_MAN_LINE_28[3]	VDP_MAN_LINE_28[2]	VDP_MAN_LINE_28[1]	VDP_MAN_LINE_28[0]
0x6C	0x00	VDP_MAN_LINE_29	rw	VDP_MAN_LINE_29[7]	VDP_MAN_LINE_29[6]	VDP_MAN_LINE_29[5]	VDP_MAN_LINE_29[4]	VDP_MAN_LINE_29[3]	VDP_MAN_LINE_29[2]	VDP_MAN_LINE_29[1]	VDP_MAN_LINE_29[0]
0x6D	0x00	VDP_MAN_LINE_10_30	rw	VDP_MAN_LINE_10_30[7]	VDP_MAN_LINE_10_30[6]	VDP_MAN_LINE_10_30[5]	VDP_MAN_LINE_10_30[4]	VDP_MAN_LINE_10_30[3]	VDP_MAN_LINE_10_30[2]	VDP_MAN_LINE_10_30[1]	VDP_MAN_LINE_10_30[0]
0x6E	0x00	VDP_MAN_LINE_11_31	rw	VDP_MAN_LINE_11_31[7]	VDP_MAN_LINE_11_31[6]	VDP_MAN_LINE_11_31[5]	VDP_MAN_LINE_11_31[4]	VDP_MAN_LINE_11_31[3]	VDP_MAN_LINE_11_31[2]	VDP_MAN_LINE_11_31[1]	VDP_MAN_LINE_11_31[0]
0x6F	0x00	VDP_MAN_LINE_12_32	rw	VDP_MAN_LINE_12_32[7]	VDP_MAN_LINE_12_32[6]	VDP_MAN_LINE_12_32[5]	VDP_MAN_LINE_12_32[4]	VDP_MAN_LINE_12_32[3]	VDP_MAN_LINE_12_32[2]	VDP_MAN_LINE_12_32[1]	VDP_MAN_LINE_12_32[0]
0x70	0x00	VDP_MAN_LINE_13_33	rw	VDP_MAN_LINE_13_33[7]	VDP_MAN_LINE_13_33[6]	VDP_MAN_LINE_13_33[5]	VDP_MAN_LINE_13_33[4]	VDP_MAN_LINE_13_33[3]	VDP_MAN_LINE_13_33[2]	VDP_MAN_LINE_13_33[1]	VDP_MAN_LINE_13_33[0]
0x71	0x00	VDP_MAN_LINE_14_34	rw	VDP_MAN_LINE_14_34[7]	VDP_MAN_LINE_14_34[6]	VDP_MAN_LINE_14_34[5]	VDP_MAN_LINE_14_34[4]	VDP_MAN_LINE_14_34[3]	VDP_MAN_LINE_14_34[2]	VDP_MAN_LINE_14_34[1]	VDP_MAN_LINE_14_34[0]
0x72	0x00	VDP_MAN_LINE_15_35	rw	VDP_MAN_LINE_15_35[7]	VDP_MAN_LINE_15_35[6]	VDP_MAN_LINE_15_35[5]	VDP_MAN_LINE_15_35[4]	VDP_MAN_LINE_15_35[3]	VDP_MAN_LINE_15_35[2]	VDP_MAN_LINE_15_35[1]	VDP_MAN_LINE_15_35[0]
0x73	0x00	VDP_MAN_LINE_16_36	rw	VDP_MAN_LINE_16_36[7]	VDP_MAN_LINE_16_36[6]	VDP_MAN_LINE_16_36[5]	VDP_MAN_LINE_16_36[4]	VDP_MAN_LINE_16_36[3]	VDP_MAN_LINE_16_36[2]	VDP_MAN_LINE_16_36[1]	VDP_MAN_LINE_16_36[0]
0x74	0x00	VDP_MAN_LINE_17_37	rw	VDP_MAN_LINE_17_37[7]	VDP_MAN_LINE_17_37[6]	VDP_MAN_LINE_17_37[5]	VDP_MAN_LINE_17_37[4]	VDP_MAN_LINE_17_37[3]	VDP_MAN_LINE_17_37[2]	VDP_MAN_LINE_17_37[1]	VDP_MAN_LINE_17_37[0]
0x75	0x00	VDP_MAN_LINE_18_38	rw	VDP_MAN_LINE_18_38[7]	VDP_MAN_LINE_18_38[6]	VDP_MAN_LINE_18_38[5]	VDP_MAN_LINE_18_38[4]	VDP_MAN_LINE_18_38[3]	VDP_MAN_LINE_18_38[2]	VDP_MAN_LINE_18_38[1]	VDP_MAN_LINE_18_38[0]
0x76	0x00	VDP_MAN_LINE_19_39	rw	VDP_MAN_LINE_19_39[7]	VDP_MAN_LINE_19_39[6]	VDP_MAN_LINE_19_39[5]	VDP_MAN_LINE_19_39[4]	VDP_MAN_LINE_19_39[3]	VDP_MAN_LINE_19_39[2]	VDP_MAN_LINE_19_39[1]	VDP_MAN_LINE_19_39[0]
0x77	0x00	VDP_MAN_LINE_20_40	rw	VDP_MAN_LINE_20_40[7]	VDP_MAN_LINE_20_40[6]	VDP_MAN_LINE_20_40[5]	VDP_MAN_LINE_20_40[4]	VDP_MAN_LINE_20_40[3]	VDP_MAN_LINE_20_40[2]	VDP_MAN_LINE_20_40[1]	VDP_MAN_LINE_20_40[0]
0x78	0x00	VDP_STATUS_CLEAR	sc	STATUS_CLEAR_TTXT	STATUS_CLEAR_VITC	-	STATUS_CLEAR_GEMS_VPS	VDP_STATUS_CLEAR_FAST_I2C	STATUS_CLEAR_WSS_CGMS	-	STATUS_CLEAR_CCAP
0x98	0x88	VDP_FILTER_ADAPTIVE_SLICER_CONFIG	rw	LOW_DATA_STD_FILTER_EN	-	ADAP1_SL_CONFIG_EN	TTX_SEL	ADAP2_SL_CONFIG_EN	-	-	-
0x99	0xDD	VDP_ADAP2_STD_EN	rw	ADAP2_TTXT_STD_EN	ADAP2_VITC_STD_EN	-	ADAP2_GEMS_STD_EN	ADAP2_VPS_STD_EN	ADAP2_WSS_CGMS_STD_EN	-	ADAP2_CCAP_STD_EN
0x9C	0x20	VDP_STATUS_CONFIG	rw	-	-	GS_VPS_PDC_UTC_CB_CHANGE	WSS_CGMS_CB_CHANGE	RAW_STATUS_ENABLE	GS_VPS_PDC_UTC_CGMSTB[2]	GS_VPS_PDC_UTC_CGMSTB[1]	GS_VPS_PDC_UTC_CGMSTB[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9D	0x02	VDP_MISC_CONFIG	rw	-	-	-	-	-	-	SLICE_CORRECTOR_EN	-
0x9E	0x00	VDP_ADAP2_FAST_LEARN_EN	rw	-	-	-	-	ADAP2_VPS_CTB_FAST_LEARN_EN	-	-	-
0xA5	0x90	VDP_NEW_TTX_CONFIG1	rw	-	VDP_USE_PREDEF_FREQ	VDP_CRI_TOLERANCE	VDP_FRM_CODE_TOLERANCE	VDP_CRI_8BIT	-	-	-
0xA6	0x00	VDP_NEW_TTX_CONFIG2	rw	-	-	-	VDP_INVERT_EVEN_FIELD	-	-	-	-
0xA8	0x08	VDP_PARITY_MAX	rw	-	VDP_MANUAL_TTXC	-	-	-	-	-	-
0xAC	0xC8	VDP_CRI_MAG_THRESH	rw	VDP_CRI_MAG_TRESH[7]	VDP_CRI_MAG_TRESH[6]	VDP_CRI_MAG_TRESH[5]	VDP_CRI_MAG_TRESH[4]	VDP_CRI_MAG_TRESH[3]	VDP_CRI_MAG_TRESH[2]	VDP_CRI_MAG_TRESH[1]	VDP_CRI_MAG_TRESH[0]
0xC0	0x00	FAST_I2C_REG_CONF1	rw	VDP_FAST_REG_CONF_CUS2	VDP_FAST_REG_CONF_CUST	VDP_FAST_REG_CONF_CCAP	VDP_FAST_REG_CONF_GEM1X_2X	VDP_FAST_REG_CONF_CGMS_WSS	VDP_FAST_REG_CONF_VITC	VDP_FAST_REG_CONF_VPS_CGMSTB	VDP_FAST_REG_CONF_TTXT
0xC2	0x00	FAST_I2C_VBI_STD	r	-	-	-	-	VDP_FAST_VBI_STD[3]	VDP_FAST_VBI_STD[2]	VDP_FAST_VBI_STD[1]	VDP_FAST_VBI_STD[0]
0xC3	0x00	FAST_I2C_PACKET_SIZE	r	VDP_FAST_PACKET_SIZE[7]	VDP_FAST_PACKET_SIZE[6]	VDP_FAST_PACKET_SIZE[5]	VDP_FAST_PACKET_SIZE[4]	VDP_FAST_PACKET_SIZE[3]	VDP_FAST_PACKET_SIZE[2]	VDP_FAST_PACKET_SIZE[1]	VDP_FAST_PACKET_SIZE[0]
0xC4	0x00	FAST_I2C_REG_00	r	VDP_FAST_REG00[7]	VDP_FAST_REG00[6]	VDP_FAST_REG00[5]	VDP_FAST_REG00[4]	VDP_FAST_REG00[3]	VDP_FAST_REG00[2]	VDP_FAST_REG00[1]	VDP_FAST_REG00[0]
0xC5	0x00	FAST_I2C_REG_01	r	VDP_FAST_REG01[7]	VDP_FAST_REG01[6]	VDP_FAST_REG01[5]	VDP_FAST_REG01[4]	VDP_FAST_REG01[3]	VDP_FAST_REG01[2]	VDP_FAST_REG01[1]	VDP_FAST_REG01[0]
0xC6	0x00	FAST_I2C_REG_02	r	VDP_FAST_REG02[7]	VDP_FAST_REG02[6]	VDP_FAST_REG02[5]	VDP_FAST_REG02[4]	VDP_FAST_REG02[3]	VDP_FAST_REG02[2]	VDP_FAST_REG02[1]	VDP_FAST_REG02[0]
0xC7	0x00	FAST_I2C_REG_03	r	VDP_FAST_REG03[7]	VDP_FAST_REG03[6]	VDP_FAST_REG03[5]	VDP_FAST_REG03[4]	VDP_FAST_REG03[3]	VDP_FAST_REG03[2]	VDP_FAST_REG03[1]	VDP_FAST_REG03[0]
0xC8	0x00	FAST_I2C_REG_04	r	VDP_FAST_REG04[7]	VDP_FAST_REG04[6]	VDP_FAST_REG04[5]	VDP_FAST_REG04[4]	VDP_FAST_REG04[3]	VDP_FAST_REG04[2]	VDP_FAST_REG04[1]	VDP_FAST_REG04[0]
0xC9	0x00	FAST_I2C_REG_05	r	VDP_FAST_REG05[7]	VDP_FAST_REG05[6]	VDP_FAST_REG05[5]	VDP_FAST_REG05[4]	VDP_FAST_REG05[3]	VDP_FAST_REG05[2]	VDP_FAST_REG05[1]	VDP_FAST_REG05[0]
0xCA	0x00	FAST_I2C_REG_06	r	VDP_FAST_REG06[7]	VDP_FAST_REG06[6]	VDP_FAST_REG06[5]	VDP_FAST_REG06[4]	VDP_FAST_REG06[3]	VDP_FAST_REG06[2]	VDP_FAST_REG06[1]	VDP_FAST_REG06[0]
0xCB	0x00	FAST_I2C_REG_07	r	VDP_FAST_REG07[7]	VDP_FAST_REG07[6]	VDP_FAST_REG07[5]	VDP_FAST_REG07[4]	VDP_FAST_REG07[3]	VDP_FAST_REG07[2]	VDP_FAST_REG07[1]	VDP_FAST_REG07[0]
0xCC	0x00	FAST_I2C_REG_08	r	VDP_FAST_REG08[7]	VDP_FAST_REG08[6]	VDP_FAST_REG08[5]	VDP_FAST_REG08[4]	VDP_FAST_REG08[3]	VDP_FAST_REG08[2]	VDP_FAST_REG08[1]	VDP_FAST_REG08[0]
0xCD	0x00	FAST_I2C_REG_09	r	VDP_FAST_REG09[7]	VDP_FAST_REG09[6]	VDP_FAST_REG09[5]	VDP_FAST_REG09[4]	VDP_FAST_REG09[3]	VDP_FAST_REG09[2]	VDP_FAST_REG09[1]	VDP_FAST_REG09[0]
0xCE	0x00	FAST_I2C_REG_10	r	VDP_FAST_REG10[7]	VDP_FAST_REG10[6]	VDP_FAST_REG10[5]	VDP_FAST_REG10[4]	VDP_FAST_REG10[3]	VDP_FAST_REG10[2]	VDP_FAST_REG10[1]	VDP_FAST_REG10[0]
0xCF	0x00	FAST_I2C_REG_11	r	VDP_FAST_REG11[7]	VDP_FAST_REG11[6]	VDP_FAST_REG11[5]	VDP_FAST_REG11[4]	VDP_FAST_REG11[3]	VDP_FAST_REG11[2]	VDP_FAST_REG11[1]	VDP_FAST_REG11[0]
0xD0	0x00	FAST_I2C_REG_12	r	VDP_FAST_REG12[7]	VDP_FAST_REG12[6]	VDP_FAST_REG12[5]	VDP_FAST_REG12[4]	VDP_FAST_REG12[3]	VDP_FAST_REG12[2]	VDP_FAST_REG12[1]	VDP_FAST_REG12[0]
0xD1	0x00	FAST_I2C_REG_13	r	VDP_FAST_REG13[7]	VDP_FAST_REG13[6]	VDP_FAST_REG13[5]	VDP_FAST_REG13[4]	VDP_FAST_REG13[3]	VDP_FAST_REG13[2]	VDP_FAST_REG13[1]	VDP_FAST_REG13[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xD2	0x00	FAST_I2C_REG_14	r	VDP_FAST_REG14[7]	VDP_FAST_REG14[6]	VDP_FAST_REG14[5]	VDP_FAST_REG14[4]	VDP_FAST_REG14[3]	VDP_FAST_REG14[2]	VDP_FAST_REG14[1]	VDP_FAST_REG14[0]
0xD3	0x00	FAST_I2C_REG_15	r	VDP_FAST_REG15[7]	VDP_FAST_REG15[6]	VDP_FAST_REG15[5]	VDP_FAST_REG15[4]	VDP_FAST_REG15[3]	VDP_FAST_REG15[2]	VDP_FAST_REG15[1]	VDP_FAST_REG15[0]
0xD4	0x00	FAST_I2C_REG_16	r	VDP_FAST_REG16[7]	VDP_FAST_REG16[6]	VDP_FAST_REG16[5]	VDP_FAST_REG16[4]	VDP_FAST_REG16[3]	VDP_FAST_REG16[2]	VDP_FAST_REG16[1]	VDP_FAST_REG16[0]
0xD5	0x00	FAST_I2C_REG_17	r	VDP_FAST_REG17[7]	VDP_FAST_REG17[6]	VDP_FAST_REG17[5]	VDP_FAST_REG17[4]	VDP_FAST_REG17[3]	VDP_FAST_REG17[2]	VDP_FAST_REG17[1]	VDP_FAST_REG17[0]
0xD6	0x00	FAST_I2C_REG_18	r	VDP_FAST_REG18[7]	VDP_FAST_REG18[6]	VDP_FAST_REG18[5]	VDP_FAST_REG18[4]	VDP_FAST_REG18[3]	VDP_FAST_REG18[2]	VDP_FAST_REG18[1]	VDP_FAST_REG18[0]
0xD7	0x00	FAST_I2C_REG_19	r	VDP_FAST_REG19[7]	VDP_FAST_REG19[6]	VDP_FAST_REG19[5]	VDP_FAST_REG19[4]	VDP_FAST_REG19[3]	VDP_FAST_REG19[2]	VDP_FAST_REG19[1]	VDP_FAST_REG19[0]
0xD8	0x00	FAST_I2C_REG_20	r	VDP_FAST_REG20[7]	VDP_FAST_REG20[6]	VDP_FAST_REG20[5]	VDP_FAST_REG20[4]	VDP_FAST_REG20[3]	VDP_FAST_REG20[2]	VDP_FAST_REG20[1]	VDP_FAST_REG20[0]
0xD9	0x00	FAST_I2C_REG_21	r	VDP_FAST_REG21[7]	VDP_FAST_REG21[6]	VDP_FAST_REG21[5]	VDP_FAST_REG21[4]	VDP_FAST_REG21[3]	VDP_FAST_REG21[2]	VDP_FAST_REG21[1]	VDP_FAST_REG21[0]
0xDA	0x00	FAST_I2C_REG_22	r	VDP_FAST_REG22[7]	VDP_FAST_REG22[6]	VDP_FAST_REG22[5]	VDP_FAST_REG22[4]	VDP_FAST_REG22[3]	VDP_FAST_REG22[2]	VDP_FAST_REG22[1]	VDP_FAST_REG22[0]
0xDB	0x00	FAST_I2C_REG_23	r	VDP_FAST_REG23[7]	VDP_FAST_REG23[6]	VDP_FAST_REG23[5]	VDP_FAST_REG23[4]	VDP_FAST_REG23[3]	VDP_FAST_REG23[2]	VDP_FAST_REG23[1]	VDP_FAST_REG23[0]
0xDC	0x00	FAST_I2C_REG_24	r	VDP_FAST_REG24[7]	VDP_FAST_REG24[6]	VDP_FAST_REG24[5]	VDP_FAST_REG24[4]	VDP_FAST_REG24[3]	VDP_FAST_REG24[2]	VDP_FAST_REG24[1]	VDP_FAST_REG24[0]
0xDD	0x00	FAST_I2C_REG_25	r	VDP_FAST_REG25[7]	VDP_FAST_REG25[6]	VDP_FAST_REG25[5]	VDP_FAST_REG25[4]	VDP_FAST_REG25[3]	VDP_FAST_REG25[2]	VDP_FAST_REG25[1]	VDP_FAST_REG25[0]
0xDE	0x00	FAST_I2C_REG_26	r	VDP_FAST_REG26[7]	VDP_FAST_REG26[6]	VDP_FAST_REG26[5]	VDP_FAST_REG26[4]	VDP_FAST_REG26[3]	VDP_FAST_REG26[2]	VDP_FAST_REG26[1]	VDP_FAST_REG26[0]
0xDF	0x00	FAST_I2C_REG_27	r	VDP_FAST_REG27[7]	VDP_FAST_REG27[6]	VDP_FAST_REG27[5]	VDP_FAST_REG27[4]	VDP_FAST_REG27[3]	VDP_FAST_REG27[2]	VDP_FAST_REG27[1]	VDP_FAST_REG27[0]
0xE0	0x00	FAST_I2C_REG_28	r	VDP_FAST_REG28[7]	VDP_FAST_REG28[6]	VDP_FAST_REG28[5]	VDP_FAST_REG28[4]	VDP_FAST_REG28[3]	VDP_FAST_REG28[2]	VDP_FAST_REG28[1]	VDP_FAST_REG28[0]
0xE1	0x00	FAST_I2C_REG_29	r	VDP_FAST_REG29[7]	VDP_FAST_REG29[6]	VDP_FAST_REG29[5]	VDP_FAST_REG29[4]	VDP_FAST_REG29[3]	VDP_FAST_REG29[2]	VDP_FAST_REG29[1]	VDP_FAST_REG29[0]
0xE2	0x00	FAST_I2C_REG_30	r	VDP_FAST_REG30[7]	VDP_FAST_REG30[6]	VDP_FAST_REG30[5]	VDP_FAST_REG30[4]	VDP_FAST_REG30[3]	VDP_FAST_REG30[2]	VDP_FAST_REG30[1]	VDP_FAST_REG30[0]
0xE3	0x00	FAST_I2C_REG_31	r	VDP_FAST_REG31[7]	VDP_FAST_REG31[6]	VDP_FAST_REG31[5]	VDP_FAST_REG31[4]	VDP_FAST_REG31[3]	VDP_FAST_REG31[2]	VDP_FAST_REG31[1]	VDP_FAST_REG31[0]
0xE4	0x00	FAST_I2C_REG_32	r	VDP_FAST_REG32[7]	VDP_FAST_REG32[6]	VDP_FAST_REG32[5]	VDP_FAST_REG32[4]	VDP_FAST_REG32[3]	VDP_FAST_REG32[2]	VDP_FAST_REG32[1]	VDP_FAST_REG32[0]
0xE5	0x00	FAST_I2C_REG_33	r	VDP_FAST_REG33[7]	VDP_FAST_REG33[6]	VDP_FAST_REG33[5]	VDP_FAST_REG33[4]	VDP_FAST_REG33[3]	VDP_FAST_REG33[2]	VDP_FAST_REG33[1]	VDP_FAST_REG33[0]
0xE6	0x00	FAST_I2C_REG_34	r	VDP_FAST_REG34[7]	VDP_FAST_REG34[6]	VDP_FAST_REG34[5]	VDP_FAST_REG34[4]	VDP_FAST_REG34[3]	VDP_FAST_REG34[2]	VDP_FAST_REG34[1]	VDP_FAST_REG34[0]
0xE7	0x00	FAST_I2C_REG_35	r	VDP_FAST_REG35[7]	VDP_FAST_REG35[6]	VDP_FAST_REG35[5]	VDP_FAST_REG35[4]	VDP_FAST_REG35[3]	VDP_FAST_REG35[2]	VDP_FAST_REG35[1]	VDP_FAST_REG35[0]
0xE8	0x00	FAST_I2C_REG_36	r	VDP_FAST_REG36[7]	VDP_FAST_REG36[6]	VDP_FAST_REG36[5]	VDP_FAST_REG36[4]	VDP_FAST_REG36[3]	VDP_FAST_REG36[2]	VDP_FAST_REG36[1]	VDP_FAST_REG36[0]
0xE9	0x00	FAST_I2C_REG_37	r	VDP_FAST_REG37[7]	VDP_FAST_REG37[6]	VDP_FAST_REG37[5]	VDP_FAST_REG37[4]	VDP_FAST_REG37[3]	VDP_FAST_REG37[2]	VDP_FAST_REG37[1]	VDP_FAST_REG37[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xEA	0x00	FAST_I2C_REG_38	r	VDP_FAST_REG38[7]	VDP_FAST_REG38[6]	VDP_FAST_REG38[5]	VDP_FAST_REG38[4]	VDP_FAST_REG38[3]	VDP_FAST_REG38[2]	VDP_FAST_REG38[1]	VDP_FAST_REG38[0]
0xEB	0x00	FAST_I2C_REG_39	r	VDP_FAST_REG39[7]	VDP_FAST_REG39[6]	VDP_FAST_REG39[5]	VDP_FAST_REG39[4]	VDP_FAST_REG39[3]	VDP_FAST_REG39[2]	VDP_FAST_REG39[1]	VDP_FAST_REG39[0]
0xEC	0x00	FAST_I2C_REG_40	r	VDP_FAST_REG40[7]	VDP_FAST_REG40[6]	VDP_FAST_REG40[5]	VDP_FAST_REG40[4]	VDP_FAST_REG40[3]	VDP_FAST_REG40[2]	VDP_FAST_REG40[1]	VDP_FAST_REG40[0]
0xED	0x00	FAST_I2C_REG_41	r	VDP_FAST_REG41[7]	VDP_FAST_REG41[6]	VDP_FAST_REG41[5]	VDP_FAST_REG41[4]	VDP_FAST_REG41[3]	VDP_FAST_REG41[2]	VDP_FAST_REG41[1]	VDP_FAST_REG41[0]
0xEE	0x00	FAST_I2C_REG_42	r	VDP_FAST_REG42[7]	VDP_FAST_REG42[6]	VDP_FAST_REG42[5]	VDP_FAST_REG42[4]	VDP_FAST_REG42[3]	VDP_FAST_REG42[2]	VDP_FAST_REG42[1]	VDP_FAST_REG42[0]
0xEF	0x00	FAST_I2C_REG_43	r	VDP_FAST_REG43[7]	VDP_FAST_REG43[6]	VDP_FAST_REG43[5]	VDP_FAST_REG43[4]	VDP_FAST_REG43[3]	VDP_FAST_REG43[2]	VDP_FAST_REG43[1]	VDP_FAST_REG43[0]
0xF0	0x00	FAST_I2C_REG_44	r	VDP_FAST_REG44[7]	VDP_FAST_REG44[6]	VDP_FAST_REG44[5]	VDP_FAST_REG44[4]	VDP_FAST_REG44[3]	VDP_FAST_REG44[2]	VDP_FAST_REG44[1]	VDP_FAST_REG44[0]

1.4 AFE MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x0F	ADC POWERDOWN CONTROL	rw	PDN_ADC_CLK3	PDN_ADC_CLK2	PDN_ADC_CLK1	PDN_ADC_CLK0	PDN_ADC3	PDN_ADC2	PDN_ADC1	PDN_ADC0
0x02	0x00	INPUT MUX CONTROL_1	rw	ADC_SWITCH_MAN	EMB_SYNC_SEL_MAN_EN	-	-	-	AIN_SEL[2]	AIN_SEL[1]	AIN_SEL[0]
0x03	0x00	INPUT MUX CONTROL_2	rw	ADC0_SW_MAN[3]	ADC0_SW_MAN[2]	ADC0_SW_MAN[1]	ADC0_SW_MAN[0]	ADC1_SW_MAN[3]	ADC1_SW_MAN[2]	ADC1_SW_MAN[1]	ADC1_SW_MAN[0]
0x04	0x00	INPUT MUX CONTROL_3	rw	ADC2_SW_MAN[3]	ADC2_SW_MAN[2]	ADC2_SW_MAN[1]	ADC2_SW_MAN[0]	ADC3_SW_MAN[3]	ADC3_SW_MAN[2]	ADC3_SW_MAN[1]	ADC3_SW_MAN[0]
0x05	0x00	ANTI-ALIAS FILTER ENABLE	rw	-	-	-	-	AA_FILTER_EN3	AA_FILTER_EN2	AA_FILTER_EN1	AA_FILTER_EN0
0x06	0x00	ANTI-ALIAS FILTER CALIBRATION	rw	-	-	AA_FILT_HIGH_BW[1]	-	-	-	-	-
0x07	0x00	ANTI-ALIAS FILTER BANDWIDTH	rw	AA_FILT_HIGH_BW[0]	AA_FILT_PROG_BW[1]	AA_FILT_PROG_BW[0]	-	-	-	-	-
0x14	0x00	FAST BLANK	rw	-	-	-	-	FB_SELECT[3]	FB_SELECT[2]	FB_SELECT[1]	FB_SELECT[0]
0x15	0x0A	SYNC STRIPPER	rw	EMB_SYNC_1_SEL_MAN[1]	EMB_SYNC_1_SEL_MAN[0]	EMB_SYNC_2_SEL_MAN[1]	EMB_SYNC_2_SEL_MAN[0]	SYNC1_FILTER_SEL[1]	SYNC1_FILTER_SEL[0]	SYNC2_FILTER_SEL[1]	SYNC2_FILTER_SEL[0]
0x16	0x98	SYNC SLICER LEVEL	rw	-	-	-	SLICE_LEVEL[4]	SLICE_LEVEL[3]	SLICE_LEVEL[2]	SLICE_LEVEL[1]	SLICE_LEVEL[0]
0x17	0x00	TRILEVEL INTERRUPT ENABLE 1	rw	TRI1_INT_MASKB[1]	TRI1_INT_MASKB[0]	TRI2_INT_MASKB[1]	TRI2_INT_MASKB[0]	TRI3_INT_MASKB[1]	TRI3_INT_MASKB[0]	TRI4_INT_MASKB[1]	TRI4_INT_MASKB[0]
0x18	0x00	TRILEVEL INTERRUPT ENABLE 2	rw	TRI5_INT_MASKB[1]	TRI5_INT_MASKB[0]	TRI6_INT_MASKB[1]	TRI6_INT_MASKB[0]	TRI7_INT_MASKB[1]	TRI7_INT_MASKB[0]	TRI8_INT_MASKB[1]	TRI8_INT_MASKB[0]
0x19	0x00	TRILEVEL INTERRUPT CLEAR 1	sc	TRI1_INT_CLEAR[1]	TRI1_INT_CLEAR[0]	TRI2_INT_CLEAR[1]	TRI2_INT_CLEAR[0]	TRI3_INT_CLEAR[1]	TRI3_INT_CLEAR[0]	TRI4_INT_CLEAR[1]	TRI4_INT_CLEAR[0]
0x1A	0x00	TRILEVEL INTERRUPT CLEAR 2	sc	TRI5_INT_CLEAR[1]	TRI5_INT_CLEAR[0]	TRI6_INT_CLEAR[1]	TRI6_INT_CLEAR[0]	TRI7_INT_CLEAR[1]	TRI7_INT_CLEAR[0]	TRI8_INT_CLEAR[1]	TRI8_INT_CLEAR[0]
0x1B	0x00	TRILEVEL INTERRUPT STATUS 1	r	TRI1_INT_STATUS[1]	TRI1_INT_STATUS[0]	TRI2_INT_STATUS[1]	TRI2_INT_STATUS[0]	TRI3_INT_STATUS[1]	TRI3_INT_STATUS[0]	TRI4_INT_STATUS[1]	TRI4_INT_STATUS[0]
0x1C	0x00	TRILEVEL INTERRUPT STATUS 2	r	TRI5_INT_STATUS[1]	TRI5_INT_STATUS[0]	TRI6_INT_STATUS[1]	TRI6_INT_STATUS[0]	TRI7_INT_STATUS[1]	TRI7_INT_STATUS[0]	TRI8_INT_STATUS[1]	TRI8_INT_STATUS[0]
0x1D	0x6D	TRI1 SLICE CONTROL	rw	-	TRI1_SLICER_PWRDN	TRI1_BILEVEL_SLICE_EN	TRI1_UPPER_SLICE_LEVEL[2]	TRI1_UPPER_SLICE_LEVEL[1]	TRI1_UPPER_SLICE_LEVEL[0]	TRI1_LOWER_SLICE_LEVEL[1]	TRI1_LOWER_SLICE_LEVEL[0]
0x1E	0x6D	TRI2 SLICE CONTROL	rw	-	TRI2_SLICER_PWRDN	TRI2_BILEVEL_SLICE_EN	TRI2_UPPER_SLICE_LEVEL[2]	TRI2_UPPER_SLICE_LEVEL[1]	TRI2_UPPER_SLICE_LEVEL[0]	TRI2_LOWER_SLICE_LEVEL[1]	TRI2_LOWER_SLICE_LEVEL[0]
0x1F	0x6D	TRI3 SLICE CONTROL	rw	-	TRI3_SLICER_PWRDN	TRI3_BILEVEL_SLICE_EN	TRI3_UPPER_SLICE_LEVEL[2]	TRI3_UPPER_SLICE_LEVEL[1]	TRI3_UPPER_SLICE_LEVEL[0]	TRI3_LOWER_SLICE_LEVEL[1]	TRI3_LOWER_SLICE_LEVEL[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x20	0x6D	TRI4 SLICE CONTROL	rw	-	TRI4_SLICER_PWRDN	TRI4_BILEVEL_SLICE_EN	TRI4_UPPER_SLICE_LEVEL[2]	TRI4_UPPER_SLICE_LEVEL[1]	TRI4_UPPER_SLICE_LEVEL[0]	TRI4_LOWER_SLICE_LEVEL[1]	TRI4_LOWER_SLICE_LEVEL[0]
0x21	0x6D	TRI5 SLICE CONTROL	rw	-	TRI5_SLICER_PWRDN	TRI5_BILEVEL_SLICE_EN	TRI5_UPPER_SLICE_LEVEL[2]	TRI5_UPPER_SLICE_LEVEL[1]	TRI5_UPPER_SLICE_LEVEL[0]	TRI5_LOWER_SLICE_LEVEL[1]	TRI5_LOWER_SLICE_LEVEL[0]
0x22	0x6D	TRI6 SLICE CONTROL	rw	-	TRI6_SLICER_PWRDN	TRI6_BILEVEL_SLICE_EN	TRI6_UPPER_SLICE_LEVEL[2]	TRI6_UPPER_SLICE_LEVEL[1]	TRI6_UPPER_SLICE_LEVEL[0]	TRI6_LOWER_SLICE_LEVEL[1]	TRI6_LOWER_SLICE_LEVEL[0]
0x23	0x6D	TRI7 SLICE CONTROL	rw	-	TRI7_SLICER_PWRDN	TRI7_BILEVEL_SLICE_EN	TRI7_UPPER_SLICE_LEVEL[2]	TRI7_UPPER_SLICE_LEVEL[1]	TRI7_UPPER_SLICE_LEVEL[0]	TRI7_LOWER_SLICE_LEVEL[1]	TRI7_LOWER_SLICE_LEVEL[0]
0x24	0x6D	TRI8 SLICE CONTROL	rw	-	TRI8_SLICER_PWRDN	TRI8_BILEVEL_SLICE_EN	TRI8_UPPER_SLICE_LEVEL[2]	TRI8_UPPER_SLICE_LEVEL[1]	TRI8_UPPER_SLICE_LEVEL[0]	TRI8_LOWER_SLICE_LEVEL[1]	TRI8_LOWER_SLICE_LEVEL[0]
0x27	0x00	TRI-INPUTS LEVEL READBACK_1	r	TRI1_READBACK[1]	TRI1_READBACK[0]	TRI2_READBACK[1]	TRI2_READBACK[0]	TRI3_READBACK[1]	TRI3_READBACK[0]	TRI4_READBACK[1]	TRI4_READBACK[0]
0x28	0x00	TRI-INPUTS LEVEL READBACK_2	r	TRI5_READBACK[1]	TRI5_READBACK[0]	TRI6_READBACK[1]	TRI6_READBACK[0]	TRI7_READBACK[1]	TRI7_READBACK[0]	TRI8_READBACK[1]	TRI8_READBACK[0]

1.5 SDP MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x02	AUTODETECT_ENABLES	rw	-	SDP_AD_SECAM_EN	SDP_AD_N443_EN	SDP_AD_PAL60_EN	SDP_AD_PALCN_EN	SDP_AD_PALM_EN	SDP_AD_NTSC_EN	SDP_AD_PAL_EN
0x01	0x36	PEDESTAL_SELECTION	rw	-	SDP_SECAM_PED_EN	SDP_N443_PED_EN	SDP_PAL60_PED_EN	SDP_PALCN_PED_EN	SDP_PALM_PED_EN	SDP_NTSC_PED_EN	SDP_PAL_PED_EN
0x03	0xC4	LUMA_GAIN_1	rw	SDP_Y_AGC_EN	SDP_PW_EN	SDP_MAN_GAIN_VCR	SDP_Y_GAIN_MAN[12]	SDP_Y_GAIN_MAN[11]	SDP_Y_GAIN_MAN[10]	SDP_Y_GAIN_MAN[9]	SDP_Y_GAIN_MAN[8]
0x04	0x0B	LUMA_GAIN_2	rw	SDP_Y_GAIN_MAN[7]	SDP_Y_GAIN_MAN[6]	SDP_Y_GAIN_MAN[5]	SDP_Y_GAIN_MAN[4]	SDP_Y_GAIN_MAN[3]	SDP_Y_GAIN_MAN[2]	SDP_Y_GAIN_MAN[1]	SDP_Y_GAIN_MAN[0]
0x05	0xC3	CHROMA_GAIN_1	rw	SDP_C_AGC_EN	SDP_PC_EN	-	SDP_C_GAIN_ACT_MAN[12]	SDP_C_GAIN_ACT_MAN[11]	SDP_C_GAIN_ACT_MAN[10]	SDP_C_GAIN_ACT_MAN[9]	SDP_C_GAIN_ACT_MAN[8]
0x06	0xC0	CHROMA_GAIN_2	rw	SDP_C_GAIN_ACT_MAN[7]	SDP_C_GAIN_ACT_MAN[6]	SDP_C_GAIN_ACT_MAN[5]	SDP_C_GAIN_ACT_MAN[4]	SDP_C_GAIN_ACT_MAN[3]	SDP_C_GAIN_ACT_MAN[2]	SDP_C_GAIN_ACT_MAN[1]	SDP_C_GAIN_ACT_MAN[0]
0x07	0x8B	COLOUR_KILL_ON_LEVEL	rw	SDP_CKILL_EN	SDP_CK_LOW_THR[6]	SDP_CK_LOW_THR[5]	SDP_CK_LOW_THR[4]	SDP_CK_LOW_THR[3]	SDP_CK_LOW_THR[2]	SDP_CK_LOW_THR[1]	SDP_CK_LOW_THR[0]
0x08	0x1A	COLOUR_KILL_OFF_LEVEL	rw	SDP_CK_HIGH_THR[7]	SDP_CK_HIGH_THR[6]	SDP_CK_HIGH_THR[5]	SDP_CK_HIGH_THR[4]	SDP_CK_HIGH_THR[3]	SDP_CK_HIGH_THR[2]	SDP_CK_HIGH_THR[1]	SDP_CK_HIGH_THR[0]
0x0A	0xE5	LUMA_GAIN_SPEED	rw	-	-	-	SDP_DGAIN_SPEED[4]	SDP_DGAIN_SPEED[3]	SDP_DGAIN_SPEED[2]	SDP_DGAIN_SPEED[1]	SDP_DGAIN_SPEED[0]
0x0B	0xE5	CHROMA_GAIN_SPEED	rw	-	-	-	SDP_C_DGAIN_SPEED[4]	SDP_C_DGAIN_SPEED[3]	SDP_C_DGAIN_SPEED[2]	SDP_C_DGAIN_SPEED[1]	SDP_C_DGAIN_SPEED[0]
0x0C	0xE5	DIGITAL_CLAMP_SPEED	rw	-	-	-	SDP_DCLP_SPEED[4]	SDP_DCLP_SPEED[3]	SDP_DCLP_SPEED[2]	SDP_DCLP_SPEED[1]	SDP_DCLP_SPEED[0]
0x0D	0xE4	ANALOGUE_CLAMP_SPEED	rw	-	-	-	SDP_ACLP_SPEED[4]	SDP_ACLP_SPEED[3]	SDP_ACLP_SPEED[2]	SDP_ACLP_SPEED[1]	SDP_ACLP_SPEED[0]
0x0E	0x31	VIDEO_ENHANCEMENTS	rw	-	-	SDP_SCM_CTI_EN	SDP_Y_2D_PK_EN	SDP_V_PK_EN	SDP_H_PK_EN	SDP_LTI_EN	SDP_CTI_EN
0x0F	0x00	GAIN_RECOVERY_SPEED_1	rw	SDP_PC_REC_RATE[11]	SDP_PC_REC_RATE[10]	SDP_PC_REC_RATE[9]	SDP_PC_REC_RATE[8]	SDP_PW_REC_RATE[11]	SDP_PW_REC_RATE[10]	SDP_PW_REC_RATE[9]	SDP_PW_REC_RATE[8]
0x10	0x01	GAIN_RECOVERY_SPEED_2	rw	SDP_PW_REC_RATE[7]	SDP_PW_REC_RATE[6]	SDP_PW_REC_RATE[5]	SDP_PW_REC_RATE[4]	SDP_PW_REC_RATE[3]	SDP_PW_REC_RATE[2]	SDP_PW_REC_RATE[1]	SDP_PW_REC_RATE[0]
0x11	0x10	GAIN_RECOVERY_SPEED_3	rw	SDP_PC_REC_RATE[7]	SDP_PC_REC_RATE[6]	SDP_PC_REC_RATE[5]	SDP_PC_REC_RATE[4]	SDP_PC_REC_RATE[3]	SDP_PC_REC_RATE[2]	SDP_PC_REC_RATE[1]	SDP_PC_REC_RATE[0]
0x12	0x01	3D_ENABLES	rw	-	-	-	-	SDP_SHIP_EN	SDP_FR_TBC_EN	-	SDP_3D_COMB_EN
0x13	0x80	CONTRAST	rw	SDP_CONTRAST[9]	SDP_CONTRAST[8]	SDP_CONTRAST[7]	SDP_CONTRAST[6]	SDP_CONTRAST[5]	SDP_CONTRAST[4]	SDP_CONTRAST[3]	SDP_CONTRAST[2]
0x14	0x00	BRIGHTNESS	rw	SDP_BRIGHTNESS[9]	SDP_BRIGHTNESS[8]	SDP_BRIGHTNESS[7]	SDP_BRIGHTNESS[6]	SDP_BRIGHTNESS[5]	SDP_BRIGHTNESS[4]	SDP_BRIGHTNESS[3]	SDP_BRIGHTNESS[2]
0x15	0x80	SATURATION	rw	SDP_SATURATION[9]	SDP_SATURATION[8]	SDP_SATURATION[7]	SDP_SATURATION[6]	SDP_SATURATION[5]	SDP_SATURATION[4]	SDP_SATURATION[3]	SDP_SATURATION[2]
0x16	0x00	HUE_TINT_1	rw	SDP_HUE[9]	SDP_HUE[8]	SDP_HUE[7]	SDP_HUE[6]	SDP_HUE[5]	SDP_HUE[4]	SDP_HUE[3]	SDP_HUE[2]
0x17	0x00	HUE_TINT_2	rw	SDP_HUE[1]	SDP_HUE[0]	SDP_SATURATION[1]	SDP_SATURATION[0]	SDP_BRIGHTNESS[1]	SDP_BRIGHTNESS[0]	SDP_CONTRAST[1]	SDP_CONTRAST[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x18	0xFF	Y_SHAPING_FILTER_1	rw	SDP_BLANK_C_VBI	SDP_FORCE_CKILL_HQI	SDP_Y_SHAPE_SEL_VBI[5]	SDP_Y_SHAPE_SEL_VBI[4]	SDP_Y_SHAPE_SEL_VBI[3]	SDP_Y_SHAPE_SEL_VBI[2]	SDP_Y_SHAPE_SEL_VBI[1]	SDP_Y_SHAPE_SEL_VBI[0]
0x19	0xCD	Y_SHAPING_FILTER_2	rw	SDP_Y_SHAPE_AUTO_EN	SDP_FORCE_COMP_HQI	SDP_Y_SHAPE_SEL_HQI[5]	SDP_Y_SHAPE_SEL_HQI[4]	SDP_Y_SHAPE_SEL_HQI[3]	SDP_Y_SHAPE_SEL_HQI[2]	SDP_Y_SHAPE_SEL_HQI[1]	SDP_Y_SHAPE_SEL_HQI[0]
0x1A	0x95	Y_SHAPING_FILTER_3	rw	SDP_HQI_REQ_STD	-	SDP_Y_SHAPE_SEL_LQI[5]	SDP_Y_SHAPE_SEL_LQI[4]	SDP_Y_SHAPE_SEL_LQI[3]	SDP_Y_SHAPE_SEL_LQI[2]	SDP_Y_SHAPE_SEL_LQI[1]	SDP_Y_SHAPE_SEL_LQI[0]
0x1B	0x1E	Y_SHAPING_FILTER_4	rw	-	-	SDP_Y_SHAPE_SEL_SCM[5]	SDP_Y_SHAPE_SEL_SCM[4]	SDP_Y_SHAPE_SEL_SCM[3]	SDP_Y_SHAPE_SEL_SCM[2]	SDP_Y_SHAPE_SEL_SCM[1]	SDP_Y_SHAPE_SEL_SCM[0]
0x1C	0xC4	C_SHAPING_FILTER_1	rw	SDP_C_SHAPE_AUTO_EN	SDP_CSH_WBW_AUTO	-	SDP_C_SHAPE_SEL_HQI[4]	SDP_C_SHAPE_SEL_HQI[3]	SDP_C_SHAPE_SEL_HQI[2]	SDP_C_SHAPE_SEL_HQI[1]	SDP_C_SHAPE_SEL_HQI[0]
0x1D	0x02	C_SHAPING_FILTER_2	rw	-	-	-	SDP_C_SHAPE_SEL_LQI[4]	SDP_C_SHAPE_SEL_LQI[3]	SDP_C_SHAPE_SEL_LQI[2]	SDP_C_SHAPE_SEL_LQI[1]	SDP_C_SHAPE_SEL_LQI[0]
0x1E	0x04	C_SHAPING_FILTER_3	rw	-	-	-	SDP_C_SHAPE_SEL_SCM[4]	SDP_C_SHAPE_SEL_SCM[3]	SDP_C_SHAPE_SEL_SCM[2]	SDP_C_SHAPE_SEL_SCM[1]	SDP_C_SHAPE_SEL_SCM[0]
0x1F	0x12	COMB_SPLIT_FILTER	rw	-	-	-	SDP_SPLIT_FILTER_SEL[4]	SDP_SPLIT_FILTER_SEL[3]	SDP_SPLIT_FILTER_SEL[2]	SDP_SPLIT_FILTER_SEL[1]	SDP_SPLIT_FILTER_SEL[0]
0x20	0x00	C_IF_FILTER	rw	-	-	-	SDP_IF_FILT_SEL[4]	SDP_IF_FILT_SEL[3]	SDP_IF_FILT_SEL[2]	SDP_IF_FILT_SEL[1]	SDP_IF_FILT_SEL[0]
0x21	0xFF	DELAY_LINE	rw	SDP_U_DEL_LINE_EN	SDP_V_DEL_LINE_EN	-	-	-	-	-	-
0x22	0x20	HORIZONTAL_PEAKING	rw	SDP_H_PK_INV	SDP_H_PK_GAIN[3]	SDP_H_PK_GAIN[2]	SDP_H_PK_GAIN[1]	SDP_H_PK_GAIN[0]	SDP_H_PK_CORE[2]	SDP_H_PK_CORE[1]	SDP_H_PK_CORE[0]
0x23	0x10	VERTICAL_PEAKING	rw	SDP_V_PK_INV	SDP_V_PK_GAIN[3]	SDP_V_PK_GAIN[2]	SDP_V_PK_GAIN[1]	SDP_V_PK_GAIN[0]	SDP_V_PK_CORE[2]	SDP_V_PK_CORE[1]	SDP_V_PK_CORE[0]
0x24	0x4C	H_V_PEAKING	rw	-	SDP_V_PK_FLIP[2]	SDP_V_PK_FLIP[1]	SDP_V_PK_FLIP[0]	SDP_V_PK_CLIP[1]	SDP_V_PK_CLIP[0]	SDP_H_PK_BAND[1]	SDP_H_PK_BAND[0]
0x25	0x00	LTI	rw	SDP_LTI_FILT_SEL	SDP_LTI_LEVEL[6]	SDP_LTI_LEVEL[5]	SDP_LTI_LEVEL[4]	SDP_LTI_LEVEL[3]	SDP_LTI_LEVEL[2]	SDP_LTI_LEVEL[1]	SDP_LTI_LEVEL[0]
0x26	0x8F	CTI	rw	SDP_CTI_FILT_SEL	-	SDP_CTI_LEVEL[5]	SDP_CTI_LEVEL[4]	SDP_CTI_LEVEL[3]	SDP_CTI_LEVEL[2]	SDP_CTI_LEVEL[1]	SDP_CTI_LEVEL[0]
0x27	0xAA	LTI_CTI	rw	SDP_CTI_FLIP[1]	SDP_CTI_FLIP[0]	-	-	SDP_LTI_FLIP[1]	SDP_LTI_FLIP[0]	-	-
0x28	0x02	SECAM CTI	rw	-	-	-	-	-	SDP_SCM_CTI_GAIN[1]	SDP_SCM_CTI_GAIN[0]	-
0x2A	0x00	RGB_FB_DELAY_ADJUST	rw	SDP_MAN_FB	SDP_RGB_DELAY_ADJ[2]	SDP_RGB_DELAY_ADJ[1]	SDP_RGB_DELAY_ADJ[0]	SDP_MAN_FB_EN	SDP_FB_DELAY_ADJ[2]	SDP_FB_DELAY_ADJ[1]	SDP_FB_DELAY_ADJ[0]
0x34	0xA0	LINE_TBC	rw	SDP_TBC_EN	-	-	-	-	-	-	-
0x4C	0x00	STATUS_LETTERBOX_TOP	r	SDP_LBOX_BLK_TOP[7]	SDP_LBOX_BLK_TOP[6]	SDP_LBOX_BLK_TOP[5]	SDP_LBOX_BLK_TOP[4]	SDP_LBOX_BLK_TOP[3]	SDP_LBOX_BLK_TOP[2]	SDP_LBOX_BLK_TOP[1]	SDP_LBOX_BLK_TOP[0]
0x4D	0x00	STATUS_LETTERBOX_BOTTOM	r	SDP_LBOX_BLK_BOT[7]	SDP_LBOX_BLK_BOT[6]	SDP_LBOX_BLK_BOT[5]	SDP_LBOX_BLK_BOT[4]	SDP_LBOX_BLK_BOT[3]	SDP_LBOX_BLK_BOT[2]	SDP_LBOX_BLK_BOT[1]	SDP_LBOX_BLK_BOT[0]
0x4E	0x00	STATUS_LETTERBOX_SUBTITLES_BOTTOM	r	SDP_LBOX_BLK_SUB_BOT[7]	SDP_LBOX_BLK_SUB_BOT[6]	SDP_LBOX_BLK_SUB_BOT[5]	SDP_LBOX_BLK_SUB_BOT[4]	SDP_LBOX_BLK_SUB_BOT[3]	SDP_LBOX_BLK_SUB_BOT[2]	SDP_LBOX_BLK_SUB_BOT[1]	SDP_LBOX_BLK_SUB_BOT[0]
0x4F	0x00	STATUS_NOISE_LEVEL_LSBS	r	SDP_SYNCTIP_NOISE[7]	SDP_SYNCTIP_NOISE[6]	SDP_SYNCTIP_NOISE[5]	SDP_SYNCTIP_NOISE[4]	SDP_SYNCTIP_NOISE[3]	SDP_SYNCTIP_NOISE[2]	SDP_SYNCTIP_NOISE[1]	SDP_SYNCTIP_NOISE[0]
0x50	0x00	STATUS_MACROVISION_DETECTION_1	r	-	-	-	-	SDP_MV_AGC_DETECTED	SDP_MV_PS_DETECTED	SDP_MVCS_TYPE3	SDP_MVCS_DETECT

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x51	0x00	STATUS_MACROVISION_DETECTION_2	r	SDP_BP_TOTAL_PULSE_BEG[3]	SDP_BP_TOTAL_PULSE_BEG[2]	SDP_BP_TOTAL_PULSE_BEG[1]	SDP_BP_TOTAL_PULSE_BEG[0]	SDP_BP_TOTAL_PULSES_END[3]	SDP_BP_TOTAL_PULSES_END[2]	SDP_BP_TOTAL_PULSES_END[1]	SDP_BP_TOTAL_PULSES_END[0]
0x52	0x00	STATUS_ACTIVE_STANDARD	r	-	-	-	-	SDP_STD[3]	SDP_STD[2]	SDP_STD[1]	SDP_STD[0]
0x53	0x00	STATUS_NOISE_LEVEL_MSBS	r	SDP_SYNCTIP_NOISE[11]	SDP_SYNCTIP_NOISE[10]	SDP_SYNCTIP_NOISE[9]	SDP_SYNCTIP_NOISE[8]	-	-	-	-
0x54	0x00	STATUS_LUMA_GAIN_1	r	SDP_NOISY_IP	SDP_VERY_NOISY_IP	SDP_C_CHAN_ACTIVE	SDP_Y_GAIN_MAN_RB[12]	SDP_Y_GAIN_MAN_RB[11]	SDP_Y_GAIN_MAN_RB[10]	SDP_Y_GAIN_MAN_RB[9]	SDP_Y_GAIN_MAN_RB[8]
0x55	0x00	STATUS_LUMA_GAIN_2	r	SDP_Y_GAIN_MAN_RB[7]	SDP_Y_GAIN_MAN_RB[6]	SDP_Y_GAIN_MAN_RB[5]	SDP_Y_GAIN_MAN_RB[4]	SDP_Y_GAIN_MAN_RB[3]	SDP_Y_GAIN_MAN_RB[2]	SDP_Y_GAIN_MAN_RB[1]	SDP_Y_GAIN_MAN_RB[0]
0x56	0x00	SDP_STATUS_INPUT_TYPE_1	r	SDP_HSWITCH_PRESENT	SDP_BLK_NSTD	SDP_FLD_NSTD	SDP_FRM_NSTD	SDP_LC_NSTD	SDP_ALLOW_MED_PLL	SDP_ALLOW_SLOW_PLL	SDP_FREE_RUN
0x57	0x00	SDP_STATUS_INPUT_TYPE_2	r	SDP_CKILL_ACT	SDP_VS_STD_MODE	-	SDP_ALLOW_3D_COMB	SDP_INTERLACED	SDP_TRICK_MODE	-	-
0x58	0x00	STATUS_PR_SD_DETECTION	r	-	SDP_PR_DETECTED_IN_SD	-	-	-	-	-	-
0x59	0x00	STATUS_BURST_LOCKING	r	SDP_BURST_LOCKED_RB	-	-	-	SDP_AD_50_60_HZ	SDP_PAL_SW_LOCKED	SDP_FSC_FREQ_OK	SDP_SCM_LOCKED
0x5A	0x00	STATUS_INPUT_TYPE_3	r	-	-	-	-	-	-	-	SDP_VIDEO_DETECTED
0x7B	0x69	SYNC_DETECTION_PARAMETERS_4	rw	-	-	-	-	-	SDP_EXTEND_VS_MAX_FREQ	SDP_EXTEND_VS_MIN_FREQ	-
0x89	0x03	LUMA_AGC_TARGET_1	rw	SDP_LIMIT_Y_GAIN	SDP_LIMIT_C_GAIN	SDP_LIMIT_UV_GAIN	SDP_LIMIT_G_GAIN	-	-	-	-
0x98	0xBF	HQI_SHAPING_FILTER_DISABLE	rw	SDP_NSY_DIS_SFS_STD	SDP_HSW2_DIS_SFS_STD	SDP_HSW1_DIS_SFS_STD	SDP_LC_DIS_SFS_STD	SDP_BLK_DIS_SFS_STD	SDP_FLD_SFS_STD	SDP_FRM_DIS_SFS_STD	SDP_VNSY_DIS_SFS_STD
0x99	0x10	DETECTION_FILTERING_1	rw	-	SDP_SHAPE_STD_FILT_SEL[2]	SDP_SHAPE_STD_FILT_SEL[1]	SDP_SHAPE_STD_FILT_SEL[0]	-	-	-	-
0x9A	0x01	DETECTION_FILTERING_2	rw	-	-	-	-	-	SDP_ALLOW_3D_FILT_SEL[2]	SDP_ALLOW_3D_FILT_SEL[1]	SDP_ALLOW_3D_FILT_SEL[0]
0xA1	0x50	NOISY_THRESHOLD	rw	SDP_NOISY_THR[7]	SDP_NOISY_THR[6]	SDP_NOISY_THR[5]	SDP_NOISY_THR[4]	SDP_NOISY_THR[3]	SDP_NOISY_THR[2]	SDP_NOISY_THR[1]	SDP_NOISY_THR[0]
0xA2	0xA0	VERY_NOISY_THRESHOLD	rw	SDP_VERY_NOISY_THR[7]	SDP_VERY_NOISY_THR[6]	SDP_VERY_NOISY_THR[5]	SDP_VERY_NOISY_THR[4]	SDP_VERY_NOISY_THR[3]	SDP_VERY_NOISY_THR[2]	SDP_VERY_NOISY_THR[1]	SDP_VERY_NOISY_THR[0]
0xA3	0xBE	3D_COMB_DISABLE_CLEAN	rw	SDP_CKILL_DIS_3D	-	-	-	-	-	-	-
0xA4	0xBF	3D_COMB_DISABLE_NOISY	rw	SDP_CKILL_DIS_2D	SDP_NOISY_HSW2_DIS_3D	SDP_NOISY_HSW1_DIS_3D	SDP_NOISY_LC_DIS_3D	SDP_NOISY_BLK_DIS_3D	SDP_NOISY_FLD_DIS_3D	SDP_NOISY_FRM_DIS_3D	SDP_NOISY_DIS_3D
0xA5	0xBF	3D_COMB_DISABLE_VERY_NOISY	rw	SDP_P60_N443_DIS_3D	SDP_VNOISY_HSW2_DIS_3D	SDP_VNOISY_HSW1_DIS_3D	SDP_VNOISY_LC_DIS_3D	SDP_VNOISY_BLK_DIS_3D	SDP_VNOISY_FLD_DIS_3D	SDP_VNOISY_FRM_DIS_3D	SDP_VNOISY_DIS_3D
0xA8	0x40	3D_COMB_NOISE_SENSITIVITY	rw	-	SDP_3D_COMB_NOISE_SNS[6]	SDP_3D_COMB_NOISE_SNS[5]	SDP_3D_COMB_NOISE_SNS[4]	SDP_3D_COMB_NOISE_SNS[3]	SDP_3D_COMB_NOISE_SNS[2]	SDP_3D_COMB_NOISE_SNS[1]	SDP_3D_COMB_NOISE_SNS[0]
0xA9	0x88	3D_COMB_CHROMA_SENSITIVITY	rw	SDP_3D_COMB_CHROMA_CORE[3]	SDP_3D_COMB_CHROMA_CORE[2]	SDP_3D_COMB_CHROMA_CORE[1]	SDP_3D_COMB_CHROMA_CORE[0]	SDP_3D_COMB_CHROMA_SNS[3]	SDP_3D_COMB_CHROMA_SNS[2]	SDP_3D_COMB_CHROMA_SNS[1]	SDP_3D_COMB_CHROMA_SNS[0]
0xAA	0x88	3D_COMB_LUMA_SENSITIVITY	rw	SDP_3D_COMB_LUMA_CORE[3]	SDP_3D_COMB_LUMA_CORE[2]	SDP_3D_COMB_LUMA_CORE[1]	SDP_3D_COMB_LUMA_CORE[0]	SDP_3D_COMB_LUMA_SNS[3]	SDP_3D_COMB_LUMA_SNS[2]	SDP_3D_COMB_LUMA_SNS[1]	SDP_3D_COMB_LUMA_SNS[0]
0xD9	0x44	OP_SPL_1	rw	-	SDP_SHIP_INT_EN	-	-	-	-	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xDB	0x88	LETTERBOX_DETECT_1	rw	SDP_LBOX_END_DEL[3]	SDP_LBOX_END_DEL[2]	SDP_LBOX_END_DEL[1]	SDP_LBOX_END_DEL[0]	SDP_LBOX_BEG_DEL[3]	SDP_LBOX_BEG_DEL[2]	SDP_LBOX_BEG_DEL[1]	SDP_LBOX_BEG_DEL[0]
0xDC	0x02	LETTERBOX_DETECT_2	rw	SDP_LBOX_BLK_LVL[2]	SDP_LBOX_BLK_LVL[1]	SDP_LBOX_BLK_LVL[0]	SDP_LBOX_THR[4]	SDP_LBOX_THR[3]	SDP_LBOX_THR[2]	SDP_LBOX_THR[1]	SDP_LBOX_THR[0]
0xDD	0xBC	SDP_FREE_RUN	rw	-	-	-	-	SDP_FREE_RUN_AUTO	SDP_FREE_RUN_MAN_COL_EN	SDP_FREE_RUN_CBAR_EN	SDP_FORCE_FREE_RUN
0xDE	0x23	SDP_FREE_RUN_Y	rw	SDP_FREE_RUN_Y[7]	SDP_FREE_RUN_Y[6]	SDP_FREE_RUN_Y[5]	SDP_FREE_RUN_Y[4]	SDP_FREE_RUN_Y[3]	SDP_FREE_RUN_Y[2]	SDP_FREE_RUN_Y[1]	SDP_FREE_RUN_Y[0]
0xDF	0x7D	SDP_FREE_RUN_C	rw	SDP_FREE_RUN_V[3]	SDP_FREE_RUN_V[2]	SDP_FREE_RUN_V[1]	SDP_FREE_RUN_V[0]	SDP_FREE_RUN_U[3]	SDP_FREE_RUN_U[2]	SDP_FREE_RUN_U[1]	SDP_FREE_RUN_U[0]

1.6 CEC MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00		rw	CEC_TX_FRAME_HEADER[7]	CEC_TX_FRAME_HEADER[6]	CEC_TX_FRAME_HEADER[5]	CEC_TX_FRAME_HEADER[4]	CEC_TX_FRAME_HEADER[3]	CEC_TX_FRAME_HEADER[2]	CEC_TX_FRAME_HEADER[1]	CEC_TX_FRAME_HEADER[0]
0x01	0x00		rw	CEC_TX_FRAME_DATA0[7]	CEC_TX_FRAME_DATA0[6]	CEC_TX_FRAME_DATA0[5]	CEC_TX_FRAME_DATA0[4]	CEC_TX_FRAME_DATA0[3]	CEC_TX_FRAME_DATA0[2]	CEC_TX_FRAME_DATA0[1]	CEC_TX_FRAME_DATA0[0]
0x02	0x00		rw	CEC_TX_FRAME_DATA1[7]	CEC_TX_FRAME_DATA1[6]	CEC_TX_FRAME_DATA1[5]	CEC_TX_FRAME_DATA1[4]	CEC_TX_FRAME_DATA1[3]	CEC_TX_FRAME_DATA1[2]	CEC_TX_FRAME_DATA1[1]	CEC_TX_FRAME_DATA1[0]
0x03	0x00		rw	CEC_TX_FRAME_DATA2[7]	CEC_TX_FRAME_DATA2[6]	CEC_TX_FRAME_DATA2[5]	CEC_TX_FRAME_DATA2[4]	CEC_TX_FRAME_DATA2[3]	CEC_TX_FRAME_DATA2[2]	CEC_TX_FRAME_DATA2[1]	CEC_TX_FRAME_DATA2[0]
0x04	0x00		rw	CEC_TX_FRAME_DATA3[7]	CEC_TX_FRAME_DATA3[6]	CEC_TX_FRAME_DATA3[5]	CEC_TX_FRAME_DATA3[4]	CEC_TX_FRAME_DATA3[3]	CEC_TX_FRAME_DATA3[2]	CEC_TX_FRAME_DATA3[1]	CEC_TX_FRAME_DATA3[0]
0x05	0x00		rw	CEC_TX_FRAME_DATA4[7]	CEC_TX_FRAME_DATA4[6]	CEC_TX_FRAME_DATA4[5]	CEC_TX_FRAME_DATA4[4]	CEC_TX_FRAME_DATA4[3]	CEC_TX_FRAME_DATA4[2]	CEC_TX_FRAME_DATA4[1]	CEC_TX_FRAME_DATA4[0]
0x06	0x00		rw	CEC_TX_FRAME_DATA5[7]	CEC_TX_FRAME_DATA5[6]	CEC_TX_FRAME_DATA5[5]	CEC_TX_FRAME_DATA5[4]	CEC_TX_FRAME_DATA5[3]	CEC_TX_FRAME_DATA5[2]	CEC_TX_FRAME_DATA5[1]	CEC_TX_FRAME_DATA5[0]
0x07	0x00		rw	CEC_TX_FRAME_DATA6[7]	CEC_TX_FRAME_DATA6[6]	CEC_TX_FRAME_DATA6[5]	CEC_TX_FRAME_DATA6[4]	CEC_TX_FRAME_DATA6[3]	CEC_TX_FRAME_DATA6[2]	CEC_TX_FRAME_DATA6[1]	CEC_TX_FRAME_DATA6[0]
0x08	0x00		rw	CEC_TX_FRAME_DATA7[7]	CEC_TX_FRAME_DATA7[6]	CEC_TX_FRAME_DATA7[5]	CEC_TX_FRAME_DATA7[4]	CEC_TX_FRAME_DATA7[3]	CEC_TX_FRAME_DATA7[2]	CEC_TX_FRAME_DATA7[1]	CEC_TX_FRAME_DATA7[0]
0x09	0x00		rw	CEC_TX_FRAME_DATA8[7]	CEC_TX_FRAME_DATA8[6]	CEC_TX_FRAME_DATA8[5]	CEC_TX_FRAME_DATA8[4]	CEC_TX_FRAME_DATA8[3]	CEC_TX_FRAME_DATA8[2]	CEC_TX_FRAME_DATA8[1]	CEC_TX_FRAME_DATA8[0]
0x0A	0x00		rw	CEC_TX_FRAME_DATA9[7]	CEC_TX_FRAME_DATA9[6]	CEC_TX_FRAME_DATA9[5]	CEC_TX_FRAME_DATA9[4]	CEC_TX_FRAME_DATA9[3]	CEC_TX_FRAME_DATA9[2]	CEC_TX_FRAME_DATA9[1]	CEC_TX_FRAME_DATA9[0]
0x0B	0x00		rw	CEC_TX_FRAME_DATA10[7]	CEC_TX_FRAME_DATA10[6]	CEC_TX_FRAME_DATA10[5]	CEC_TX_FRAME_DATA10[4]	CEC_TX_FRAME_DATA10[3]	CEC_TX_FRAME_DATA10[2]	CEC_TX_FRAME_DATA10[1]	CEC_TX_FRAME_DATA10[0]
0x0C	0x00		rw	CEC_TX_FRAME_DATA11[7]	CEC_TX_FRAME_DATA11[6]	CEC_TX_FRAME_DATA11[5]	CEC_TX_FRAME_DATA11[4]	CEC_TX_FRAME_DATA11[3]	CEC_TX_FRAME_DATA11[2]	CEC_TX_FRAME_DATA11[1]	CEC_TX_FRAME_DATA11[0]
0x0D	0x00		rw	CEC_TX_FRAME_DATA12[7]	CEC_TX_FRAME_DATA12[6]	CEC_TX_FRAME_DATA12[5]	CEC_TX_FRAME_DATA12[4]	CEC_TX_FRAME_DATA12[3]	CEC_TX_FRAME_DATA12[2]	CEC_TX_FRAME_DATA12[1]	CEC_TX_FRAME_DATA12[0]
0x0E	0x00		rw	CEC_TX_FRAME_DATA13[7]	CEC_TX_FRAME_DATA13[6]	CEC_TX_FRAME_DATA13[5]	CEC_TX_FRAME_DATA13[4]	CEC_TX_FRAME_DATA13[3]	CEC_TX_FRAME_DATA13[2]	CEC_TX_FRAME_DATA13[1]	CEC_TX_FRAME_DATA13[0]
0x0F	0x00		rw	CEC_TX_FRAME_DATA14[7]	CEC_TX_FRAME_DATA14[6]	CEC_TX_FRAME_DATA14[5]	CEC_TX_FRAME_DATA14[4]	CEC_TX_FRAME_DATA14[3]	CEC_TX_FRAME_DATA14[2]	CEC_TX_FRAME_DATA14[1]	CEC_TX_FRAME_DATA14[0]
0x10	0x00		rw	-	-	-	CEC_TX_FRAME_LENGTH[4]	CEC_TX_FRAME_LENGTH[3]	CEC_TX_FRAME_LENGTH[2]	CEC_TX_FRAME_LENGTH[1]	CEC_TX_FRAME_LENGTH[0]
0x11	0x00		rw	-	-	-	-	-	-	-	CEC_TX_ENABLE
0x12	0x13		rw	-	CEC_TX_RETRY[2]	CEC_TX_RETRY[1]	CEC_TX_RETRY[0]	CEC_RETRY_SFT[3]	CEC_RETRY_SFT[2]	CEC_RETRY_SFT[1]	CEC_RETRY_SFT[0]
0x13	0x57		rw	CEC_TX_SFT[3]	CEC_TX_SFT[2]	CEC_TX_SFT[1]	CEC_TX_SFT[0]	CEC_TX_SFT[3]	CEC_TX_SFT[2]	CEC_TX_SFT[1]	CEC_TX_SFT[0]
0x14	0x00		r	CEC_TX_LOWDRIVE_COUNTER[3]	CEC_TX_LOWDRIVE_COUNTER[2]	CEC_TX_LOWDRIVE_COUNTER[1]	CEC_TX_LOWDRIVE_COUNTER[0]	CEC_TX_NACK_COUNTER[3]	CEC_TX_NACK_COUNTER[2]	CEC_TX_NACK_COUNTER[1]	CEC_TX_NACK_COUNTER[0]
0x15	0x00		r	CEC_BUF0_RX_FRAME_HEADER[7]	CEC_BUF0_RX_FRAME_HEADER[6]	CEC_BUF0_RX_FRAME_HEADER[5]	CEC_BUF0_RX_FRAME_HEADER[4]	CEC_BUF0_RX_FRAME_HEADER[3]	CEC_BUF0_RX_FRAME_HEADER[2]	CEC_BUF0_RX_FRAME_HEADER[1]	CEC_BUF0_RX_FRAME_HEADER[0]
0x16	0x00		r	CEC_BUF0_RX_FRAME_DATA0[7]	CEC_BUF0_RX_FRAME_DATA0[6]	CEC_BUF0_RX_FRAME_DATA0[5]	CEC_BUF0_RX_FRAME_DATA0[4]	CEC_BUF0_RX_FRAME_DATA0[3]	CEC_BUF0_RX_FRAME_DATA0[2]	CEC_BUF0_RX_FRAME_DATA0[1]	CEC_BUF0_RX_FRAME_DATA0[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x17	0x00		r	CEC_BUF0_RX_FRAME_DATA1[7]	CEC_BUF0_RX_FRAME_DATA1[6]	CEC_BUF0_RX_FRAME_DATA1[5]	CEC_BUF0_RX_FRAME_DATA1[4]	CEC_BUF0_RX_FRAME_DATA1[3]	CEC_BUF0_RX_FRAME_DATA1[2]	CEC_BUF0_RX_FRAME_DATA1[1]	CEC_BUF0_RX_FRAME_DATA1[0]
0x18	0x00		r	CEC_BUF0_RX_FRAME_DATA2[7]	CEC_BUF0_RX_FRAME_DATA2[6]	CEC_BUF0_RX_FRAME_DATA2[5]	CEC_BUF0_RX_FRAME_DATA2[4]	CEC_BUF0_RX_FRAME_DATA2[3]	CEC_BUF0_RX_FRAME_DATA2[2]	CEC_BUF0_RX_FRAME_DATA2[1]	CEC_BUF0_RX_FRAME_DATA2[0]
0x19	0x00		r	CEC_BUF0_RX_FRAME_DATA3[7]	CEC_BUF0_RX_FRAME_DATA3[6]	CEC_BUF0_RX_FRAME_DATA3[5]	CEC_BUF0_RX_FRAME_DATA3[4]	CEC_BUF0_RX_FRAME_DATA3[3]	CEC_BUF0_RX_FRAME_DATA3[2]	CEC_BUF0_RX_FRAME_DATA3[1]	CEC_BUF0_RX_FRAME_DATA3[0]
0x1A	0x00		r	CEC_BUF0_RX_FRAME_DATA4[7]	CEC_BUF0_RX_FRAME_DATA4[6]	CEC_BUF0_RX_FRAME_DATA4[5]	CEC_BUF0_RX_FRAME_DATA4[4]	CEC_BUF0_RX_FRAME_DATA4[3]	CEC_BUF0_RX_FRAME_DATA4[2]	CEC_BUF0_RX_FRAME_DATA4[1]	CEC_BUF0_RX_FRAME_DATA4[0]
0x1B	0x00		r	CEC_BUF0_RX_FRAME_DATA5[7]	CEC_BUF0_RX_FRAME_DATA5[6]	CEC_BUF0_RX_FRAME_DATA5[5]	CEC_BUF0_RX_FRAME_DATA5[4]	CEC_BUF0_RX_FRAME_DATA5[3]	CEC_BUF0_RX_FRAME_DATA5[2]	CEC_BUF0_RX_FRAME_DATA5[1]	CEC_BUF0_RX_FRAME_DATA5[0]
0x1C	0x00		r	CEC_BUF0_RX_FRAME_DATA6[7]	CEC_BUF0_RX_FRAME_DATA6[6]	CEC_BUF0_RX_FRAME_DATA6[5]	CEC_BUF0_RX_FRAME_DATA6[4]	CEC_BUF0_RX_FRAME_DATA6[3]	CEC_BUF0_RX_FRAME_DATA6[2]	CEC_BUF0_RX_FRAME_DATA6[1]	CEC_BUF0_RX_FRAME_DATA6[0]
0x1D	0x00		r	CEC_BUF0_RX_FRAME_DATA7[7]	CEC_BUF0_RX_FRAME_DATA7[6]	CEC_BUF0_RX_FRAME_DATA7[5]	CEC_BUF0_RX_FRAME_DATA7[4]	CEC_BUF0_RX_FRAME_DATA7[3]	CEC_BUF0_RX_FRAME_DATA7[2]	CEC_BUF0_RX_FRAME_DATA7[1]	CEC_BUF0_RX_FRAME_DATA7[0]
0x1E	0x00		r	CEC_BUF0_RX_FRAME_DATA8[7]	CEC_BUF0_RX_FRAME_DATA8[6]	CEC_BUF0_RX_FRAME_DATA8[5]	CEC_BUF0_RX_FRAME_DATA8[4]	CEC_BUF0_RX_FRAME_DATA8[3]	CEC_BUF0_RX_FRAME_DATA8[2]	CEC_BUF0_RX_FRAME_DATA8[1]	CEC_BUF0_RX_FRAME_DATA8[0]
0x1F	0x00		r	CEC_BUF0_RX_FRAME_DATA9[7]	CEC_BUF0_RX_FRAME_DATA9[6]	CEC_BUF0_RX_FRAME_DATA9[5]	CEC_BUF0_RX_FRAME_DATA9[4]	CEC_BUF0_RX_FRAME_DATA9[3]	CEC_BUF0_RX_FRAME_DATA9[2]	CEC_BUF0_RX_FRAME_DATA9[1]	CEC_BUF0_RX_FRAME_DATA9[0]
0x20	0x00		r	CEC_BUF0_RX_FRAME_DATA10[7]	CEC_BUF0_RX_FRAME_DATA10[6]	CEC_BUF0_RX_FRAME_DATA10[5]	CEC_BUF0_RX_FRAME_DATA10[4]	CEC_BUF0_RX_FRAME_DATA10[3]	CEC_BUF0_RX_FRAME_DATA10[2]	CEC_BUF0_RX_FRAME_DATA10[1]	CEC_BUF0_RX_FRAME_DATA10[0]
0x21	0x00		r	CEC_BUF0_RX_FRAME_DATA11[7]	CEC_BUF0_RX_FRAME_DATA11[6]	CEC_BUF0_RX_FRAME_DATA11[5]	CEC_BUF0_RX_FRAME_DATA11[4]	CEC_BUF0_RX_FRAME_DATA11[3]	CEC_BUF0_RX_FRAME_DATA11[2]	CEC_BUF0_RX_FRAME_DATA11[1]	CEC_BUF0_RX_FRAME_DATA11[0]
0x22	0x00		r	CEC_BUF0_RX_FRAME_DATA12[7]	CEC_BUF0_RX_FRAME_DATA12[6]	CEC_BUF0_RX_FRAME_DATA12[5]	CEC_BUF0_RX_FRAME_DATA12[4]	CEC_BUF0_RX_FRAME_DATA12[3]	CEC_BUF0_RX_FRAME_DATA12[2]	CEC_BUF0_RX_FRAME_DATA12[1]	CEC_BUF0_RX_FRAME_DATA12[0]
0x23	0x00		r	CEC_BUF0_RX_FRAME_DATA13[7]	CEC_BUF0_RX_FRAME_DATA13[6]	CEC_BUF0_RX_FRAME_DATA13[5]	CEC_BUF0_RX_FRAME_DATA13[4]	CEC_BUF0_RX_FRAME_DATA13[3]	CEC_BUF0_RX_FRAME_DATA13[2]	CEC_BUF0_RX_FRAME_DATA13[1]	CEC_BUF0_RX_FRAME_DATA13[0]
0x24	0x00		r	CEC_BUF0_RX_FRAME_DATA14[7]	CEC_BUF0_RX_FRAME_DATA14[6]	CEC_BUF0_RX_FRAME_DATA14[5]	CEC_BUF0_RX_FRAME_DATA14[4]	CEC_BUF0_RX_FRAME_DATA14[3]	CEC_BUF0_RX_FRAME_DATA14[2]	CEC_BUF0_RX_FRAME_DATA14[1]	CEC_BUF0_RX_FRAME_DATA14[0]
0x25	0x00		r	-	-	-	CEC_BUF0_RX_FRAME_LENGTH[4]	CEC_BUF0_RX_FRAME_LENGTH[3]	CEC_BUF0_RX_FRAME_LENGTH[2]	CEC_BUF0_RX_FRAME_LENGTH[1]	CEC_BUF0_RX_FRAME_LENGTH[0]
0x27	0x10		rw	-	CEC_LOGICAL_ADDRESS_MASK_2	CEC_LOGICAL_ADDRESS_MASK_1	CEC_LOGICAL_ADDRESS_MASK_0	CEC_ERROR_REPORT_MODE	CEC_ERROR_DET_MODE	CEC_FORCE_NACK	CEC_FORCE_IGNORE
0x28	0xFF		rw	CEC_LOGICAL_ADDRESS1[3]	CEC_LOGICAL_ADDRESS1[2]	CEC_LOGICAL_ADDRESS1[1]	CEC_LOGICAL_ADDRESS1[0]	CEC_LOGICAL_ADDRESS0[3]	CEC_LOGICAL_ADDRESS0[2]	CEC_LOGICAL_ADDRESS0[1]	CEC_LOGICAL_ADDRESS0[0]
0x29	0x0F		rw	-	-	-	-	CEC_LOGICAL_ADDRESS2[3]	CEC_LOGICAL_ADDRESS2[2]	CEC_LOGICAL_ADDRESS2[1]	CEC_LOGICAL_ADDRESS2[0]
0x2A	0x3E		rw	-	-	-	-	-	-	-	CEC_POWER_UP
0x2B	0x07		rw	-	-	CEC_GLITCH_FILTER_CTRL[5]	CEC_GLITCH_FILTER_CTRL[4]	CEC_GLITCH_FILTER_CTRL[3]	CEC_GLITCH_FILTER_CTRL[2]	CEC_GLITCH_FILTER_CTRL[1]	CEC_GLITCH_FILTER_CTRL[0]
0x2C	0x00		sc	-	-	-	-	CEC_CLR_RX_RDY2	CEC_CLR_RX_RDY1	CEC_CLR_RX_RDY0	CEC_SOFT_RESET
0x4C	0x00		rw	-	-	-	-	-	CEC_DIS_AUTO_MODE	-	-
0x53	0x00		r	-	-	CEC_BUF2_TIMESTAMP[1]	CEC_BUF2_TIMESTAMP[0]	CEC_BUF1_TIMESTAMP[1]	CEC_BUF1_TIMESTAMP[0]	CEC_BUF0_TIMESTAMP[1]	CEC_BUF0_TIMESTAMP[0]
0x54	0x00		r	CEC_BUF1_RX_FRAME_HEADER[7]	CEC_BUF1_RX_FRAME_HEADER[6]	CEC_BUF1_RX_FRAME_HEADER[5]	CEC_BUF1_RX_FRAME_HEADER[4]	CEC_BUF1_RX_FRAME_HEADER[3]	CEC_BUF1_RX_FRAME_HEADER[2]	CEC_BUF1_RX_FRAME_HEADER[1]	CEC_BUF1_RX_FRAME_HEADER[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x55	0x00		r	CEC_BUF1_RX_FRAME_DATA0[7]	CEC_BUF1_RX_FRAME_DATA0[6]	CEC_BUF1_RX_FRAME_DATA0[5]	CEC_BUF1_RX_FRAME_DATA0[4]	CEC_BUF1_RX_FRAME_DATA0[3]	CEC_BUF1_RX_FRAME_DATA0[2]	CEC_BUF1_RX_FRAME_DATA0[1]	CEC_BUF1_RX_FRAME_DATA0[0]
0x56	0x00		r	CEC_BUF1_RX_FRAME_DATA1[7]	CEC_BUF1_RX_FRAME_DATA1[6]	CEC_BUF1_RX_FRAME_DATA1[5]	CEC_BUF1_RX_FRAME_DATA1[4]	CEC_BUF1_RX_FRAME_DATA1[3]	CEC_BUF1_RX_FRAME_DATA1[2]	CEC_BUF1_RX_FRAME_DATA1[1]	CEC_BUF1_RX_FRAME_DATA1[0]
0x57	0x00		r	CEC_BUF1_RX_FRAME_DATA2[7]	CEC_BUF1_RX_FRAME_DATA2[6]	CEC_BUF1_RX_FRAME_DATA2[5]	CEC_BUF1_RX_FRAME_DATA2[4]	CEC_BUF1_RX_FRAME_DATA2[3]	CEC_BUF1_RX_FRAME_DATA2[2]	CEC_BUF1_RX_FRAME_DATA2[1]	CEC_BUF1_RX_FRAME_DATA2[0]
0x58	0x00		r	CEC_BUF1_RX_FRAME_DATA3[7]	CEC_BUF1_RX_FRAME_DATA3[6]	CEC_BUF1_RX_FRAME_DATA3[5]	CEC_BUF1_RX_FRAME_DATA3[4]	CEC_BUF1_RX_FRAME_DATA3[3]	CEC_BUF1_RX_FRAME_DATA3[2]	CEC_BUF1_RX_FRAME_DATA3[1]	CEC_BUF1_RX_FRAME_DATA3[0]
0x59	0x00		r	CEC_BUF1_RX_FRAME_DATA4[7]	CEC_BUF1_RX_FRAME_DATA4[6]	CEC_BUF1_RX_FRAME_DATA4[5]	CEC_BUF1_RX_FRAME_DATA4[4]	CEC_BUF1_RX_FRAME_DATA4[3]	CEC_BUF1_RX_FRAME_DATA4[2]	CEC_BUF1_RX_FRAME_DATA4[1]	CEC_BUF1_RX_FRAME_DATA4[0]
0x5A	0x00		r	CEC_BUF1_RX_FRAME_DATA5[7]	CEC_BUF1_RX_FRAME_DATA5[6]	CEC_BUF1_RX_FRAME_DATA5[5]	CEC_BUF1_RX_FRAME_DATA5[4]	CEC_BUF1_RX_FRAME_DATA5[3]	CEC_BUF1_RX_FRAME_DATA5[2]	CEC_BUF1_RX_FRAME_DATA5[1]	CEC_BUF1_RX_FRAME_DATA5[0]
0x5B	0x00		r	CEC_BUF1_RX_FRAME_DATA6[7]	CEC_BUF1_RX_FRAME_DATA6[6]	CEC_BUF1_RX_FRAME_DATA6[5]	CEC_BUF1_RX_FRAME_DATA6[4]	CEC_BUF1_RX_FRAME_DATA6[3]	CEC_BUF1_RX_FRAME_DATA6[2]	CEC_BUF1_RX_FRAME_DATA6[1]	CEC_BUF1_RX_FRAME_DATA6[0]
0x5C	0x00		r	CEC_BUF1_RX_FRAME_DATA7[7]	CEC_BUF1_RX_FRAME_DATA7[6]	CEC_BUF1_RX_FRAME_DATA7[5]	CEC_BUF1_RX_FRAME_DATA7[4]	CEC_BUF1_RX_FRAME_DATA7[3]	CEC_BUF1_RX_FRAME_DATA7[2]	CEC_BUF1_RX_FRAME_DATA7[1]	CEC_BUF1_RX_FRAME_DATA7[0]
0x5D	0x00		r	CEC_BUF1_RX_FRAME_DATA8[7]	CEC_BUF1_RX_FRAME_DATA8[6]	CEC_BUF1_RX_FRAME_DATA8[5]	CEC_BUF1_RX_FRAME_DATA8[4]	CEC_BUF1_RX_FRAME_DATA8[3]	CEC_BUF1_RX_FRAME_DATA8[2]	CEC_BUF1_RX_FRAME_DATA8[1]	CEC_BUF1_RX_FRAME_DATA8[0]
0x5E	0x00		r	CEC_BUF1_RX_FRAME_DATA9[7]	CEC_BUF1_RX_FRAME_DATA9[6]	CEC_BUF1_RX_FRAME_DATA9[5]	CEC_BUF1_RX_FRAME_DATA9[4]	CEC_BUF1_RX_FRAME_DATA9[3]	CEC_BUF1_RX_FRAME_DATA9[2]	CEC_BUF1_RX_FRAME_DATA9[1]	CEC_BUF1_RX_FRAME_DATA9[0]
0x5F	0x00		r	CEC_BUF1_RX_FRAME_DATA10[7]	CEC_BUF1_RX_FRAME_DATA10[6]	CEC_BUF1_RX_FRAME_DATA10[5]	CEC_BUF1_RX_FRAME_DATA10[4]	CEC_BUF1_RX_FRAME_DATA10[3]	CEC_BUF1_RX_FRAME_DATA10[2]	CEC_BUF1_RX_FRAME_DATA10[1]	CEC_BUF1_RX_FRAME_DATA10[0]
0x60	0x00		r	CEC_BUF1_RX_FRAME_DATA11[7]	CEC_BUF1_RX_FRAME_DATA11[6]	CEC_BUF1_RX_FRAME_DATA11[5]	CEC_BUF1_RX_FRAME_DATA11[4]	CEC_BUF1_RX_FRAME_DATA11[3]	CEC_BUF1_RX_FRAME_DATA11[2]	CEC_BUF1_RX_FRAME_DATA11[1]	CEC_BUF1_RX_FRAME_DATA11[0]
0x61	0x00		r	CEC_BUF1_RX_FRAME_DATA12[7]	CEC_BUF1_RX_FRAME_DATA12[6]	CEC_BUF1_RX_FRAME_DATA12[5]	CEC_BUF1_RX_FRAME_DATA12[4]	CEC_BUF1_RX_FRAME_DATA12[3]	CEC_BUF1_RX_FRAME_DATA12[2]	CEC_BUF1_RX_FRAME_DATA12[1]	CEC_BUF1_RX_FRAME_DATA12[0]
0x62	0x00		r	CEC_BUF1_RX_FRAME_DATA13[7]	CEC_BUF1_RX_FRAME_DATA13[6]	CEC_BUF1_RX_FRAME_DATA13[5]	CEC_BUF1_RX_FRAME_DATA13[4]	CEC_BUF1_RX_FRAME_DATA13[3]	CEC_BUF1_RX_FRAME_DATA13[2]	CEC_BUF1_RX_FRAME_DATA13[1]	CEC_BUF1_RX_FRAME_DATA13[0]
0x63	0x00		r	CEC_BUF1_RX_FRAME_DATA14[7]	CEC_BUF1_RX_FRAME_DATA14[6]	CEC_BUF1_RX_FRAME_DATA14[5]	CEC_BUF1_RX_FRAME_DATA14[4]	CEC_BUF1_RX_FRAME_DATA14[3]	CEC_BUF1_RX_FRAME_DATA14[2]	CEC_BUF1_RX_FRAME_DATA14[1]	CEC_BUF1_RX_FRAME_DATA14[0]
0x64	0x00		r	-	-	-	CEC_BUF1_RX_FRAME_LENGTH[4]	CEC_BUF1_RX_FRAME_LENGTH[3]	CEC_BUF1_RX_FRAME_LENGTH[2]	CEC_BUF1_RX_FRAME_LENGTH[1]	CEC_BUF1_RX_FRAME_LENGTH[0]
0x65	0x00		r	CEC_BUF2_RX_FRAME_HEADER[7]	CEC_BUF2_RX_FRAME_HEADER[6]	CEC_BUF2_RX_FRAME_HEADER[5]	CEC_BUF2_RX_FRAME_HEADER[4]	CEC_BUF2_RX_FRAME_HEADER[3]	CEC_BUF2_RX_FRAME_HEADER[2]	CEC_BUF2_RX_FRAME_HEADER[1]	CEC_BUF2_RX_FRAME_HEADER[0]
0x66	0x00		r	CEC_BUF2_RX_FRAME_DATA0[7]	CEC_BUF2_RX_FRAME_DATA0[6]	CEC_BUF2_RX_FRAME_DATA0[5]	CEC_BUF2_RX_FRAME_DATA0[4]	CEC_BUF2_RX_FRAME_DATA0[3]	CEC_BUF2_RX_FRAME_DATA0[2]	CEC_BUF2_RX_FRAME_DATA0[1]	CEC_BUF2_RX_FRAME_DATA0[0]
0x67	0x00		r	CEC_BUF2_RX_FRAME_DATA1[7]	CEC_BUF2_RX_FRAME_DATA1[6]	CEC_BUF2_RX_FRAME_DATA1[5]	CEC_BUF2_RX_FRAME_DATA1[4]	CEC_BUF2_RX_FRAME_DATA1[3]	CEC_BUF2_RX_FRAME_DATA1[2]	CEC_BUF2_RX_FRAME_DATA1[1]	CEC_BUF2_RX_FRAME_DATA1[0]
0x68	0x00		r	CEC_BUF2_RX_FRAME_DATA2[7]	CEC_BUF2_RX_FRAME_DATA2[6]	CEC_BUF2_RX_FRAME_DATA2[5]	CEC_BUF2_RX_FRAME_DATA2[4]	CEC_BUF2_RX_FRAME_DATA2[3]	CEC_BUF2_RX_FRAME_DATA2[2]	CEC_BUF2_RX_FRAME_DATA2[1]	CEC_BUF2_RX_FRAME_DATA2[0]
0x69	0x00		r	CEC_BUF2_RX_FRAME_DATA3[7]	CEC_BUF2_RX_FRAME_DATA3[6]	CEC_BUF2_RX_FRAME_DATA3[5]	CEC_BUF2_RX_FRAME_DATA3[4]	CEC_BUF2_RX_FRAME_DATA3[3]	CEC_BUF2_RX_FRAME_DATA3[2]	CEC_BUF2_RX_FRAME_DATA3[1]	CEC_BUF2_RX_FRAME_DATA3[0]
0x6A	0x00		r	CEC_BUF2_RX_FRAME_DATA4[7]	CEC_BUF2_RX_FRAME_DATA4[6]	CEC_BUF2_RX_FRAME_DATA4[5]	CEC_BUF2_RX_FRAME_DATA4[4]	CEC_BUF2_RX_FRAME_DATA4[3]	CEC_BUF2_RX_FRAME_DATA4[2]	CEC_BUF2_RX_FRAME_DATA4[1]	CEC_BUF2_RX_FRAME_DATA4[0]
0x6B	0x00		r	CEC_BUF2_RX_FRAME_DATA5[7]	CEC_BUF2_RX_FRAME_DATA5[6]	CEC_BUF2_RX_FRAME_DATA5[5]	CEC_BUF2_RX_FRAME_DATA5[4]	CEC_BUF2_RX_FRAME_DATA5[3]	CEC_BUF2_RX_FRAME_DATA5[2]	CEC_BUF2_RX_FRAME_DATA5[1]	CEC_BUF2_RX_FRAME_DATA5[0]
0x6C	0x00		r	CEC_BUF2_RX_FRAME_DATA6[7]	CEC_BUF2_RX_FRAME_DATA6[6]	CEC_BUF2_RX_FRAME_DATA6[5]	CEC_BUF2_RX_FRAME_DATA6[4]	CEC_BUF2_RX_FRAME_DATA6[3]	CEC_BUF2_RX_FRAME_DATA6[2]	CEC_BUF2_RX_FRAME_DATA6[1]	CEC_BUF2_RX_FRAME_DATA6[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6D	0x00		r	CEC_BUF2_RX_FRAME_DATA7[7]	CEC_BUF2_RX_FRAME_DATA7[6]	CEC_BUF2_RX_FRAME_DATA7[5]	CEC_BUF2_RX_FRAME_DATA7[4]	CEC_BUF2_RX_FRAME_DATA7[3]	CEC_BUF2_RX_FRAME_DATA7[2]	CEC_BUF2_RX_FRAME_DATA7[1]	CEC_BUF2_RX_FRAME_DATA7[0]
0x6E	0x00		r	CEC_BUF2_RX_FRAME_DATA8[7]	CEC_BUF2_RX_FRAME_DATA8[6]	CEC_BUF2_RX_FRAME_DATA8[5]	CEC_BUF2_RX_FRAME_DATA8[4]	CEC_BUF2_RX_FRAME_DATA8[3]	CEC_BUF2_RX_FRAME_DATA8[2]	CEC_BUF2_RX_FRAME_DATA8[1]	CEC_BUF2_RX_FRAME_DATA8[0]
0x6F	0x00		r	CEC_BUF2_RX_FRAME_DATA9[7]	CEC_BUF2_RX_FRAME_DATA9[6]	CEC_BUF2_RX_FRAME_DATA9[5]	CEC_BUF2_RX_FRAME_DATA9[4]	CEC_BUF2_RX_FRAME_DATA9[3]	CEC_BUF2_RX_FRAME_DATA9[2]	CEC_BUF2_RX_FRAME_DATA9[1]	CEC_BUF2_RX_FRAME_DATA9[0]
0x70	0x00		r	CEC_BUF2_RX_FRAME_DATA10[7]	CEC_BUF2_RX_FRAME_DATA10[6]	CEC_BUF2_RX_FRAME_DATA10[5]	CEC_BUF2_RX_FRAME_DATA10[4]	CEC_BUF2_RX_FRAME_DATA10[3]	CEC_BUF2_RX_FRAME_DATA10[2]	CEC_BUF2_RX_FRAME_DATA10[1]	CEC_BUF2_RX_FRAME_DATA10[0]
0x71	0x00		r	CEC_BUF2_RX_FRAME_DATA11[7]	CEC_BUF2_RX_FRAME_DATA11[6]	CEC_BUF2_RX_FRAME_DATA11[5]	CEC_BUF2_RX_FRAME_DATA11[4]	CEC_BUF2_RX_FRAME_DATA11[3]	CEC_BUF2_RX_FRAME_DATA11[2]	CEC_BUF2_RX_FRAME_DATA11[1]	CEC_BUF2_RX_FRAME_DATA11[0]
0x72	0x00		r	CEC_BUF2_RX_FRAME_DATA12[7]	CEC_BUF2_RX_FRAME_DATA12[6]	CEC_BUF2_RX_FRAME_DATA12[5]	CEC_BUF2_RX_FRAME_DATA12[4]	CEC_BUF2_RX_FRAME_DATA12[3]	CEC_BUF2_RX_FRAME_DATA12[2]	CEC_BUF2_RX_FRAME_DATA12[1]	CEC_BUF2_RX_FRAME_DATA12[0]
0x73	0x00		r	CEC_BUF2_RX_FRAME_DATA13[7]	CEC_BUF2_RX_FRAME_DATA13[6]	CEC_BUF2_RX_FRAME_DATA13[5]	CEC_BUF2_RX_FRAME_DATA13[4]	CEC_BUF2_RX_FRAME_DATA13[3]	CEC_BUF2_RX_FRAME_DATA13[2]	CEC_BUF2_RX_FRAME_DATA13[1]	CEC_BUF2_RX_FRAME_DATA13[0]
0x74	0x00		r	CEC_BUF2_RX_FRAME_DATA14[7]	CEC_BUF2_RX_FRAME_DATA14[6]	CEC_BUF2_RX_FRAME_DATA14[5]	CEC_BUF2_RX_FRAME_DATA14[4]	CEC_BUF2_RX_FRAME_DATA14[3]	CEC_BUF2_RX_FRAME_DATA14[2]	CEC_BUF2_RX_FRAME_DATA14[1]	CEC_BUF2_RX_FRAME_DATA14[0]
0x75	0x00		r	-	-	-	CEC_BUF2_RX_FRAME_LENGTH[4]	CEC_BUF2_RX_FRAME_LENGTH[3]	CEC_BUF2_RX_FRAME_LENGTH[2]	CEC_BUF2_RX_FRAME_LENGTH[1]	CEC_BUF2_RX_FRAME_LENGTH[0]
0x76	0x00		r	-	-	-	-	-	CEC_RX_RDY2	CEC_RX_RDY1	CEC_RX_RDY0
0x77	0x00		rw	-	-	-	-	-	-	-	CEC_USE_ALL_BUFS
0x78	0x6D		rw	CEC_WAKE_OPCODE0[7]	CEC_WAKE_OPCODE0[6]	CEC_WAKE_OPCODE0[5]	CEC_WAKE_OPCODE0[4]	CEC_WAKE_OPCODE0[3]	CEC_WAKE_OPCODE0[2]	CEC_WAKE_OPCODE0[1]	CEC_WAKE_OPCODE0[0]
0x79	0x8F		rw	CEC_WAKE_OPCODE1[7]	CEC_WAKE_OPCODE1[6]	CEC_WAKE_OPCODE1[5]	CEC_WAKE_OPCODE1[4]	CEC_WAKE_OPCODE1[3]	CEC_WAKE_OPCODE1[2]	CEC_WAKE_OPCODE1[1]	CEC_WAKE_OPCODE1[0]
0x7A	0x82		rw	CEC_WAKE_OPCODE2[7]	CEC_WAKE_OPCODE2[6]	CEC_WAKE_OPCODE2[5]	CEC_WAKE_OPCODE2[4]	CEC_WAKE_OPCODE2[3]	CEC_WAKE_OPCODE2[2]	CEC_WAKE_OPCODE2[1]	CEC_WAKE_OPCODE2[0]
0x7B	0x04		rw	CEC_WAKE_OPCODE3[7]	CEC_WAKE_OPCODE3[6]	CEC_WAKE_OPCODE3[5]	CEC_WAKE_OPCODE3[4]	CEC_WAKE_OPCODE3[3]	CEC_WAKE_OPCODE3[2]	CEC_WAKE_OPCODE3[1]	CEC_WAKE_OPCODE3[0]
0x7C	0x0D		rw	CEC_WAKE_OPCODE4[7]	CEC_WAKE_OPCODE4[6]	CEC_WAKE_OPCODE4[5]	CEC_WAKE_OPCODE4[4]	CEC_WAKE_OPCODE4[3]	CEC_WAKE_OPCODE4[2]	CEC_WAKE_OPCODE4[1]	CEC_WAKE_OPCODE4[0]
0x7D	0x70		rw	CEC_WAKE_OPCODE5[7]	CEC_WAKE_OPCODE5[6]	CEC_WAKE_OPCODE5[5]	CEC_WAKE_OPCODE5[4]	CEC_WAKE_OPCODE5[3]	CEC_WAKE_OPCODE5[2]	CEC_WAKE_OPCODE5[1]	CEC_WAKE_OPCODE5[0]
0x7E	0x42		rw	CEC_WAKE_OPCODE6[7]	CEC_WAKE_OPCODE6[6]	CEC_WAKE_OPCODE6[5]	CEC_WAKE_OPCODE6[4]	CEC_WAKE_OPCODE6[3]	CEC_WAKE_OPCODE6[2]	CEC_WAKE_OPCODE6[1]	CEC_WAKE_OPCODE6[0]
0x7F	0x41		rw	CEC_WAKE_OPCODE7[7]	CEC_WAKE_OPCODE7[6]	CEC_WAKE_OPCODE7[5]	CEC_WAKE_OPCODE7[4]	CEC_WAKE_OPCODE7[3]	CEC_WAKE_OPCODE7[2]	CEC_WAKE_OPCODE7[1]	CEC_WAKE_OPCODE7[0]

1.7 AVLINK MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00		rw	-	-	-	-	-	-	AVL_TX_FRAME_MODE[1]	AVL_TX_FRAME_MODE[0]
0x01	0x00		rw	AVL_TX_FRAME_HEADER[7]	AVL_TX_FRAME_HEADER[6]	AVL_TX_FRAME_HEADER[5]	AVL_TX_FRAME_HEADER[4]	AVL_TX_FRAME_HEADER[3]	AVL_TX_FRAME_HEADER[2]	AVL_TX_FRAME_HEADER[1]	AVL_TX_FRAME_HEADER[0]
0x02	0x00		rw	AVL_TX_FRAME_DATA0[7]	AVL_TX_FRAME_DATA0[6]	AVL_TX_FRAME_DATA0[5]	AVL_TX_FRAME_DATA0[4]	AVL_TX_FRAME_DATA0[3]	AVL_TX_FRAME_DATA0[2]	AVL_TX_FRAME_DATA0[1]	AVL_TX_FRAME_DATA0[0]
0x03	0x00		rw	AVL_TX_FRAME_DATA1[7]	AVL_TX_FRAME_DATA1[6]	AVL_TX_FRAME_DATA1[5]	AVL_TX_FRAME_DATA1[4]	AVL_TX_FRAME_DATA1[3]	AVL_TX_FRAME_DATA1[2]	AVL_TX_FRAME_DATA1[1]	AVL_TX_FRAME_DATA1[0]
0x04	0x00		rw	AVL_TX_FRAME_DATA2[7]	AVL_TX_FRAME_DATA2[6]	AVL_TX_FRAME_DATA2[5]	AVL_TX_FRAME_DATA2[4]	AVL_TX_FRAME_DATA2[3]	AVL_TX_FRAME_DATA2[2]	AVL_TX_FRAME_DATA2[1]	AVL_TX_FRAME_DATA2[0]
0x05	0x00		rw	AVL_TX_FRAME_DATA3[7]	AVL_TX_FRAME_DATA3[6]	AVL_TX_FRAME_DATA3[5]	AVL_TX_FRAME_DATA3[4]	AVL_TX_FRAME_DATA3[3]	AVL_TX_FRAME_DATA3[2]	AVL_TX_FRAME_DATA3[1]	AVL_TX_FRAME_DATA3[0]
0x06	0x00		rw	AVL_TX_FRAME_DATA4[7]	AVL_TX_FRAME_DATA4[6]	AVL_TX_FRAME_DATA4[5]	AVL_TX_FRAME_DATA4[4]	AVL_TX_FRAME_DATA4[3]	AVL_TX_FRAME_DATA4[2]	AVL_TX_FRAME_DATA4[1]	AVL_TX_FRAME_DATA4[0]
0x07	0x00		rw	AVL_TX_FRAME_DATA5[7]	AVL_TX_FRAME_DATA5[6]	AVL_TX_FRAME_DATA5[5]	AVL_TX_FRAME_DATA5[4]	AVL_TX_FRAME_DATA5[3]	AVL_TX_FRAME_DATA5[2]	AVL_TX_FRAME_DATA5[1]	AVL_TX_FRAME_DATA5[0]
0x08	0x00		rw	AVL_TX_FRAME_DATA6[7]	AVL_TX_FRAME_DATA6[6]	AVL_TX_FRAME_DATA6[5]	AVL_TX_FRAME_DATA6[4]	AVL_TX_FRAME_DATA6[3]	AVL_TX_FRAME_DATA6[2]	AVL_TX_FRAME_DATA6[1]	AVL_TX_FRAME_DATA6[0]
0x09	0x00		rw	AVL_TX_FRAME_DATA7[7]	AVL_TX_FRAME_DATA7[6]	AVL_TX_FRAME_DATA7[5]	AVL_TX_FRAME_DATA7[4]	AVL_TX_FRAME_DATA7[3]	AVL_TX_FRAME_DATA7[2]	AVL_TX_FRAME_DATA7[1]	AVL_TX_FRAME_DATA7[0]
0x0A	0x00		rw	AVL_TX_FRAME_DATA8[7]	AVL_TX_FRAME_DATA8[6]	AVL_TX_FRAME_DATA8[5]	AVL_TX_FRAME_DATA8[4]	AVL_TX_FRAME_DATA8[3]	AVL_TX_FRAME_DATA8[2]	AVL_TX_FRAME_DATA8[1]	AVL_TX_FRAME_DATA8[0]
0x0B	0x00		rw	AVL_TX_FRAME_DATA9[7]	AVL_TX_FRAME_DATA9[6]	AVL_TX_FRAME_DATA9[5]	AVL_TX_FRAME_DATA9[4]	AVL_TX_FRAME_DATA9[3]	AVL_TX_FRAME_DATA9[2]	AVL_TX_FRAME_DATA9[1]	AVL_TX_FRAME_DATA9[0]
0x0C	0x00		rw	AVL_TX_FRAME_DATA10[7]	AVL_TX_FRAME_DATA10[6]	AVL_TX_FRAME_DATA10[5]	AVL_TX_FRAME_DATA10[4]	AVL_TX_FRAME_DATA10[3]	AVL_TX_FRAME_DATA10[2]	AVL_TX_FRAME_DATA10[1]	AVL_TX_FRAME_DATA10[0]
0x0D	0x00		rw	AVL_TX_FRAME_DATA11[7]	AVL_TX_FRAME_DATA11[6]	AVL_TX_FRAME_DATA11[5]	AVL_TX_FRAME_DATA11[4]	AVL_TX_FRAME_DATA11[3]	AVL_TX_FRAME_DATA11[2]	AVL_TX_FRAME_DATA11[1]	AVL_TX_FRAME_DATA11[0]
0x0E	0x00		rw	-	-	-	-	-	-	-	AVL_TX_FRAME_ECT
0x0F	0x00		rw	AVL_TX_FRAME_LENGTH[7]	AVL_TX_FRAME_LENGTH[6]	AVL_TX_FRAME_LENGTH[5]	AVL_TX_FRAME_LENGTH[4]	AVL_TX_FRAME_LENGTH[3]	AVL_TX_FRAME_LENGTH[2]	AVL_TX_FRAME_LENGTH[1]	AVL_TX_FRAME_LENGTH[0]
0x10	0x00		rw	-	-	-	-	-	-	-	AVL_TX_ENABLE
0x11	0x1C		rw	-	AVL_TX_SFT3[3]	AVL_TX_SFT3[2]	AVL_TX_SFT3[1]	AVL_TX_SFT3[0]	AVL_TX_RETRY[2]	AVL_TX_RETRY[1]	AVL_TX_RETRY[0]
0x12	0x75		rw	AVL_TX_SFT7[3]	AVL_TX_SFT7[2]	AVL_TX_SFT7[1]	AVL_TX_SFT7[0]	AVL_TX_SFT5[3]	AVL_TX_SFT5[2]	AVL_TX_SFT5[1]	AVL_TX_SFT5[0]
0x13	0x09		rw	-	-	-	-	AVL_TX_SFT9[3]	AVL_TX_SFT9[2]	AVL_TX_SFT9[1]	AVL_TX_SFT9[0]
0x14	0x00		r	-	-	-	-	AVL_TX_NACK_COUNTER[3]	AVL_TX_NACK_COUNTER[2]	AVL_TX_NACK_COUNTER[1]	AVL_TX_NACK_COUNTER[0]
0x15	0x00		r	-	-	-	-	-	-	AVL_RX_FRAME_MODE[1]	AVL_RX_FRAME_MODE[0]
0x16	0x00		r	AVL_RX_FRAME_HEADER[7]	AVL_RX_FRAME_HEADER[6]	AVL_RX_FRAME_HEADER[5]	AVL_RX_FRAME_HEADER[4]	AVL_RX_FRAME_HEADER[3]	AVL_RX_FRAME_HEADER[2]	AVL_RX_FRAME_HEADER[1]	AVL_RX_FRAME_HEADER[0]
0x17	0x00		r	AVL_RX_FRAME_DATA0[7]	AVL_RX_FRAME_DATA0[6]	AVL_RX_FRAME_DATA0[5]	AVL_RX_FRAME_DATA0[4]	AVL_RX_FRAME_DATA0[3]	AVL_RX_FRAME_DATA0[2]	AVL_RX_FRAME_DATA0[1]	AVL_RX_FRAME_DATA0[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x18	0x00		r	AVL_RX_FRAME_DATA1[7]	AVL_RX_FRAME_DATA1[6]	AVL_RX_FRAME_DATA1[5]	AVL_RX_FRAME_DATA1[4]	AVL_RX_FRAME_DATA1[3]	AVL_RX_FRAME_DATA1[2]	AVL_RX_FRAME_DATA1[1]	AVL_RX_FRAME_DATA1[0]
0x19	0x00		r	AVL_RX_FRAME_DATA2[7]	AVL_RX_FRAME_DATA2[6]	AVL_RX_FRAME_DATA2[5]	AVL_RX_FRAME_DATA2[4]	AVL_RX_FRAME_DATA2[3]	AVL_RX_FRAME_DATA2[2]	AVL_RX_FRAME_DATA2[1]	AVL_RX_FRAME_DATA2[0]
0x1A	0x00		r	AVL_RX_FRAME_DATA3[7]	AVL_RX_FRAME_DATA3[6]	AVL_RX_FRAME_DATA3[5]	AVL_RX_FRAME_DATA3[4]	AVL_RX_FRAME_DATA3[3]	AVL_RX_FRAME_DATA3[2]	AVL_RX_FRAME_DATA3[1]	AVL_RX_FRAME_DATA3[0]
0x1B	0x00		r	AVL_RX_FRAME_DATA4[7]	AVL_RX_FRAME_DATA4[6]	AVL_RX_FRAME_DATA4[5]	AVL_RX_FRAME_DATA4[4]	AVL_RX_FRAME_DATA4[3]	AVL_RX_FRAME_DATA4[2]	AVL_RX_FRAME_DATA4[1]	AVL_RX_FRAME_DATA4[0]
0x1C	0x00		r	AVL_RX_FRAME_DATA5[7]	AVL_RX_FRAME_DATA5[6]	AVL_RX_FRAME_DATA5[5]	AVL_RX_FRAME_DATA5[4]	AVL_RX_FRAME_DATA5[3]	AVL_RX_FRAME_DATA5[2]	AVL_RX_FRAME_DATA5[1]	AVL_RX_FRAME_DATA5[0]
0x1D	0x00		r	AVL_RX_FRAME_DATA6[7]	AVL_RX_FRAME_DATA6[6]	AVL_RX_FRAME_DATA6[5]	AVL_RX_FRAME_DATA6[4]	AVL_RX_FRAME_DATA6[3]	AVL_RX_FRAME_DATA6[2]	AVL_RX_FRAME_DATA6[1]	AVL_RX_FRAME_DATA6[0]
0x1E	0x00		r	AVL_RX_FRAME_DATA7[7]	AVL_RX_FRAME_DATA7[6]	AVL_RX_FRAME_DATA7[5]	AVL_RX_FRAME_DATA7[4]	AVL_RX_FRAME_DATA7[3]	AVL_RX_FRAME_DATA7[2]	AVL_RX_FRAME_DATA7[1]	AVL_RX_FRAME_DATA7[0]
0x1F	0x00		r	AVL_RX_FRAME_DATA8[7]	AVL_RX_FRAME_DATA8[6]	AVL_RX_FRAME_DATA8[5]	AVL_RX_FRAME_DATA8[4]	AVL_RX_FRAME_DATA8[3]	AVL_RX_FRAME_DATA8[2]	AVL_RX_FRAME_DATA8[1]	AVL_RX_FRAME_DATA8[0]
0x20	0x00		r	AVL_RX_FRAME_DATA9[7]	AVL_RX_FRAME_DATA9[6]	AVL_RX_FRAME_DATA9[5]	AVL_RX_FRAME_DATA9[4]	AVL_RX_FRAME_DATA9[3]	AVL_RX_FRAME_DATA9[2]	AVL_RX_FRAME_DATA9[1]	AVL_RX_FRAME_DATA9[0]
0x21	0x00		r	AVL_RX_FRAME_DATA10[7]	AVL_RX_FRAME_DATA10[6]	AVL_RX_FRAME_DATA10[5]	AVL_RX_FRAME_DATA10[4]	AVL_RX_FRAME_DATA10[3]	AVL_RX_FRAME_DATA10[2]	AVL_RX_FRAME_DATA10[1]	AVL_RX_FRAME_DATA10[0]
0x22	0x00		r	AVL_RX_FRAME_DATA11[7]	AVL_RX_FRAME_DATA11[6]	AVL_RX_FRAME_DATA11[5]	AVL_RX_FRAME_DATA11[4]	AVL_RX_FRAME_DATA11[3]	AVL_RX_FRAME_DATA11[2]	AVL_RX_FRAME_DATA11[1]	AVL_RX_FRAME_DATA11[0]
0x23	0x00		r	-	-	-	-	-	-	-	AVL_RX_FRAME_ECT
0x24	0x00		r	AVL_RX_FRAME_LENGTH[7]	AVL_RX_FRAME_LENGTH[6]	AVL_RX_FRAME_LENGTH[5]	AVL_RX_FRAME_LENGTH[4]	AVL_RX_FRAME_LENGTH[3]	AVL_RX_FRAME_LENGTH[2]	AVL_RX_FRAME_LENGTH[1]	AVL_RX_FRAME_LENGTH[0]
0x25	0x00		rw	-	-	-	-	-	-	-	AVL_RX_ENABLE
0x26	0x10		rw	-	AVL_LOGICAL_ADDRESS_MASK_2	AVL_LOGICAL_ADDRESS_MASK_1	AVL_LOGICAL_ADDRESS_MASK_0	AVL_ERROR_REPORT_MODE	AVL_ERROR_DET_MODE	AVL_FORCE_NACK	AVL_FORCE_IGNORE
0x27	0x00		rw	-	-	-	-	-	-	-	AVL_AVLINK_POWER_UP
0x28	0x07		rw	-	-	AVL_GLITCH_FILTER_CTRL[5]	AVL_GLITCH_FILTER_CTRL[4]	AVL_GLITCH_FILTER_CTRL[3]	AVL_GLITCH_FILTER_CTRL[2]	AVL_GLITCH_FILTER_CTRL[1]	AVL_GLITCH_FILTER_CTRL[0]
0x29	0x00		sc	-	-	-	-	-	-	AVL_FORCE_ERROR	AVL_SOFT_RESET
0x2A	0xFF		rw	AVL_LOGICAL_ADDRESS1[3]	AVL_LOGICAL_ADDRESS1[2]	AVL_LOGICAL_ADDRESS1[1]	AVL_LOGICAL_ADDRESS1[0]	AVL_LOGICAL_ADDRESS0[3]	AVL_LOGICAL_ADDRESS0[2]	AVL_LOGICAL_ADDRESS0[1]	AVL_LOGICAL_ADDRESS0[0]
0x2B	0x0F		rw	-	-	-	-	AVL_LOGICAL_ADDRESS2[3]	AVL_LOGICAL_ADDRESS2[2]	AVL_LOGICAL_ADDRESS2[1]	AVL_LOGICAL_ADDRESS2[0]
0x2C	0x0F		rw	AVL_ST_TOTAL_H[7]	AVL_ST_TOTAL_H[6]	AVL_ST_TOTAL_H[5]	AVL_ST_TOTAL_H[4]	AVL_ST_TOTAL_H[3]	AVL_ST_TOTAL_H[2]	AVL_ST_TOTAL_H[1]	AVL_ST_TOTAL_H[0]
0x2D	0xBB		rw	AVL_ST_TOTAL_L[7]	AVL_ST_TOTAL_L[6]	AVL_ST_TOTAL_L[5]	AVL_ST_TOTAL_L[4]	AVL_ST_TOTAL_L[3]	AVL_ST_TOTAL_L[2]	AVL_ST_TOTAL_L[1]	AVL_ST_TOTAL_L[0]
0x2E	0x0E		rw	AVL_ST_TOTAL_MIN_H[7]	AVL_ST_TOTAL_MIN_H[6]	AVL_ST_TOTAL_MIN_H[5]	AVL_ST_TOTAL_MIN_H[4]	AVL_ST_TOTAL_MIN_H[3]	AVL_ST_TOTAL_MIN_H[2]	AVL_ST_TOTAL_MIN_H[1]	AVL_ST_TOTAL_MIN_H[0]
0x2F	0xDB		rw	AVL_ST_TOTAL_MIN_L[7]	AVL_ST_TOTAL_MIN_L[6]	AVL_ST_TOTAL_MIN_L[5]	AVL_ST_TOTAL_MIN_L[4]	AVL_ST_TOTAL_MIN_L[3]	AVL_ST_TOTAL_MIN_L[2]	AVL_ST_TOTAL_MIN_L[1]	AVL_ST_TOTAL_MIN_L[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x30	0x10		rw	AVL_ST_TOTAL_MAX_H[7]	AVL_ST_TOTAL_MAX_H[6]	AVL_ST_TOTAL_MAX_H[5]	AVL_ST_TOTAL_MAX_H[4]	AVL_ST_TOTAL_MAX_H[3]	AVL_ST_TOTAL_MAX_H[2]	AVL_ST_TOTAL_MAX_H[1]	AVL_ST_TOTAL_MAX_H[0]
0x31	0x9B		rw	AVL_ST_TOTAL_MAX_L[7]	AVL_ST_TOTAL_MAX_L[6]	AVL_ST_TOTAL_MAX_L[5]	AVL_ST_TOTAL_MAX_L[4]	AVL_ST_TOTAL_MAX_L[3]	AVL_ST_TOTAL_MAX_L[2]	AVL_ST_TOTAL_MAX_L[1]	AVL_ST_TOTAL_MAX_L[0]
0x32	0x0C		rw	AVL_ST_LOW_H[7]	AVL_ST_LOW_H[6]	AVL_ST_LOW_H[5]	AVL_ST_LOW_H[4]	AVL_ST_LOW_H[3]	AVL_ST_LOW_H[2]	AVL_ST_LOW_H[1]	AVL_ST_LOW_H[0]
0x33	0xEF		rw	AVL_ST_LOW_L[7]	AVL_ST_LOW_L[6]	AVL_ST_LOW_L[5]	AVL_ST_LOW_L[4]	AVL_ST_LOW_L[3]	AVL_ST_LOW_L[2]	AVL_ST_LOW_L[1]	AVL_ST_LOW_L[0]
0x34	0x0C		rw	AVL_ST_LOW_MINIMUM_H[7]	AVL_ST_LOW_MINIMUM_H[6]	AVL_ST_LOW_MINIMUM_H[5]	AVL_ST_LOW_MINIMUM_H[4]	AVL_ST_LOW_MINIMUM_H[3]	AVL_ST_LOW_MINIMUM_H[2]	AVL_ST_LOW_MINIMUM_H[1]	AVL_ST_LOW_MINIMUM_H[0]
0x35	0x0F		rw	AVL_ST_LOW_MINIMUM_L[7]	AVL_ST_LOW_MINIMUM_L[6]	AVL_ST_LOW_MINIMUM_L[5]	AVL_ST_LOW_MINIMUM_L[4]	AVL_ST_LOW_MINIMUM_L[3]	AVL_ST_LOW_MINIMUM_L[2]	AVL_ST_LOW_MINIMUM_L[1]	AVL_ST_LOW_MINIMUM_L[0]
0x36	0x0D		rw	AVL_ST_LOW_MAXIMUM_H[7]	AVL_ST_LOW_MAXIMUM_H[6]	AVL_ST_LOW_MAXIMUM_H[5]	AVL_ST_LOW_MAXIMUM_H[4]	AVL_ST_LOW_MAXIMUM_H[3]	AVL_ST_LOW_MAXIMUM_H[2]	AVL_ST_LOW_MAXIMUM_H[1]	AVL_ST_LOW_MAXIMUM_H[0]
0x37	0xCF		rw	AVL_ST_LOW_MAXIMUM_L[7]	AVL_ST_LOW_MAXIMUM_L[6]	AVL_ST_LOW_MAXIMUM_L[5]	AVL_ST_LOW_MAXIMUM_L[4]	AVL_ST_LOW_MAXIMUM_L[3]	AVL_ST_LOW_MAXIMUM_L[2]	AVL_ST_LOW_MAXIMUM_L[1]	AVL_ST_LOW_MAXIMUM_L[0]
0x38	0x08		rw	AVL_BIT_TOTAL_H[7]	AVL_BIT_TOTAL_H[6]	AVL_BIT_TOTAL_H[5]	AVL_BIT_TOTAL_H[4]	AVL_BIT_TOTAL_H[3]	AVL_BIT_TOTAL_H[2]	AVL_BIT_TOTAL_H[1]	AVL_BIT_TOTAL_H[0]
0x39	0x64		rw	AVL_BIT_TOTAL_L[7]	AVL_BIT_TOTAL_L[6]	AVL_BIT_TOTAL_L[5]	AVL_BIT_TOTAL_L[4]	AVL_BIT_TOTAL_L[3]	AVL_BIT_TOTAL_L[2]	AVL_BIT_TOTAL_L[1]	AVL_BIT_TOTAL_L[0]
0x3A	0x06		rw	AVL_BIT_TOTAL_MIN_H[7]	AVL_BIT_TOTAL_MIN_H[6]	AVL_BIT_TOTAL_MIN_H[5]	AVL_BIT_TOTAL_MIN_H[4]	AVL_BIT_TOTAL_MIN_H[3]	AVL_BIT_TOTAL_MIN_H[2]	AVL_BIT_TOTAL_MIN_H[1]	AVL_BIT_TOTAL_MIN_H[0]
0x3B	0xFE		rw	AVL_BIT_TOTAL_MIN_L[7]	AVL_BIT_TOTAL_MIN_L[6]	AVL_BIT_TOTAL_MIN_L[5]	AVL_BIT_TOTAL_MIN_L[4]	AVL_BIT_TOTAL_MIN_L[3]	AVL_BIT_TOTAL_MIN_L[2]	AVL_BIT_TOTAL_MIN_L[1]	AVL_BIT_TOTAL_MIN_L[0]
0x3C	0x09		rw	AVL_BIT_TOTAL_MAX_H[7]	AVL_BIT_TOTAL_MAX_H[6]	AVL_BIT_TOTAL_MAX_H[5]	AVL_BIT_TOTAL_MAX_H[4]	AVL_BIT_TOTAL_MAX_H[3]	AVL_BIT_TOTAL_MAX_H[2]	AVL_BIT_TOTAL_MAX_H[1]	AVL_BIT_TOTAL_MAX_H[0]
0x3D	0xCA		rw	AVL_BIT_TOTAL_MAX_L[7]	AVL_BIT_TOTAL_MAX_L[6]	AVL_BIT_TOTAL_MAX_L[5]	AVL_BIT_TOTAL_MAX_L[4]	AVL_BIT_TOTAL_MAX_L[3]	AVL_BIT_TOTAL_MAX_L[2]	AVL_BIT_TOTAL_MAX_L[1]	AVL_BIT_TOTAL_MAX_L[0]
0x3E	0x02		rw	AVL_BIT_LOW_ONE_H[7]	AVL_BIT_LOW_ONE_H[6]	AVL_BIT_LOW_ONE_H[5]	AVL_BIT_LOW_ONE_H[4]	AVL_BIT_LOW_ONE_H[3]	AVL_BIT_LOW_ONE_H[2]	AVL_BIT_LOW_ONE_H[1]	AVL_BIT_LOW_ONE_H[0]
0x3F	0x19		rw	AVL_BIT_LOW_ONE_L[7]	AVL_BIT_LOW_ONE_L[6]	AVL_BIT_LOW_ONE_L[5]	AVL_BIT_LOW_ONE_L[4]	AVL_BIT_LOW_ONE_L[3]	AVL_BIT_LOW_ONE_L[2]	AVL_BIT_LOW_ONE_L[1]	AVL_BIT_LOW_ONE_L[0]
0x40	0x01		rw	AVL_BIT_LOW_ONE_MIN_H[7]	AVL_BIT_LOW_ONE_MIN_H[6]	AVL_BIT_LOW_ONE_MIN_H[5]	AVL_BIT_LOW_ONE_MIN_H[4]	AVL_BIT_LOW_ONE_MIN_H[3]	AVL_BIT_LOW_ONE_MIN_H[2]	AVL_BIT_LOW_ONE_MIN_H[1]	AVL_BIT_LOW_ONE_MIN_H[0]
0x41	0x39		rw	AVL_BIT_LOW_ONE_MIN_L[7]	AVL_BIT_LOW_ONE_MIN_L[6]	AVL_BIT_LOW_ONE_MIN_L[5]	AVL_BIT_LOW_ONE_MIN_L[4]	AVL_BIT_LOW_ONE_MIN_L[3]	AVL_BIT_LOW_ONE_MIN_L[2]	AVL_BIT_LOW_ONE_MIN_L[1]	AVL_BIT_LOW_ONE_MIN_L[0]
0x42	0x02		rw	AVL_BIT_LOW_ONE_MAX_H[7]	AVL_BIT_LOW_ONE_MAX_H[6]	AVL_BIT_LOW_ONE_MAX_H[5]	AVL_BIT_LOW_ONE_MAX_H[4]	AVL_BIT_LOW_ONE_MAX_H[3]	AVL_BIT_LOW_ONE_MAX_H[2]	AVL_BIT_LOW_ONE_MAX_H[1]	AVL_BIT_LOW_ONE_MAX_H[0]
0x43	0xF9		rw	AVL_BIT_LOW_ONE_MAX_L[7]	AVL_BIT_LOW_ONE_MAX_L[6]	AVL_BIT_LOW_ONE_MAX_L[5]	AVL_BIT_LOW_ONE_MAX_L[4]	AVL_BIT_LOW_ONE_MAX_L[3]	AVL_BIT_LOW_ONE_MAX_L[2]	AVL_BIT_LOW_ONE_MAX_L[1]	AVL_BIT_LOW_ONE_MAX_L[0]
0x44	0x05		rw	AVL_BIT_LOW_ZERO_H[7]	AVL_BIT_LOW_ZERO_H[6]	AVL_BIT_LOW_ZERO_H[5]	AVL_BIT_LOW_ZERO_H[4]	AVL_BIT_LOW_ZERO_H[3]	AVL_BIT_LOW_ZERO_H[2]	AVL_BIT_LOW_ZERO_H[1]	AVL_BIT_LOW_ZERO_H[0]
0x45	0x3E		rw	AVL_BIT_LOW_ZERO_L[7]	AVL_BIT_LOW_ZERO_L[6]	AVL_BIT_LOW_ZERO_L[5]	AVL_BIT_LOW_ZERO_L[4]	AVL_BIT_LOW_ZERO_L[3]	AVL_BIT_LOW_ZERO_L[2]	AVL_BIT_LOW_ZERO_L[1]	AVL_BIT_LOW_ZERO_L[0]
0x46	0x05		rw	AVL_BIT_LOW_MAX_H[7]	AVL_BIT_LOW_MAX_H[6]	AVL_BIT_LOW_MAX_H[5]	AVL_BIT_LOW_MAX_H[4]	AVL_BIT_LOW_MAX_H[3]	AVL_BIT_LOW_MAX_H[2]	AVL_BIT_LOW_MAX_H[1]	AVL_BIT_LOW_MAX_H[0]
0x47	0xF1		rw	AVL_BIT_LOW_MAX_L[7]	AVL_BIT_LOW_MAX_L[6]	AVL_BIT_LOW_MAX_L[5]	AVL_BIT_LOW_MAX_L[4]	AVL_BIT_LOW_MAX_L[3]	AVL_BIT_LOW_MAX_L[2]	AVL_BIT_LOW_MAX_L[1]	AVL_BIT_LOW_MAX_L[0]
0x48	0x04		rw	AVL_BIT_LOW_ZERO_MIN_H[7]	AVL_BIT_LOW_ZERO_MIN_H[6]	AVL_BIT_LOW_ZERO_MIN_H[5]	AVL_BIT_LOW_ZERO_MIN_H[4]	AVL_BIT_LOW_ZERO_MIN_H[3]	AVL_BIT_LOW_ZERO_MIN_H[2]	AVL_BIT_LOW_ZERO_MIN_H[1]	AVL_BIT_LOW_ZERO_MIN_H[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x49	0x8B		rw	AVL_BIT_LOW_ZERO_MIN_L[7]	AVL_BIT_LOW_ZERO_MIN_L[6]	AVL_BIT_LOW_ZERO_MIN_L[5]	AVL_BIT_LOW_ZERO_MIN_L[4]	AVL_BIT_LOW_ZERO_MIN_L[3]	AVL_BIT_LOW_ZERO_MIN_L[2]	AVL_BIT_LOW_ZERO_MIN_L[1]	AVL_BIT_LOW_ZERO_MIN_L[0]
0x4A	0x03		rw	AVL_SAMPLE_TIME_H[7]	AVL_SAMPLE_TIME_H[6]	AVL_SAMPLE_TIME_H[5]	AVL_SAMPLE_TIME_H[4]	AVL_SAMPLE_TIME_H[3]	AVL_SAMPLE_TIME_H[2]	AVL_SAMPLE_TIME_H[1]	AVL_SAMPLE_TIME_H[0]
0x4B	0xAC		rw	AVL_SAMPLE_TIME_L[7]	AVL_SAMPLE_TIME_L[6]	AVL_SAMPLE_TIME_L[5]	AVL_SAMPLE_TIME_L[4]	AVL_SAMPLE_TIME_L[3]	AVL_SAMPLE_TIME_L[2]	AVL_SAMPLE_TIME_L[1]	AVL_SAMPLE_TIME_L[0]
0x4C	0x0C		rw	AVL_LINE_ERROR_TIME_H[7]	AVL_LINE_ERROR_TIME_H[6]	AVL_LINE_ERROR_TIME_H[5]	AVL_LINE_ERROR_TIME_H[4]	AVL_LINE_ERROR_TIME_H[3]	AVL_LINE_ERROR_TIME_H[2]	AVL_LINE_ERROR_TIME_H[1]	AVL_LINE_ERROR_TIME_H[0]
0x4D	0x96		rw	AVL_LINE_ERROR_TIME_L[7]	AVL_LINE_ERROR_TIME_L[6]	AVL_LINE_ERROR_TIME_L[5]	AVL_LINE_ERROR_TIME_L[4]	AVL_LINE_ERROR_TIME_L[3]	AVL_LINE_ERROR_TIME_L[2]	AVL_LINE_ERROR_TIME_L[1]	AVL_LINE_ERROR_TIME_L[0]
0x4E	0x00		rw	AVL_RISE_TIME_H[7]	AVL_RISE_TIME_H[6]	AVL_RISE_TIME_H[5]	AVL_RISE_TIME_H[4]	AVL_RISE_TIME_H[3]	AVL_RISE_TIME_H[2]	AVL_RISE_TIME_H[1]	AVL_RISE_TIME_H[0]
0x4F	0x70		rw	AVL_RISE_TIME_L[7]	AVL_RISE_TIME_L[6]	AVL_RISE_TIME_L[5]	AVL_RISE_TIME_L[4]	AVL_RISE_TIME_L[3]	AVL_RISE_TIME_L[2]	AVL_RISE_TIME_L[1]	AVL_RISE_TIME_L[0]
0x50	0x00		rw	-	-	-	-	-	-	-	AVL_BIT_LOW_DETMODE
0x51	0x00		rw	-	-	-	-	-	-	-	AVL_TIMING_MAN
0x52	0x00		rw	-	-	-	-	-	-	-	AVL_MODE00_HEADER_VALIDATE
0x53	0x00		rw	AVL_PROP_DELAY_H[7]	AVL_PROP_DELAY_H[6]	AVL_PROP_DELAY_H[5]	AVL_PROP_DELAY_H[4]	AVL_PROP_DELAY_H[3]	AVL_PROP_DELAY_H[2]	AVL_PROP_DELAY_H[1]	AVL_PROP_DELAY_H[0]
0x54	0x00		rw	AVL_PROP_DELAY_L[7]	AVL_PROP_DELAY_L[6]	AVL_PROP_DELAY_L[5]	AVL_PROP_DELAY_L[4]	AVL_PROP_DELAY_L[3]	AVL_PROP_DELAY_L[2]	AVL_PROP_DELAY_L[1]	AVL_PROP_DELAY_L[0]
0x55	0x3F		rw	-	-	AVL_RX_DEVICE_CAPABILITY_ARB[5]	AVL_RX_DEVICE_CAPABILITY_ARB[4]	AVL_RX_DEVICE_CAPABILITY_ARB[3]	AVL_RX_DEVICE_CAPABILITY_ARB[2]	AVL_RX_DEVICE_CAPABILITY_ARB[1]	AVL_RX_DEVICE_CAPABILITY_ARB[0]
0x56	0x00		r	-	-	AVL_TX_RECEIVED_ARB[5]	AVL_TX_RECEIVED_ARB[4]	AVL_TX_RECEIVED_ARB[3]	AVL_TX_RECEIVED_ARB[2]	AVL_TX_RECEIVED_ARB[1]	AVL_TX_RECEIVED_ARB[0]
0x58	0x7C		rw	AVL_RX_EXPECT_FRAME_LENGTH[7]	AVL_RX_EXPECT_FRAME_LENGTH[6]	AVL_RX_EXPECT_FRAME_LENGTH[5]	AVL_RX_EXPECT_FRAME_LENGTH[4]	AVL_RX_EXPECT_FRAME_LENGTH[3]	AVL_RX_EXPECT_FRAME_LENGTH[2]	AVL_RX_EXPECT_FRAME_LENGTH[1]	AVL_RX_EXPECT_FRAME_LENGTH[0]

1.8 SDP IO MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x29	0x00	MEMORY_PAD_CONTROL	rw	-	-	-	SDP_TRI_MEMORY_IF	-	-	-	-
0x51	0x00	RINGING_REDUCTION_CONTROL_1	rw	SDP_RING_RED_EN	SDP_RING_RED_LEVEL[6]	SDP_RING_RED_LEVEL[5]	SDP_RING_RED_LEVEL[4]	SDP_RING_RED_LEVEL[3]	SDP_RING_RED_LEVEL[2]	SDP_RING_RED_LEVEL[1]	SDP_RING_RED_LEVEL[0]
0x60	0x00	RESETS	sc	-	-	-	-	-	-	-	SDP_MEM_SM_RESET
0x66	0x01	SFL_CONFIGURATION_1	rw	SDP_MAN_SFL_STANDARD[3]	SDP_MAN_SFL_STANDARD[2]	SDP_MAN_SFL_STANDARD[1]	SDP_MAN_SFL_STANDARD[0]	-	-	SDP_MAN_SFL_STD_EN	SDP_AUTO_SFL_STD_EN
0x67	0x04	SFL_CONFIGURATION_2	rw	-	-	-	-	-	SDP_SFL_EN	-	SDP_SFL_INV_PSW
0x6F	0x00	MEMORY_ARBITER_CONTROL	rw	-	-	-	-	-	-	SDP_FREEZE_FRAME	SDP_SDRAM_MEM
0x8C	0x00	AUX_EAV_POSITION_1	rw	-	-	-	-	SDP_AUX_EAV_POS_ADJ[11]	SDP_AUX_EAV_POS_ADJ[10]	SDP_AUX_EAV_POS_ADJ[9]	SDP_AUX_EAV_POS_ADJ[8]
0x8D	0x00	AUX_EAV_POSITION_2	rw	SDP_AUX_EAV_POS_ADJ[7]	SDP_AUX_EAV_POS_ADJ[6]	SDP_AUX_EAV_POS_ADJ[5]	SDP_AUX_EAV_POS_ADJ[4]	SDP_AUX_EAV_POS_ADJ[3]	SDP_AUX_EAV_POS_ADJ[2]	SDP_AUX_EAV_POS_ADJ[1]	SDP_AUX_EAV_POS_ADJ[0]
0x8E	0x00	AUX_SAV_POSITION_1	rw	-	-	-	-	SDP_AUX_SAV_POS_ADJ[11]	SDP_AUX_SAV_POS_ADJ[10]	SDP_AUX_SAV_POS_ADJ[9]	SDP_AUX_SAV_POS_ADJ[8]
0x8F	0x00	AUX_SAV_POSITION_2	rw	SDP_AUX_SAV_POS_ADJ[7]	SDP_AUX_SAV_POS_ADJ[6]	SDP_AUX_SAV_POS_ADJ[5]	SDP_AUX_SAV_POS_ADJ[4]	SDP_AUX_SAV_POS_ADJ[3]	SDP_AUX_SAV_POS_ADJ[2]	SDP_AUX_SAV_POS_ADJ[1]	SDP_AUX_SAV_POS_ADJ[0]
0x90	0x00	EAV_POSITION_1	rw	-	-	-	-	SDP_EAV_POS_ADJ[11]	SDP_EAV_POS_ADJ[10]	SDP_EAV_POS_ADJ[9]	SDP_EAV_POS_ADJ[8]
0x91	0x00	EAV_POSITION_2	rw	SDP_EAV_POS_ADJ[7]	SDP_EAV_POS_ADJ[6]	SDP_EAV_POS_ADJ[5]	SDP_EAV_POS_ADJ[4]	SDP_EAV_POS_ADJ[3]	SDP_EAV_POS_ADJ[2]	SDP_EAV_POS_ADJ[1]	SDP_EAV_POS_ADJ[0]
0x92	0x00	SAV_POSITION_1	rw	-	-	-	-	SDP_SAV_POS_ADJ[11]	SDP_SAV_POS_ADJ[10]	SDP_SAV_POS_ADJ[9]	SDP_SAV_POS_ADJ[8]
0x93	0x00	SAV_POSITION_2	rw	SDP_SAV_POS_ADJ[7]	SDP_SAV_POS_ADJ[6]	SDP_SAV_POS_ADJ[5]	SDP_SAV_POS_ADJ[4]	SDP_SAV_POS_ADJ[3]	SDP_SAV_POS_ADJ[2]	SDP_SAV_POS_ADJ[1]	SDP_SAV_POS_ADJ[0]
0x94	0x00	HSYNC_BEGIN_1	rw	-	-	-	-	SDP_HS_BEG_ADJ[11]	SDP_HS_BEG_ADJ[10]	SDP_HS_BEG_ADJ[9]	SDP_HS_BEG_ADJ[8]
0x95	0x00	HSYNC_BEGIN_2	rw	SDP_HS_BEG_ADJ[7]	SDP_HS_BEG_ADJ[6]	SDP_HS_BEG_ADJ[5]	SDP_HS_BEG_ADJ[4]	SDP_HS_BEG_ADJ[3]	SDP_HS_BEG_ADJ[2]	SDP_HS_BEG_ADJ[1]	SDP_HS_BEG_ADJ[0]
0x96	0x00	HSYNC_WIDTH_1	rw	-	-	-	-	SDP_HS_WIDTH[11]	SDP_HS_WIDTH[10]	SDP_HS_WIDTH[9]	SDP_HS_WIDTH[8]
0x97	0x20	HSYNC_WIDTH_2	rw	SDP_HS_WIDTH[7]	SDP_HS_WIDTH[6]	SDP_HS_WIDTH[5]	SDP_HS_WIDTH[4]	SDP_HS_WIDTH[3]	SDP_HS_WIDTH[2]	SDP_HS_WIDTH[1]	SDP_HS_WIDTH[0]
0x98	0x00	DE_HORIZONTAL_BEGIN_1	rw	-	-	-	-	SDP_DE_H_BEG_ADJ[11]	SDP_DE_H_BEG_ADJ[10]	SDP_DE_H_BEG_ADJ[9]	SDP_DE_H_BEG_ADJ[8]
0x99	0x00	DE_HORIZONTAL_BEGIN_2	rw	SDP_DE_H_BEG_ADJ[7]	SDP_DE_H_BEG_ADJ[6]	SDP_DE_H_BEG_ADJ[5]	SDP_DE_H_BEG_ADJ[4]	SDP_DE_H_BEG_ADJ[3]	SDP_DE_H_BEG_ADJ[2]	SDP_DE_H_BEG_ADJ[1]	SDP_DE_H_BEG_ADJ[0]
0x9A	0x00	DE_HORIZONTAL_END_1	rw	-	-	-	-	SDP_DE_H_END_ADJ[11]	SDP_DE_H_END_ADJ[10]	SDP_DE_H_END_ADJ[9]	SDP_DE_H_END_ADJ[8]
0x9B	0x00	DE_HORIZONTAL_END_2	rw	SDP_DE_H_END_ADJ[7]	SDP_DE_H_END_ADJ[6]	SDP_DE_H_END_ADJ[5]	SDP_DE_H_END_ADJ[4]	SDP_DE_H_END_ADJ[3]	SDP_DE_H_END_ADJ[2]	SDP_DE_H_END_ADJ[1]	SDP_DE_H_END_ADJ[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9C	0x00	VSYNC_FIELD_HORIZONTAL_BEGIN_1	rw	-	-	-	-	SDP_VSF_H_BEG_ADJ[11]	SDP_VSF_H_BEG_ADJ[10]	SDP_VSF_H_BEG_ADJ[9]	SDP_VSF_H_BEG_ADJ[8]
0x9D	0x00	VSYNC_FIELD_HORIZONTAL_BEGIN_2	rw	SDP_VSF_H_BEG_ADJ[7]	SDP_VSF_H_BEG_ADJ[6]	SDP_VSF_H_BEG_ADJ[5]	SDP_VSF_H_BEG_ADJ[4]	SDP_VSF_H_BEG_ADJ[3]	SDP_VSF_H_BEG_ADJ[2]	SDP_VSF_H_BEG_ADJ[1]	SDP_VSF_H_BEG_ADJ[0]
0x9E	0x00	VSYNC_FIELD_HORIZONTAL_BEGIN_3	rw	-	-	-	-	SDP_VSF_H_MID_ADJ[11]	SDP_VSF_H_MID_ADJ[10]	SDP_VSF_H_MID_ADJ[9]	SDP_VSF_H_MID_ADJ[8]
0x9F	0x00	VSYNC_FIELD_HORIZONTAL_BEGIN_4	rw	SDP_VSF_H_MID_ADJ[7]	SDP_VSF_H_MID_ADJ[6]	SDP_VSF_H_MID_ADJ[5]	SDP_VSF_H_MID_ADJ[4]	SDP_VSF_H_MID_ADJ[3]	SDP_VSF_H_MID_ADJ[2]	SDP_VSF_H_MID_ADJ[1]	SDP_VSF_H_MID_ADJ[0]
0xA0	0x04	V_BIT_BEGIN_ODD	rw	-	-	SDP_V_BEG_O_ADJ[5]	SDP_V_BEG_O_ADJ[4]	SDP_V_BEG_O_ADJ[3]	SDP_V_BEG_O_ADJ[2]	SDP_V_BEG_O_ADJ[1]	SDP_V_BEG_O_ADJ[0]
0xA1	0x04	V_BIT_BEGIN_EVEN	rw	-	-	SDP_V_BEG_E_ADJ[5]	SDP_V_BEG_E_ADJ[4]	SDP_V_BEG_E_ADJ[3]	SDP_V_BEG_E_ADJ[2]	SDP_V_BEG_E_ADJ[1]	SDP_V_BEG_E_ADJ[0]
0xA2	0x04	V_BIT_END_ODD	rw	-	-	SDP_V_END_O_ADJ[5]	SDP_V_END_O_ADJ[4]	SDP_V_END_O_ADJ[3]	SDP_V_END_O_ADJ[2]	SDP_V_END_O_ADJ[1]	SDP_V_END_O_ADJ[0]
0xA3	0x04	V_BIT_END_EVEN	rw	-	-	SDP_V_END_E_ADJ[5]	SDP_V_END_E_ADJ[4]	SDP_V_END_E_ADJ[3]	SDP_V_END_E_ADJ[2]	SDP_V_END_E_ADJ[1]	SDP_V_END_E_ADJ[0]
0xA4	0x04	F_BIT_TOGGLE_ODD	rw	-	-	SDP_F_TOG_O_ADJ[5]	SDP_F_TOG_O_ADJ[4]	SDP_F_TOG_O_ADJ[3]	SDP_F_TOG_O_ADJ[2]	SDP_F_TOG_O_ADJ[1]	SDP_F_TOG_O_ADJ[0]
0xA5	0x04	F_BIT_TOGGLE_EVEN	rw	-	-	SDP_F_TOG_E_ADJ[5]	SDP_F_TOG_E_ADJ[4]	SDP_F_TOG_E_ADJ[3]	SDP_F_TOG_E_ADJ[2]	SDP_F_TOG_E_ADJ[1]	SDP_F_TOG_E_ADJ[0]
0xA6	0x04	FIELD_TOGGLE_ODD	rw	-	-	SDP_FLD_TOG_O_ADJ[5]	SDP_FLD_TOG_O_ADJ[4]	SDP_FLD_TOG_O_ADJ[3]	SDP_FLD_TOG_O_ADJ[2]	SDP_FLD_TOG_O_ADJ[1]	SDP_FLD_TOG_O_ADJ[0]
0xA7	0x04	FIELD_TOGGLE_EVEN	rw	-	-	SDP_FLD_TOG_E_ADJ[5]	SDP_FLD_TOG_E_ADJ[4]	SDP_FLD_TOG_E_ADJ[3]	SDP_FLD_TOG_E_ADJ[2]	SDP_FLD_TOG_E_ADJ[1]	SDP_FLD_TOG_E_ADJ[0]
0xA8	0x04	VSYNC_VERTICAL_BEGIN_ODD	rw	-	-	SDP_VS_V_BEG_O_ADJ[5]	SDP_VS_V_BEG_O_ADJ[4]	SDP_VS_V_BEG_O_ADJ[3]	SDP_VS_V_BEG_O_ADJ[2]	SDP_VS_V_BEG_O_ADJ[1]	SDP_VS_V_BEG_O_ADJ[0]
0xA9	0x04	VSYNC_VERTICAL_BEGIN_EVEN	rw	-	-	SDP_VS_V_BEG_E_ADJ[5]	SDP_VS_V_BEG_E_ADJ[4]	SDP_VS_V_BEG_E_ADJ[3]	SDP_VS_V_BEG_E_ADJ[2]	SDP_VS_V_BEG_E_ADJ[1]	SDP_VS_V_BEG_E_ADJ[0]
0xAA	0x04	VSYNC_VERTICAL_END_ODD	rw	-	-	SDP_VS_V_END_O_ADJ[5]	SDP_VS_V_END_O_ADJ[4]	SDP_VS_V_END_O_ADJ[3]	SDP_VS_V_END_O_ADJ[2]	SDP_VS_V_END_O_ADJ[1]	SDP_VS_V_END_O_ADJ[0]
0xAB	0x04	VSYNC_VERTICAL_END_EVEN	rw	-	-	SDP_VS_V_END_E_ADJ[5]	SDP_VS_V_END_E_ADJ[4]	SDP_VS_V_END_E_ADJ[3]	SDP_VS_V_END_E_ADJ[2]	SDP_VS_V_END_E_ADJ[1]	SDP_VS_V_END_E_ADJ[0]
0xAC	0x04	DE_VERTICAL_BEGIN_ODD	rw	-	-	SDP_DE_V_BEG_O_ADJ[5]	SDP_DE_V_BEG_O_ADJ[4]	SDP_DE_V_BEG_O_ADJ[3]	SDP_DE_V_BEG_O_ADJ[2]	SDP_DE_V_BEG_O_ADJ[1]	SDP_DE_V_BEG_O_ADJ[0]
0xAD	0x04	DE_VERTICAL_BEGIN_EVEN	rw	-	-	SDP_DE_V_BEG_E_ADJ[5]	SDP_DE_V_BEG_E_ADJ[4]	SDP_DE_V_BEG_E_ADJ[3]	SDP_DE_V_BEG_E_ADJ[2]	SDP_DE_V_BEG_E_ADJ[1]	SDP_DE_V_BEG_E_ADJ[0]
0xAE	0x04	DE_VERTICAL_END_ODD	rw	-	-	SDP_DE_V_END_O_ADJ[5]	SDP_DE_V_END_O_ADJ[4]	SDP_DE_V_END_O_ADJ[3]	SDP_DE_V_END_O_ADJ[2]	SDP_DE_V_END_O_ADJ[1]	SDP_DE_V_END_O_ADJ[0]
0xAF	0x04	DE_VERTICAL_END_EVEN	rw	-	-	SDP_DE_V_END_E_ADJ[5]	SDP_DE_V_END_E_ADJ[4]	SDP_DE_V_END_E_ADJ[3]	SDP_DE_V_END_E_ADJ[2]	SDP_DE_V_END_E_ADJ[1]	SDP_DE_V_END_E_ADJ[0]
0xB0	0xC0	BLANKING_CONTROL	rw	SDP_VBLANK_EN	SDP_HBLANK_EN	SDP_FHE_TOG_INV	SDP_FHO_TOG_INV	SDP_VHE_END_INV	SDP_VHO_END_INV	SDP_VHE_BEG_INV	SDP_VHO_BEG_INV
0xB1	0x7D	POLARITY	rw	-	SDP_V_BIT_POL	SDP_F_BIT_POL	SDP_DE_POL	SDP_CS_POL	SDP_FLD_POL	SDP_VS_POL	SDP_HS_POL

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB2	0x6C	SAV_EAV_CONTROLS	rw	-	-	-	-	SDP_EAV_EN	SDP_SAV_EN	SDP_FRZ_F_BIT	-
0xB3	0x20	ANCILLARY_DATA_BEGIN	rw	SDP_REPL_ANC_DATA	SDP_SPLIT_ANC_DATA	SDP_SPLIT_AV_CODE	-	-	-	-	-
0xB4	0x04	V_BIT_BEGIN_ODD_TM	rw	-	-	SDP_V_BEG_TRICK_O_ADJ[5]	SDP_V_BEG_TRICK_O_ADJ[4]	SDP_V_BEG_TRICK_O_ADJ[3]	SDP_V_BEG_TRICK_O_ADJ[2]	SDP_V_BEG_TRICK_O_ADJ[1]	SDP_V_BEG_TRICK_O_ADJ[0]
0xB5	0x04	V_BIT_BEGIN_EVEN_TM	rw	-	-	SDP_V_BEG_TRICK_E_ADJ[5]	SDP_V_BEG_TRICK_E_ADJ[4]	SDP_V_BEG_TRICK_E_ADJ[3]	SDP_V_BEG_TRICK_E_ADJ[2]	SDP_V_BEG_TRICK_E_ADJ[1]	SDP_V_BEG_TRICK_E_ADJ[0]
0xB6	0x04	V_BIT_END_ODD_TM	rw	-	-	SDP_V_END_TRICK_O_ADJ[5]	SDP_V_END_TRICK_O_ADJ[4]	SDP_V_END_TRICK_O_ADJ[3]	SDP_V_END_TRICK_O_ADJ[2]	SDP_V_END_TRICK_O_ADJ[1]	SDP_V_END_TRICK_O_ADJ[0]
0xB7	0x04	V_BIT_END_EVEN_TM	rw	-	-	SDP_V_END_TRICK_E_ADJ[5]	SDP_V_END_TRICK_E_ADJ[4]	SDP_V_END_TRICK_E_ADJ[3]	SDP_V_END_TRICK_E_ADJ[2]	SDP_V_END_TRICK_E_ADJ[1]	SDP_V_END_TRICK_E_ADJ[0]
0xB8	0x04	F_BIT_TOGGLE_ODD_TM	rw	-	-	SDP_F_TOG_TRICK_O_ADJ[5]	SDP_F_TOG_TRICK_O_ADJ[4]	SDP_F_TOG_TRICK_O_ADJ[3]	SDP_F_TOG_TRICK_O_ADJ[2]	SDP_F_TOG_TRICK_O_ADJ[1]	SDP_F_TOG_TRICK_O_ADJ[0]
0xB9	0x04	F_BIT_TOGGLE_EVEN_TM	rw	-	-	SDP_F_TOG_TRICK_E_ADJ[5]	SDP_F_TOG_TRICK_E_ADJ[4]	SDP_F_TOG_TRICK_E_ADJ[3]	SDP_F_TOG_TRICK_E_ADJ[2]	SDP_F_TOG_TRICK_E_ADJ[1]	SDP_F_TOG_TRICK_E_ADJ[0]
0xC2	0x04	AUX_V_BIT_BEGIN_ODD	rw	-	-	SDP_AUX_V_BEG_O_ADJ[5]	SDP_AUX_V_BEG_O_ADJ[4]	SDP_AUX_V_BEG_O_ADJ[3]	SDP_AUX_V_BEG_O_ADJ[2]	SDP_AUX_V_BEG_O_ADJ[1]	SDP_AUX_V_BEG_O_ADJ[0]
0xC3	0x04	AUX_V_BIT_BEGIN_EVEN	rw	-	-	SDP_AUX_V_BEG_E_ADJ[5]	SDP_AUX_V_BEG_E_ADJ[4]	SDP_AUX_V_BEG_E_ADJ[3]	SDP_AUX_V_BEG_E_ADJ[2]	SDP_AUX_V_BEG_E_ADJ[1]	SDP_AUX_V_BEG_E_ADJ[0]
0xC4	0x04	AUX_V_BIT_END_ODD	rw	-	-	SDP_AUX_V_END_O_ADJ[5]	SDP_AUX_V_END_O_ADJ[4]	SDP_AUX_V_END_O_ADJ[3]	SDP_AUX_V_END_O_ADJ[2]	SDP_AUX_V_END_O_ADJ[1]	SDP_AUX_V_END_O_ADJ[0]
0xC5	0x04	AUX_V_BIT_END_EVEN	rw	-	-	SDP_AUX_V_END_E_ADJ[5]	SDP_AUX_V_END_E_ADJ[4]	SDP_AUX_V_END_E_ADJ[3]	SDP_AUX_V_END_E_ADJ[2]	SDP_AUX_V_END_E_ADJ[1]	SDP_AUX_V_END_E_ADJ[0]
0xC6	0x04	AUX_F_BIT_TOGGLE_ODD	rw	-	-	SDP_AUX_F_TOG_O_ADJ[5]	SDP_AUX_F_TOG_O_ADJ[4]	SDP_AUX_F_TOG_O_ADJ[3]	SDP_AUX_F_TOG_O_ADJ[2]	SDP_AUX_F_TOG_O_ADJ[1]	SDP_AUX_F_TOG_O_ADJ[0]
0xC7	0x04	AUX_F_BIT_TOGGLE_EVEN	rw	-	-	SDP_AUX_F_TOG_E_ADJ[5]	SDP_AUX_F_TOG_E_ADJ[4]	SDP_AUX_F_TOG_E_ADJ[3]	SDP_AUX_F_TOG_E_ADJ[2]	SDP_AUX_F_TOG_E_ADJ[1]	SDP_AUX_F_TOG_E_ADJ[0]
0xC8	0xEB	AUX_SAV_EAV_CONTROLS_1	rw	-	SDP_AUX_V_BIT_POL	SDP_AUX_F_BIT_POL	-	SDP_ANC_MAIN_EN	SDP_ANC_AUX_EN	SDP_AUX_VBLANK_EN	SDP_AUX_HBLANK_EN
0xC9	0x6C	AUX_SAV_EAV_CONTROLS_2	rw	-	-	-	SDP_AUX_REPL_AV_CODE	SDP_AUX_EAV_EN	SDP_AUX_SAV_EN	-	-
0xE0	0x47	SDP_CSC_A1_1	rw	SDP_CSC_SCALE	SDP_CSC_AUTO	SDP_RET_VID_ADJ	SDP_A1[12]	SDP_A1[11]	SDP_A1[10]	SDP_A1[9]	SDP_A1[8]
0xE1	0xD2	SDP_CSC_A1_2	rw	SDP_A1[7]	SDP_A1[6]	SDP_A1[5]	SDP_A1[4]	SDP_A1[3]	SDP_A1[2]	SDP_A1[1]	SDP_A1[0]
0xE2	0x00	SDP_CSC_A2_1	rw	-	-	-	SDP_A2[12]	SDP_A2[11]	SDP_A2[10]	SDP_A2[9]	SDP_A2[8]
0xE3	0x00	SDP_CSC_A2_2	rw	SDP_A2[7]	SDP_A2[6]	SDP_A2[5]	SDP_A2[4]	SDP_A2[3]	SDP_A2[2]	SDP_A2[1]	SDP_A2[0]
0xE4	0x00	SDP_CSC_A3_1	rw	-	-	-	SDP_A3[12]	SDP_A3[11]	SDP_A3[10]	SDP_A3[9]	SDP_A3[8]
0xE5	0x40	SDP_CSC_A3_2	rw	SDP_A3[7]	SDP_A3[6]	SDP_A3[5]	SDP_A3[4]	SDP_A3[3]	SDP_A3[2]	SDP_A3[1]	SDP_A3[0]
0xE6	0x7F	SDP_CSC_A4_1	rw	-	SDP_A4[14]	SDP_A4[13]	SDP_A4[12]	SDP_A4[11]	SDP_A4[10]	SDP_A4[9]	SDP_A4[8]
0xE7	0x00	SDP_CSC_A4_2	rw	SDP_A4[7]	SDP_A4[6]	SDP_A4[5]	SDP_A4[4]	SDP_A4[3]	SDP_A4[2]	SDP_A4[1]	SDP_A4[0]
0xE8	0x00	SDP_CSC_B1_1	rw	-	-	-	SDP_B1[12]	SDP_B1[11]	SDP_B1[10]	SDP_B1[9]	SDP_B1[8]
0xE9	0x00	SDP_CSC_B1_2	rw	SDP_B1[7]	SDP_B1[6]	SDP_B1[5]	SDP_B1[4]	SDP_B1[3]	SDP_B1[2]	SDP_B1[1]	SDP_B1[0]
0xEA	0x09	SDP_CSC_B2_1	rw	-	-	-	SDP_B2[12]	SDP_B2[11]	SDP_B2[10]	SDP_B2[9]	SDP_B2[8]
0xEB	0x26	SDP_CSC_B2_2	rw	SDP_B2[7]	SDP_B2[6]	SDP_B2[5]	SDP_B2[4]	SDP_B2[3]	SDP_B2[2]	SDP_B2[1]	SDP_B2[0]
0xEC	0x00	SDP_CSC_B3_1	rw	-	-	-	SDP_B3[12]	SDP_B3[11]	SDP_B3[10]	SDP_B3[9]	SDP_B3[8]
0xED	0x00	SDP_CSC_B3_2	rw	SDP_B3[7]	SDP_B3[6]	SDP_B3[5]	SDP_B3[4]	SDP_B3[3]	SDP_B3[2]	SDP_B3[1]	SDP_B3[0]
0xEE	0x00	SDP_CSC_B4_1	rw	-	SDP_B4[14]	SDP_B4[13]	SDP_B4[12]	SDP_B4[11]	SDP_B4[10]	SDP_B4[9]	SDP_B4[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xEF	0x00	SDP_CSC_B4_2	rw	SDP_B4[7]	SDP_B4[6]	SDP_B4[5]	SDP_B4[4]	SDP_B4[3]	SDP_B4[2]	SDP_B4[1]	SDP_B4[0]
0xF0	0x00	SDP_CSC_C1_1	rw	-	-	-	SDP_C1[12]	SDP_C1[11]	SDP_C1[10]	SDP_C1[9]	SDP_C1[8]
0xF1	0x00	SDP_CSC_C1_2	rw	SDP_C1[7]	SDP_C1[6]	SDP_C1[5]	SDP_C1[4]	SDP_C1[3]	SDP_C1[2]	SDP_C1[1]	SDP_C1[0]
0xF2	0x00	SDP_CSC_C2_1	rw	-	-	-	SDP_C2[12]	SDP_C2[11]	SDP_C2[10]	SDP_C2[9]	SDP_C2[8]
0xF3	0x00	SDP_CSC_C2_2	rw	SDP_C2[7]	SDP_C2[6]	SDP_C2[5]	SDP_C2[4]	SDP_C2[3]	SDP_C2[2]	SDP_C2[1]	SDP_C2[0]
0xF4	0x06	SDP_CSC_C3_1	rw	-	-	-	SDP_C3[12]	SDP_C3[11]	SDP_C3[10]	SDP_C3[9]	SDP_C3[8]
0xF5	0x81	SDP_CSC_C3_2	rw	SDP_C3[7]	SDP_C3[6]	SDP_C3[5]	SDP_C3[4]	SDP_C3[3]	SDP_C3[2]	SDP_C3[1]	SDP_C3[0]
0xF6	0x00	SDP_CSC_C4_1	rw	-	SDP_C4[14]	SDP_C4[13]	SDP_C4[12]	SDP_C4[11]	SDP_C4[10]	SDP_C4[9]	SDP_C4[8]
0xF7	0x00	SDP_CSC_C4_2	rw	SDP_C4[7]	SDP_C4[6]	SDP_C4[5]	SDP_C4[4]	SDP_C4[3]	SDP_C4[2]	SDP_C4[1]	SDP_C4[0]

1.9 HDMI MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	HDMI_REGISTER_00H	rw	-	-	EN_BG_PORT_A	EN_BG_PORT_B	BG_MEAS_PORT_SEL[1]	BG_MEAS_PORT_SEL[0]	HDMI_PORT_SELECT[1]	HDMI_PORT_SELECT[0]
0x01	0x78	HDMI_REGISTER_01H	rw	TERM_AUTO	CLOCK_TERMB_DISABLE	CLOCK_TERMA_DISABLE	-	-	HDCP_ONLY_MODE	OVR_MUX_HBR	MUX_HBR_OUT
0x02	0x00	HDMI_REGISTER_02H	rw	-	-	-	-	-	-	OVR_MUX_DSD_OUT	MUX_DSD_OUT
0x03	0x18	HDMI REGISTER_03H	rw	-	I2SOUTMODE[1]	I2SOUTMODE[0]	I2SBITWIDTH[4]	I2SBITWIDTH[3]	I2SBITWIDTH[2]	I2SBITWIDTH[1]	I2SBITWIDTH[0]
0x04	0x00	HDMI REGISTER_04H	r	-	AV_MUTE	HDCP_KEYS_READ	HDCP_KEY_ERROR	-	-	TMDS_PLL_LOCKED	AUDIO_PLL_LOCKED
0x05	0x00	HDMI_REGISTER_05H	r	HDMI_MODE	HDMI_CONTENT_ENCRYPTED	DVI_HSYNC_POLARITY	DVI_VSYNC_POLARITY	HDMI_PIXEL_REPETITION[3]	HDMI_PIXEL_REPETITION[2]	HDMI_PIXEL_REPETITION[1]	HDMI_PIXEL_REPETITION[0]
0x07	0x00	LINE WIDTH_1	r	VERT_FILTER_LOCKED	AUDIO_CHANNEL_MODE	DE_REGEN_FILTER_LOCKED	LINE_WIDTH[12]	LINE_WIDTH[11]	LINE_WIDTH[10]	LINE_WIDTH[9]	LINE_WIDTH[8]
0x08	0x00	LINE WIDTH_2	r	LINE_WIDTH[7]	LINE_WIDTH[6]	LINE_WIDTH[5]	LINE_WIDTH[4]	LINE_WIDTH[3]	LINE_WIDTH[2]	LINE_WIDTH[1]	LINE_WIDTH[0]
0x09	0x00	FIELD0 HEIGHT_1	r	-	-	-	FIELD0_HEIGHT[12]	FIELD0_HEIGHT[11]	FIELD0_HEIGHT[10]	FIELD0_HEIGHT[9]	FIELD0_HEIGHT[8]
0x0A	0x00	FIELD0 HEIGHT_2	r	FIELD0_HEIGHT[7]	FIELD0_HEIGHT[6]	FIELD0_HEIGHT[5]	FIELD0_HEIGHT[4]	FIELD0_HEIGHT[3]	FIELD0_HEIGHT[2]	FIELD0_HEIGHT[1]	FIELD0_HEIGHT[0]
0x0B	0x00	FIELD1 HEIGHT_1	r	DEEP_COLOR_MODE[1]	DEEP_COLOR_MODE[0]	HDMI_INTERLACED	FIELD1_HEIGHT[12]	FIELD1_HEIGHT[11]	FIELD1_HEIGHT[10]	FIELD1_HEIGHT[9]	FIELD1_HEIGHT[8]
0x0C	0x00	FIELD1 HEIGHT_2	r	FIELD1_HEIGHT[7]	FIELD1_HEIGHT[6]	FIELD1_HEIGHT[5]	FIELD1_HEIGHT[4]	FIELD1_HEIGHT[3]	FIELD1_HEIGHT[2]	FIELD1_HEIGHT[1]	FIELD1_HEIGHT[0]
0x0D	0x04	HDMI_REGISTER_0DH	rw	-	-	-	-	FREQTOLERANCE[3]	FREQTOLERANCE[2]	FREQTOLERANCE[1]	FREQTOLERANCE[0]
0x0F	0x1F	AUDIO MUTE SPEED	rw	MAN_AUDIO_DL_BYPASS	AUDIO_DELAY_LINE_BYPASS	-	AUDIO_MUTE_SPEED[4]	AUDIO_MUTE_SPEED[3]	AUDIO_MUTE_SPEED[2]	AUDIO_MUTE_SPEED[1]	AUDIO_MUTE_SPEED[0]
0x10	0x25	HDMI_REGISTER_10H	rw	-	-	CTS_CHANGE_THRESHOLD[5]	CTS_CHANGE_THRESHOLD[4]	CTS_CHANGE_THRESHOLD[3]	CTS_CHANGE_THRESHOLD[2]	CTS_CHANGE_THRESHOLD[1]	CTS_CHANGE_THRESHOLD[0]
0x11	0x7D	AUDIO FIFO ALMOST FULL THRESHOLD	rw	-	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[5]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[4]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[3]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[2]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[1]	AUDIO_FIFO_ALMOST_FULL_THRESHOLD[0]
0x12	0x02	AUDIO FIFO ALMOST EMPTY THRESHOLD	rw	-	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[5]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[4]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[3]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[2]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[1]	AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[0]
0x13	0x7F	AUDIO COAST MASK	rw	-	AC_MSK_VCLK_CHNG	AC_MSK_VPLL_UNLOCK	-	AC_MSK_NEW_CTS	AC_MSK_NEW_N	AC_MSK_CHNG_PORT	AC_MSK_VCLK_DET
0x14	0x3F	MUTE MASK 21_16	rw	-	-	MT_MSK_COMPRS_AUD	MT_MSK_AUD_MODE_CHNG	-	-	MT_MSK_PARITY_ERR	MT_MSK_VCLK_CHNG
0x15	0xFF	MUTE MASK 15_8	rw	MT_MSK_APLL_UNLOCK	MT_MSK_VPLL_UNLOCK	MT_MSK_ACR_NOT_DET	-	MT_MSK_FLATLINE_DET	-	MT_MSK_FIFO_UNDERLFOW	MT_MSK_FIFO_OVERFLOW
0x16	0xFF	MUTE MASK 7_0	rw	MT_MSK_AVMUTE	MT_MSK_NOT_HDMIMODE	MT_MSK_NEW_CTS	MT_MSK_NEW_N	MT_MSK_CHMODE_CHNG	MT_MSK_APCKT_ECC_ERR	MT_MSK_CHNG_PORT	MT_MSK_VCLK_DET
0x18	0x00	PACKETS DETECTED_2	r	-	-	-	-	HBR_AUDIO_PCKT_DET	-	DSD_PACKET_DET	AUDIO_SAMPLE_PCKT_DET
0x1A	0x80	MUTE_CTRL	rw	-	IGNORE_PARITY_ERR	-	MUTE_AUDIO	WAIT_UNMUTE[2]	WAIT_UNMUTE[1]	WAIT_UNMUTE[0]	NOT_AUTO_UNMUTE

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x1B	0x18	DEEPCOLOR_FIFO_DEBUG_1	rw	-	-	-	DCFIFO_RESET_ON_LOCK	DCFIFO_KILL_NOT_LOCKED	DCFIFO_KILL_DIS	-	-
0x1C	0x00	DEEPCOLOR_FIFO_DEBUG_2	r	-	-	-	-	DCFIFO_LOCKED	DCFIFO_LEVEL[2]	DCFIFO_LEVEL[1]	DCFIFO_LEVEL[0]
0x1D	0x00	REGISTER_1DH	rw	-	-	UP_CONVERSION_MODE	-	-	-	-	-
0x1E	0x00	TOTAL_LINE_WIDTH_1	r	-	-	TOTAL_LINE_WIDTH[13]	TOTAL_LINE_WIDTH[12]	TOTAL_LINE_WIDTH[11]	TOTAL_LINE_WIDTH[10]	TOTAL_LINE_WIDTH[9]	TOTAL_LINE_WIDTH[8]
0x1F	0x00	TOTAL_LINE_WIDTH_2	r	TOTAL_LINE_WIDTH[7]	TOTAL_LINE_WIDTH[6]	TOTAL_LINE_WIDTH[5]	TOTAL_LINE_WIDTH[4]	TOTAL_LINE_WIDTH[3]	TOTAL_LINE_WIDTH[2]	TOTAL_LINE_WIDTH[1]	TOTAL_LINE_WIDTH[0]
0x20	0x00	HSYNC_FRONT_PORCH_1	r	-	-	-	HSYNC_FRONT_PORCH[12]	HSYNC_FRONT_PORCH[11]	HSYNC_FRONT_PORCH[10]	HSYNC_FRONT_PORCH[9]	HSYNC_FRONT_PORCH[8]
0x21	0x00	HSYNC_FRONT_PORCH_2	r	HSYNC_FRONT_PORCH[7]	HSYNC_FRONT_PORCH[6]	HSYNC_FRONT_PORCH[5]	HSYNC_FRONT_PORCH[4]	HSYNC_FRONT_PORCH[3]	HSYNC_FRONT_PORCH[2]	HSYNC_FRONT_PORCH[1]	HSYNC_FRONT_PORCH[0]
0x22	0x00	HSYNC_PULSE_WIDTH_1	r	-	-	-	HSYNC_PULSE_WIDTH[12]	HSYNC_PULSE_WIDTH[11]	HSYNC_PULSE_WIDTH[10]	HSYNC_PULSE_WIDTH[9]	HSYNC_PULSE_WIDTH[8]
0x23	0x00	HSYNC_PULSE_WIDTH_2	r	HSYNC_PULSE_WIDTH[7]	HSYNC_PULSE_WIDTH[6]	HSYNC_PULSE_WIDTH[5]	HSYNC_PULSE_WIDTH[4]	HSYNC_PULSE_WIDTH[3]	HSYNC_PULSE_WIDTH[2]	HSYNC_PULSE_WIDTH[1]	HSYNC_PULSE_WIDTH[0]
0x24	0x00	HSYNC_BACK_PORCH_1	r	-	-	-	HSYNC_BACK_PORCH[12]	HSYNC_BACK_PORCH[11]	HSYNC_BACK_PORCH[10]	HSYNC_BACK_PORCH[9]	HSYNC_BACK_PORCH[8]
0x25	0x00	HSYNC_BACK_PORCH_2	r	HSYNC_BACK_PORCH[7]	HSYNC_BACK_PORCH[6]	HSYNC_BACK_PORCH[5]	HSYNC_BACK_PORCH[4]	HSYNC_BACK_PORCH[3]	HSYNC_BACK_PORCH[2]	HSYNC_BACK_PORCH[1]	HSYNC_BACK_PORCH[0]
0x26	0x00	FIELD0_TOTAL_HEIGHT_1	r	-	-	FIELD0_TOTAL_HEIGHT[13]	FIELD0_TOTAL_HEIGHT[12]	FIELD0_TOTAL_HEIGHT[11]	FIELD0_TOTAL_HEIGHT[10]	FIELD0_TOTAL_HEIGHT[9]	FIELD0_TOTAL_HEIGHT[8]
0x27	0x00	FIELD0_TOTAL_HEIGHT_2	r	FIELD0_TOTAL_HEIGHT[7]	FIELD0_TOTAL_HEIGHT[6]	FIELD0_TOTAL_HEIGHT[5]	FIELD0_TOTAL_HEIGHT[4]	FIELD0_TOTAL_HEIGHT[3]	FIELD0_TOTAL_HEIGHT[2]	FIELD0_TOTAL_HEIGHT[1]	FIELD0_TOTAL_HEIGHT[0]
0x28	0x00	FIELD1_TOTAL_HEIGHT_1	r	-	-	FIELD1_TOTAL_HEIGHT[13]	FIELD1_TOTAL_HEIGHT[12]	FIELD1_TOTAL_HEIGHT[11]	FIELD1_TOTAL_HEIGHT[10]	FIELD1_TOTAL_HEIGHT[9]	FIELD1_TOTAL_HEIGHT[8]
0x29	0x00	FIELD1_TOTAL_HEIGHT_2	r	FIELD1_TOTAL_HEIGHT[7]	FIELD1_TOTAL_HEIGHT[6]	FIELD1_TOTAL_HEIGHT[5]	FIELD1_TOTAL_HEIGHT[4]	FIELD1_TOTAL_HEIGHT[3]	FIELD1_TOTAL_HEIGHT[2]	FIELD1_TOTAL_HEIGHT[1]	FIELD1_TOTAL_HEIGHT[0]
0x2A	0x00	FIELD0_VS_FRONT_PORCH_1	r	-	-	FIELD0_VS_FRONT_PORCH[13]	FIELD0_VS_FRONT_PORCH[12]	FIELD0_VS_FRONT_PORCH[11]	FIELD0_VS_FRONT_PORCH[10]	FIELD0_VS_FRONT_PORCH[9]	FIELD0_VS_FRONT_PORCH[8]
0x2B	0x00	FIELD0_VS_FRONT_PORCH_2	r	FIELD0_VS_FRONT_PORCH[7]	FIELD0_VS_FRONT_PORCH[6]	FIELD0_VS_FRONT_PORCH[5]	FIELD0_VS_FRONT_PORCH[4]	FIELD0_VS_FRONT_PORCH[3]	FIELD0_VS_FRONT_PORCH[2]	FIELD0_VS_FRONT_PORCH[1]	FIELD0_VS_FRONT_PORCH[0]
0x2C	0x00	FIELD1_VS_FRONT_PORCH_1	r	-	-	FIELD1_VS_FRONT_PORCH[13]	FIELD1_VS_FRONT_PORCH[12]	FIELD1_VS_FRONT_PORCH[11]	FIELD1_VS_FRONT_PORCH[10]	FIELD1_VS_FRONT_PORCH[9]	FIELD1_VS_FRONT_PORCH[8]
0x2D	0x00	FIELD1_VS_FRONT_PORCH_2	r	FIELD1_VS_FRONT_PORCH[7]	FIELD1_VS_FRONT_PORCH[6]	FIELD1_VS_FRONT_PORCH[5]	FIELD1_VS_FRONT_PORCH[4]	FIELD1_VS_FRONT_PORCH[3]	FIELD1_VS_FRONT_PORCH[2]	FIELD1_VS_FRONT_PORCH[1]	FIELD1_VS_FRONT_PORCH[0]
0x2E	0x00	FIELD0_VS_PULSE_WIDTH_1	r	-	-	FIELD0_VS_PULSE_WIDTH[13]	FIELD0_VS_PULSE_WIDTH[12]	FIELD0_VS_PULSE_WIDTH[11]	FIELD0_VS_PULSE_WIDTH[10]	FIELD0_VS_PULSE_WIDTH[9]	FIELD0_VS_PULSE_WIDTH[8]
0x2F	0x00	FIELD0_VS_PULSE_WIDTH_2	r	FIELD0_VS_PULSE_WIDTH[7]	FIELD0_VS_PULSE_WIDTH[6]	FIELD0_VS_PULSE_WIDTH[5]	FIELD0_VS_PULSE_WIDTH[4]	FIELD0_VS_PULSE_WIDTH[3]	FIELD0_VS_PULSE_WIDTH[2]	FIELD0_VS_PULSE_WIDTH[1]	FIELD0_VS_PULSE_WIDTH[0]
0x30	0x00	FIELD1_VS_PULSE_WIDTH_1	r	-	-	FIELD1_VS_PULSE_WIDTH[13]	FIELD1_VS_PULSE_WIDTH[12]	FIELD1_VS_PULSE_WIDTH[11]	FIELD1_VS_PULSE_WIDTH[10]	FIELD1_VS_PULSE_WIDTH[9]	FIELD1_VS_PULSE_WIDTH[8]
0x31	0x00	FIELD1_VS_PULSE_WIDTH_2	r	FIELD1_VS_PULSE_WIDTH[7]	FIELD1_VS_PULSE_WIDTH[6]	FIELD1_VS_PULSE_WIDTH[5]	FIELD1_VS_PULSE_WIDTH[4]	FIELD1_VS_PULSE_WIDTH[3]	FIELD1_VS_PULSE_WIDTH[2]	FIELD1_VS_PULSE_WIDTH[1]	FIELD1_VS_PULSE_WIDTH[0]
0x32	0x00	FIELD0_VS_BACK_PORCH_1	r	-	-	FIELD0_VS_BACK_PORCH[13]	FIELD0_VS_BACK_PORCH[12]	FIELD0_VS_BACK_PORCH[11]	FIELD0_VS_BACK_PORCH[10]	FIELD0_VS_BACK_PORCH[9]	FIELD0_VS_BACK_PORCH[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x33	0x00	FIELD0_VS_BACK_PORCH_2	r	FIELD0_VS_BACK_PORCH[7]	FIELD0_VS_BACK_PORCH[6]	FIELD0_VS_BACK_PORCH[5]	FIELD0_VS_BACK_PORCH[4]	FIELD0_VS_BACK_PORCH[3]	FIELD0_VS_BACK_PORCH[2]	FIELD0_VS_BACK_PORCH[1]	FIELD0_VS_BACK_PORCH[0]
0x34	0x00	FIELD1_VS_BACK_PORCH_1	r	-	-	FIELD1_VS_BACK_PORCH[13]	FIELD1_VS_BACK_PORCH[12]	FIELD1_VS_BACK_PORCH[11]	FIELD1_VS_BACK_PORCH[10]	FIELD1_VS_BACK_PORCH[9]	FIELD1_VS_BACK_PORCH[8]
0x35	0x00	FIELD1_VS_BACK_PORCH_2	r	FIELD1_VS_BACK_PORCH[7]	FIELD1_VS_BACK_PORCH[6]	FIELD1_VS_BACK_PORCH[5]	FIELD1_VS_BACK_PORCH[4]	FIELD1_VS_BACK_PORCH[3]	FIELD1_VS_BACK_PORCH[2]	FIELD1_VS_BACK_PORCH[1]	FIELD1_VS_BACK_PORCH[0]
0x36	0x00	CHANNEL STATUS DATA_1	r	CS_DATA[7]	CS_DATA[6]	CS_DATA[5]	CS_DATA[4]	CS_DATA[3]	CS_DATA[2]	CS_DATA[1]	CS_DATA[0]
0x37	0x00	CHANNEL STATUS DATA_2	r	CS_DATA[15]	CS_DATA[14]	CS_DATA[13]	CS_DATA[12]	CS_DATA[11]	CS_DATA[10]	CS_DATA[9]	CS_DATA[8]
0x38	0x00	CHANNEL STATUS DATA_3	r	CS_DATA[23]	CS_DATA[22]	CS_DATA[21]	CS_DATA[20]	CS_DATA[19]	CS_DATA[18]	CS_DATA[17]	CS_DATA[16]
0x39	0x00	CHANNEL STATUS DATA_4	r	CS_DATA[31]	CS_DATA[30]	CS_DATA[29]	CS_DATA[28]	CS_DATA[27]	CS_DATA[26]	CS_DATA[25]	CS_DATA[24]
0x3A	0x00	CHANNEL STATUS DATA_5	r	CS_DATA[39]	CS_DATA[38]	CS_DATA[37]	CS_DATA[36]	CS_DATA[35]	CS_DATA[34]	CS_DATA[33]	CS_DATA[32]
0x40	0x00	REGISTER_40H	rw	-	OVERRIDE_DEEP_COLOR_MODE	DEEP_COLOR_MODE_USER[1]	DEEP_COLOR_MODE_USER[0]	-	-	-	-
0x41	0x40	REGISTER_41H	rw	-	-	-	DEREP_N_OVERRIDE	DEREP_N[3]	DEREP_N[2]	DEREP_N[1]	DEREP_N[0]
0x47	0x00	REGISTER_47H	rw	-	-	-	-	-	QZERO_ITC_DIS	QZERO_RGB_FULL	ALWAYS_STORE_INF
0x48	0x00	REGISTER_48H	rw	DIS_PWRDNB	DIS_CABLE_DET_RST	-	-	-	-	-	-
0x50	0x00	HDMI_REGISTER_50	rw	-	-	-	GAMUT_IRQ_NEXT_FIELD	-	-	CS_COPYRIGHT_MANUAL	CS_COPYRIGHT_VALUE
0x51	0x00		r	TMDSFREQ[8]	TMDSFREQ[7]	TMDSFREQ[6]	TMDSFREQ[5]	TMDSFREQ[4]	TMDSFREQ[3]	TMDSFREQ[2]	TMDSFREQ[1]
0x52	0x00		r	TMDSFREQ[0]	TMDSFREQ_FRAC[6]	TMDSFREQ_FRAC[5]	TMDSFREQ_FRAC[4]	TMDSFREQ_FRAC[3]	TMDSFREQ_FRAC[2]	TMDSFREQ_FRAC[1]	TMDSFREQ_FRAC[0]
0x53	0x00	HDMI_COLORSPACE	r	-	-	-	-	HDMI_COLORSPACE[3]	HDMI_COLORSPACE[2]	HDMI_COLORSPACE[1]	HDMI_COLORSPACE[0]
0x56	0x58	FILT_5V_DET_REG	rw	FILT_5V_DET_DIS	FILT_5V_DET_TIMER[6]	FILT_5V_DET_TIMER[5]	FILT_5V_DET_TIMER[4]	FILT_5V_DET_TIMER[3]	FILT_5V_DET_TIMER[2]	FILT_5V_DET_TIMER[1]	FILT_5V_DET_TIMER[0]
0x5A	0x00	REGISTER_5A	sc	-	-	BG_MEAS_REQ	-	HDCP_REPT_EDID_RESET	DCFIFO_RECENTER	-	FORCE_N_UPDATE
0x5B	0x00	CTS_N_1	r	CTS[19]	CTS[18]	CTS[17]	CTS[16]	CTS[15]	CTS[14]	CTS[13]	CTS[12]
0x5C	0x00	CTS_N_2	r	CTS[11]	CTS[10]	CTS[9]	CTS[8]	CTS[7]	CTS[6]	CTS[5]	CTS[4]
0x5D	0x00	CTS_N_3	r	CTS[3]	CTS[2]	CTS[1]	CTS[0]	N[19]	N[18]	N[17]	N[16]
0x5E	0x00	CTS_N_4	r	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]
0x5F	0x00	CTS_N_5	r	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]
0x69	0xA2		rw	HPA_DELAY_SEL[3]	HPA_DELAY_SEL[2]	HPA_DELAY_SEL[1]	HPA_DELAY_SEL[0]	HPA_OVR_TERM	HPA_AUTO_INT_EDID[1]	HPA_AUTO_INT_EDID[0]	HPA_MANUAL
0x6A	0x00		rw	-	I2S_SPDIF_MAP_INV	I2S_SPDIF_MAP_ROT[1]	I2S_SPDIF_MAP_ROT[0]	DSD_MAP_INV	DSD_MAP_ROT[2]	DSD_MAP_ROT[1]	DSD_MAP_ROT[0]
0x72	0x04		rw	-	-	-	VGA_PWRDN	-	-	-	-
0x73	0x00	DDC PAD	rw	-	-	-	-	DDC_PDN_B	DDC_PDN_A	-	-
0x8C	0xA3	EQ DYNAMIC FREQ	rw	EQ_DYN_FREQ2[3]	EQ_DYN_FREQ2[2]	EQ_DYN_FREQ2[1]	EQ_DYN_FREQ2[0]	EQ_DYN_FREQ1[3]	EQ_DYN_FREQ1[2]	EQ_DYN_FREQ1[1]	EQ_DYN_FREQ1[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x8D	0x0B	EQ_DYN1_LF	rw	EQ_DYN1_LF[7]	EQ_DYN1_LF[6]	EQ_DYN1_LF[5]	EQ_DYN1_LF[4]	EQ_DYN1_LF[3]	EQ_DYN1_LF[2]	EQ_DYN1_LF[1]	EQ_DYN1_LF[0]
0x8E	0x20	EQ_DYN1_HF	rw	EQ_DYN1_HF[7]	EQ_DYN1_HF[6]	EQ_DYN1_HF[5]	EQ_DYN1_HF[4]	EQ_DYN1_HF[3]	EQ_DYN1_HF[2]	EQ_DYN1_HF[1]	EQ_DYN1_HF[0]
0x90	0x0B	EQ_DYN2_LF	rw	EQ_DYN2_LF[7]	EQ_DYN2_LF[6]	EQ_DYN2_LF[5]	EQ_DYN2_LF[4]	EQ_DYN2_LF[3]	EQ_DYN2_LF[2]	EQ_DYN2_LF[1]	EQ_DYN2_LF[0]
0x91	0x20	EQ_DYN2_HF	rw	EQ_DYN2_HF[7]	EQ_DYN2_HF[6]	EQ_DYN2_HF[5]	EQ_DYN2_HF[4]	EQ_DYN2_HF[3]	EQ_DYN2_HF[2]	EQ_DYN2_HF[1]	EQ_DYN2_HF[0]
0x93	0x0B	EQ_DYN3_LF	rw	EQ_DYN3_LF[7]	EQ_DYN3_LF[6]	EQ_DYN3_LF[5]	EQ_DYN3_LF[4]	EQ_DYN3_LF[3]	EQ_DYN3_LF[2]	EQ_DYN3_LF[1]	EQ_DYN3_LF[0]
0x94	0x20	EQ_DYN3_HF	rw	EQ_DYN3_HF[7]	EQ_DYN3_HF[6]	EQ_DYN3_HF[5]	EQ_DYN3_HF[4]	EQ_DYN3_HF[3]	EQ_DYN3_HF[2]	EQ_DYN3_HF[1]	EQ_DYN3_HF[0]
0x96	0x00	EQ DYNAMIC ENABLE	rw	-	-	-	-	-	-	-	EQ_DYN_EN
0xE0	0x00		r	BG_TMDSFREQ[8]	BG_TMDSFREQ[7]	BG_TMDSFREQ[6]	BG_TMDSFREQ[5]	BG_TMDSFREQ[4]	BG_TMDSFREQ[3]	BG_TMDSFREQ[2]	BG_TMDSFREQ[1]
0xE1	0x00		r	BG_TMDSFREQ[0]	BG_TMDSFREQ_FRAC[6]	BG_TMDSFREQ_FRAC[5]	BG_TMDSFREQ_FRAC[4]	BG_TMDSFREQ_FRAC[3]	BG_TMDSFREQ_FRAC[2]	BG_TMDSFREQ_FRAC[1]	BG_TMDSFREQ_FRAC[0]
0xE2	0x00		r	-	-	-	BG_LINE_WIDTH[12]	BG_LINE_WIDTH[11]	BG_LINE_WIDTH[10]	BG_LINE_WIDTH[9]	BG_LINE_WIDTH[8]
0xE3	0x00		r	BG_LINE_WIDTH[7]	BG_LINE_WIDTH[6]	BG_LINE_WIDTH[5]	BG_LINE_WIDTH[4]	BG_LINE_WIDTH[3]	BG_LINE_WIDTH[2]	BG_LINE_WIDTH[1]	BG_LINE_WIDTH[0]
0xE4	0x00		r	-	-	BG_TOTAL_LINE_WIDTH[13]	BG_TOTAL_LINE_WIDTH[12]	BG_TOTAL_LINE_WIDTH[11]	BG_TOTAL_LINE_WIDTH[10]	BG_TOTAL_LINE_WIDTH[9]	BG_TOTAL_LINE_WIDTH[8]
0xE5	0x00		r	BG_TOTAL_LINE_WIDTH[7]	BG_TOTAL_LINE_WIDTH[6]	BG_TOTAL_LINE_WIDTH[5]	BG_TOTAL_LINE_WIDTH[4]	BG_TOTAL_LINE_WIDTH[3]	BG_TOTAL_LINE_WIDTH[2]	BG_TOTAL_LINE_WIDTH[1]	BG_TOTAL_LINE_WIDTH[0]
0xE6	0x00		r	-	-	-	BG_FIELD_HEIGHT[12]	BG_FIELD_HEIGHT[11]	BG_FIELD_HEIGHT[10]	BG_FIELD_HEIGHT[9]	BG_FIELD_HEIGHT[8]
0xE7	0x00		r	BG_FIELD_HEIGHT[7]	BG_FIELD_HEIGHT[6]	BG_FIELD_HEIGHT[5]	BG_FIELD_HEIGHT[4]	BG_FIELD_HEIGHT[3]	BG_FIELD_HEIGHT[2]	BG_FIELD_HEIGHT[1]	BG_FIELD_HEIGHT[0]
0xE8	0x00		r	-	-	-	BG_TOTAL_FIELD_HEIGHT[12]	BG_TOTAL_FIELD_HEIGHT[11]	BG_TOTAL_FIELD_HEIGHT[10]	BG_TOTAL_FIELD_HEIGHT[9]	BG_TOTAL_FIELD_HEIGHT[8]
0xE9	0x00		r	BG_TOTAL_FIELD_HEIGHT[7]	BG_TOTAL_FIELD_HEIGHT[6]	BG_TOTAL_FIELD_HEIGHT[5]	BG_TOTAL_FIELD_HEIGHT[4]	BG_TOTAL_FIELD_HEIGHT[3]	BG_TOTAL_FIELD_HEIGHT[2]	BG_TOTAL_FIELD_HEIGHT[1]	BG_TOTAL_FIELD_HEIGHT[0]
0xEA	0x00		r	BG_PIX_REP[3]	BG_PIX_REP[2]	BG_PIX_REP[1]	BG_PIX_REP[0]	BG_DEEP_COLOR_MODE[1]	BG_DEEP_COLOR_MODE[0]	BG_PARAM_LOCK	BG_HDMI_INTERLACED
0xEB	0x00		r	-	-	-	-	-	-	-	BG_HDMI_MODE

1.10 REPEATER MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	BKSV_1	r	BKSV[7]	BKSV[6]	BKSV[5]	BKSV[4]	BKSV[3]	BKSV[2]	BKSV[1]	BKSV[0]
0x01	0x00	BKSV_2	r	BKSV[15]	BKSV[14]	BKSV[13]	BKSV[12]	BKSV[11]	BKSV[10]	BKSV[9]	BKSV[8]
0x02	0x00	BKSV_3	r	BKSV[23]	BKSV[22]	BKSV[21]	BKSV[20]	BKSV[19]	BKSV[18]	BKSV[17]	BKSV[16]
0x03	0x00	BKSV_4	r	BKSV[31]	BKSV[30]	BKSV[29]	BKSV[28]	BKSV[27]	BKSV[26]	BKSV[25]	BKSV[24]
0x04	0x00	BKSV_5	r	BKSV[39]	BKSV[38]	BKSV[37]	BKSV[36]	BKSV[35]	BKSV[34]	BKSV[33]	BKSV[32]
0x08	0x00	RI_1	r	RI[7]	RI[6]	RI[5]	RI[4]	RI[3]	RI[2]	RI[1]	RI[0]
0x09	0x00	RI_2	r	RI[15]	RI[14]	RI[13]	RI[12]	RI[11]	RI[10]	RI[9]	RI[8]
0x0A	0x00	PJ	r	PJ[7]	PJ[6]	PJ[5]	PJ[4]	PJ[3]	PJ[2]	PJ[1]	PJ[0]
0x10	0x00	AKSV_1	rw	AKSV[7]	AKSV[6]	AKSV[5]	AKSV[4]	AKSV[3]	AKSV[2]	AKSV[1]	AKSV[0]
0x11	0x00	AKSV_2	rw	AKSV[15]	AKSV[14]	AKSV[13]	AKSV[12]	AKSV[11]	AKSV[10]	AKSV[9]	AKSV[8]
0x12	0x00	AKSV_3	rw	AKSV[23]	AKSV[22]	AKSV[21]	AKSV[20]	AKSV[19]	AKSV[18]	AKSV[17]	AKSV[16]
0x13	0x00	AKSV_4	rw	AKSV[31]	AKSV[30]	AKSV[29]	AKSV[28]	AKSV[27]	AKSV[26]	AKSV[25]	AKSV[24]
0x14	0x00	AKSV_5	rw	AKSV[39]	AKSV[38]	AKSV[37]	AKSV[36]	AKSV[35]	AKSV[34]	AKSV[33]	AKSV[32]
0x15	0x00	AINFO	rw	AINFO[7]	AINFO[6]	AINFO[5]	AINFO[4]	AINFO[3]	AINFO[2]	AINFO[1]	AINFO[0]
0x18	0x00	AN_1	rw	AN[7]	AN[6]	AN[5]	AN[4]	AN[3]	AN[2]	AN[1]	AN[0]
0x19	0x00	AN_2	rw	AN[15]	AN[14]	AN[13]	AN[12]	AN[11]	AN[10]	AN[9]	AN[8]
0x1A	0x00	AN_3	rw	AN[23]	AN[22]	AN[21]	AN[20]	AN[19]	AN[18]	AN[17]	AN[16]
0x1B	0x00	AN_4	rw	AN[31]	AN[30]	AN[29]	AN[28]	AN[27]	AN[26]	AN[25]	AN[24]
0x1C	0x00	AN_5	rw	AN[39]	AN[38]	AN[37]	AN[36]	AN[35]	AN[34]	AN[33]	AN[32]
0x1D	0x00	AN_6	rw	AN[47]	AN[46]	AN[45]	AN[44]	AN[43]	AN[42]	AN[41]	AN[40]
0x1E	0x00	AN_7	rw	AN[55]	AN[54]	AN[53]	AN[52]	AN[51]	AN[50]	AN[49]	AN[48]
0x1F	0x00	AN_8	rw	AN[63]	AN[62]	AN[61]	AN[60]	AN[59]	AN[58]	AN[57]	AN[56]
0x20	0x00	SHA_A_1	rw	SHA_A[7]	SHA_A[6]	SHA_A[5]	SHA_A[4]	SHA_A[3]	SHA_A[2]	SHA_A[1]	SHA_A[0]
0x21	0x00	SHA_A_2	rw	SHA_A[15]	SHA_A[14]	SHA_A[13]	SHA_A[12]	SHA_A[11]	SHA_A[10]	SHA_A[9]	SHA_A[8]
0x22	0x00	SHA_A_3	rw	SHA_A[23]	SHA_A[22]	SHA_A[21]	SHA_A[20]	SHA_A[19]	SHA_A[18]	SHA_A[17]	SHA_A[16]
0x23	0x00	SHA_A_4	rw	SHA_A[31]	SHA_A[30]	SHA_A[29]	SHA_A[28]	SHA_A[27]	SHA_A[26]	SHA_A[25]	SHA_A[24]
0x24	0x00	SHA_B_1	rw	SHA_B[7]	SHA_B[6]	SHA_B[5]	SHA_B[4]	SHA_B[3]	SHA_B[2]	SHA_B[1]	SHA_B[0]
0x25	0x00	SHA_B_2	rw	SHA_B[15]	SHA_B[14]	SHA_B[13]	SHA_B[12]	SHA_B[11]	SHA_B[10]	SHA_B[9]	SHA_B[8]
0x26	0x00	SHA_B_3	rw	SHA_B[23]	SHA_B[22]	SHA_B[21]	SHA_B[20]	SHA_B[19]	SHA_B[18]	SHA_B[17]	SHA_B[16]
0x27	0x00	SHA_B_4	rw	SHA_B[31]	SHA_B[30]	SHA_B[29]	SHA_B[28]	SHA_B[27]	SHA_B[26]	SHA_B[25]	SHA_B[24]
0x28	0x00	SHA_C_1	rw	SHA_C[7]	SHA_C[6]	SHA_C[5]	SHA_C[4]	SHA_C[3]	SHA_C[2]	SHA_C[1]	SHA_C[0]
0x29	0x00	SHA_C_2	rw	SHA_C[15]	SHA_C[14]	SHA_C[13]	SHA_C[12]	SHA_C[11]	SHA_C[10]	SHA_C[9]	SHA_C[8]
0x2A	0x00	SHA_C_3	rw	SHA_C[23]	SHA_C[22]	SHA_C[21]	SHA_C[20]	SHA_C[19]	SHA_C[18]	SHA_C[17]	SHA_C[16]
0x2B	0x00	SHA_C_4	rw	SHA_C[31]	SHA_C[30]	SHA_C[29]	SHA_C[28]	SHA_C[27]	SHA_C[26]	SHA_C[25]	SHA_C[24]
0x2C	0x00	SHA_D_1	rw	SHA_D[7]	SHA_D[6]	SHA_D[5]	SHA_D[4]	SHA_D[3]	SHA_D[2]	SHA_D[1]	SHA_D[0]
0x2D	0x00	SHA_D_2	rw	SHA_D[15]	SHA_D[14]	SHA_D[13]	SHA_D[12]	SHA_D[11]	SHA_D[10]	SHA_D[9]	SHA_D[8]
0x2E	0x00	SHA_D_3	rw	SHA_D[23]	SHA_D[22]	SHA_D[21]	SHA_D[20]	SHA_D[19]	SHA_D[18]	SHA_D[17]	SHA_D[16]
0x2F	0x00	SHA_D_4	rw	SHA_D[31]	SHA_D[30]	SHA_D[29]	SHA_D[28]	SHA_D[27]	SHA_D[26]	SHA_D[25]	SHA_D[24]
0x30	0x00	SHA_E_1	rw	SHA_E[7]	SHA_E[6]	SHA_E[5]	SHA_E[4]	SHA_E[3]	SHA_E[2]	SHA_E[1]	SHA_E[0]
0x31	0x00	SHA_E_2	rw	SHA_E[15]	SHA_E[14]	SHA_E[13]	SHA_E[12]	SHA_E[11]	SHA_E[10]	SHA_E[9]	SHA_E[8]
0x32	0x00	SHA_E_3	rw	SHA_E[23]	SHA_E[22]	SHA_E[21]	SHA_E[20]	SHA_E[19]	SHA_E[18]	SHA_E[17]	SHA_E[16]
0x33	0x00	SHA_E_4	rw	SHA_E[31]	SHA_E[30]	SHA_E[29]	SHA_E[28]	SHA_E[27]	SHA_E[26]	SHA_E[25]	SHA_E[24]
0x40	0x83	BCAPS	rw	BCAPS[7]	BCAPS[6]	BCAPS[5]	BCAPS[4]	BCAPS[3]	BCAPS[2]	BCAPS[1]	BCAPS[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x41	0x00	BSTATUS_1	rw	BSTATUS[7]	BSTATUS[6]	BSTATUS[5]	BSTATUS[4]	BSTATUS[3]	BSTATUS[2]	BSTATUS[1]	BSTATUS[0]
0x42	0x00	BSTATUS_2	rw	BSTATUS[15]	BSTATUS[14]	BSTATUS[13]	BSTATUS[12]	BSTATUS[11]	BSTATUS[10]	BSTATUS[9]	BSTATUS[8]
0x72	0x00	SPA PORT C_1	rw	SPA_PORT_A[15]	SPA_PORT_A[14]	SPA_PORT_A[13]	SPA_PORT_A[12]	SPA_PORT_A[11]	SPA_PORT_A[10]	SPA_PORT_A[9]	SPA_PORT_A[8]
0x73	0x00	SPA PORT C_2	rw	SPA_PORT_A[7]	SPA_PORT_A[6]	SPA_PORT_A[5]	SPA_PORT_A[4]	SPA_PORT_A[3]	SPA_PORT_A[2]	SPA_PORT_A[1]	SPA_PORT_A[0]
0x74	0x00	SPA PORT D_1	rw	SPA_PORT_B[15]	SPA_PORT_B[14]	SPA_PORT_B[13]	SPA_PORT_B[12]	SPA_PORT_B[11]	SPA_PORT_B[10]	SPA_PORT_B[9]	SPA_PORT_B[8]
0x75	0x00	SPA PORT D_2	rw	SPA_PORT_B[7]	SPA_PORT_B[6]	SPA_PORT_B[5]	SPA_PORT_B[4]	SPA_PORT_B[3]	SPA_PORT_B[2]	SPA_PORT_B[1]	SPA_PORT_B[0]
0x76	0xC0	SPA LOCATION	rw	SPA_LOCATION[7]	SPA_LOCATION[6]	SPA_LOCATION[5]	SPA_LOCATION[4]	SPA_LOCATION[3]	SPA_LOCATION[2]	SPA_LOCATION[1]	SPA_LOCATION[0]
0x77	0x00		rw	KSV_LIST_READY	SPA_LOCATION_MSB	DISABLE_AUTO_EDID	EDID_SEGMENT_POINTER	EDID_B_ENABLE	EDID_A_ENABLE	-	-
0x78	0x00	IROM BIST	rw	-	EXT_EEPROM_TRI	-	-	-	-	-	-
0x79	0x00		r	-	-	VGA_EDID_ENABLE_CPU	-	-	-	-	-
0x7B	0x00	PORT C CHECKSUM	rw	PORT_A_CHECKSUM[7]	PORT_A_CHECKSUM[6]	PORT_A_CHECKSUM[5]	PORT_A_CHECKSUM[4]	PORT_A_CHECKSUM[3]	PORT_A_CHECKSUM[2]	PORT_A_CHECKSUM[1]	PORT_A_CHECKSUM[0]
0x7C	0x00	PORT D CHECKSUM	rw	PORT_B_CHECKSUM[7]	PORT_B_CHECKSUM[6]	PORT_B_CHECKSUM[5]	PORT_B_CHECKSUM[4]	PORT_B_CHECKSUM[3]	PORT_B_CHECKSUM[2]	PORT_B_CHECKSUM[1]	PORT_B_CHECKSUM[0]
0x7D	0x00	EDID DEBUG	r	-	-	-	-	EDID_B_ENABLE_CPU	EDID_A_ENABLE_CPU	-	-
0x7E	0x00		sc	-	-	KSV_LIST_READY_CLEAR_A	KSV_LIST_READY_CLEAR_B	-	-	LOAD_EDID	STORE_EDID
0x7F	0x04		rw	VGA_EDID_ENABLE	-	-	-	-	AUTO_HDCP_MAP_ENABLE	HDCP_MAP_SELECT[1]	HDCP_MAP_SELECT[0]
0x80	0x00	KSV 0_1	rw	KSV_0[7]	KSV_0[6]	KSV_0[5]	KSV_0[4]	KSV_0[3]	KSV_0[2]	KSV_0[1]	KSV_0[0]
0x81	0x00	KSV 0_2	rw	KSV_0[15]	KSV_0[14]	KSV_0[13]	KSV_0[12]	KSV_0[11]	KSV_0[10]	KSV_0[9]	KSV_0[8]
0x82	0x00	KSV 0_3	rw	KSV_0[23]	KSV_0[22]	KSV_0[21]	KSV_0[20]	KSV_0[19]	KSV_0[18]	KSV_0[17]	KSV_0[16]
0x83	0x00	KSV 0_4	rw	KSV_0[31]	KSV_0[30]	KSV_0[29]	KSV_0[28]	KSV_0[27]	KSV_0[26]	KSV_0[25]	KSV_0[24]
0x84	0x00	KSV 0_5	rw	KSV_0[39]	KSV_0[38]	KSV_0[37]	KSV_0[36]	KSV_0[35]	KSV_0[34]	KSV_0[33]	KSV_0[32]
0x85	0x00	KSV 1_1	rw	KSV_1[7]	KSV_1[6]	KSV_1[5]	KSV_1[4]	KSV_1[3]	KSV_1[2]	KSV_1[1]	KSV_1[0]
0x86	0x00	KSV 1_2	rw	KSV_1[15]	KSV_1[14]	KSV_1[13]	KSV_1[12]	KSV_1[11]	KSV_1[10]	KSV_1[9]	KSV_1[8]
0x87	0x00	KSV 1_3	rw	KSV_1[23]	KSV_1[22]	KSV_1[21]	KSV_1[20]	KSV_1[19]	KSV_1[18]	KSV_1[17]	KSV_1[16]
0x88	0x00	KSV 1_4	rw	KSV_1[31]	KSV_1[30]	KSV_1[29]	KSV_1[28]	KSV_1[27]	KSV_1[26]	KSV_1[25]	KSV_1[24]
0x89	0x00	KSV 1_5	rw	KSV_1[39]	KSV_1[38]	KSV_1[37]	KSV_1[36]	KSV_1[35]	KSV_1[34]	KSV_1[33]	KSV_1[32]
0x8A	0x00	KSV 2_1	rw	KSV_2[7]	KSV_2[6]	KSV_2[5]	KSV_2[4]	KSV_2[3]	KSV_2[2]	KSV_2[1]	KSV_2[0]
0x8B	0x00	KSV 2_2	rw	KSV_2[15]	KSV_2[14]	KSV_2[13]	KSV_2[12]	KSV_2[11]	KSV_2[10]	KSV_2[9]	KSV_2[8]
0x8C	0x00	KSV 2_3	rw	KSV_2[23]	KSV_2[22]	KSV_2[21]	KSV_2[20]	KSV_2[19]	KSV_2[18]	KSV_2[17]	KSV_2[16]
0x8D	0x00	KSV 2_4	rw	KSV_2[31]	KSV_2[30]	KSV_2[29]	KSV_2[28]	KSV_2[27]	KSV_2[26]	KSV_2[25]	KSV_2[24]
0x8E	0x00	KSV 2_5	rw	KSV_2[39]	KSV_2[38]	KSV_2[37]	KSV_2[36]	KSV_2[35]	KSV_2[34]	KSV_2[33]	KSV_2[32]
0x8F	0x00	KSV 3_1	rw	KSV_3[7]	KSV_3[6]	KSV_3[5]	KSV_3[4]	KSV_3[3]	KSV_3[2]	KSV_3[1]	KSV_3[0]
0x90	0x00	KSV 3_2	rw	KSV_3[15]	KSV_3[14]	KSV_3[13]	KSV_3[12]	KSV_3[11]	KSV_3[10]	KSV_3[9]	KSV_3[8]
0x91	0x00	KSV 3_3	rw	KSV_3[23]	KSV_3[22]	KSV_3[21]	KSV_3[20]	KSV_3[19]	KSV_3[18]	KSV_3[17]	KSV_3[16]
0x92	0x00	KSV 3_4	rw	KSV_3[31]	KSV_3[30]	KSV_3[29]	KSV_3[28]	KSV_3[27]	KSV_3[26]	KSV_3[25]	KSV_3[24]
0x93	0x00	KSV 3_5	rw	KSV_3[39]	KSV_3[38]	KSV_3[37]	KSV_3[36]	KSV_3[35]	KSV_3[34]	KSV_3[33]	KSV_3[32]
0x94	0x00	KSV 4_1	rw	KSV_4[7]	KSV_4[6]	KSV_4[5]	KSV_4[4]	KSV_4[3]	KSV_4[2]	KSV_4[1]	KSV_4[0]
0x95	0x00	KSV 4_2	rw	KSV_4[15]	KSV_4[14]	KSV_4[13]	KSV_4[12]	KSV_4[11]	KSV_4[10]	KSV_4[9]	KSV_4[8]
0x96	0x00	KSV 4_3	rw	KSV_4[23]	KSV_4[22]	KSV_4[21]	KSV_4[20]	KSV_4[19]	KSV_4[18]	KSV_4[17]	KSV_4[16]
0x97	0x00	KSV 4_4	rw	KSV_4[31]	KSV_4[30]	KSV_4[29]	KSV_4[28]	KSV_4[27]	KSV_4[26]	KSV_4[25]	KSV_4[24]
0x98	0x00	KSV 4_5	rw	KSV_4[39]	KSV_4[38]	KSV_4[37]	KSV_4[36]	KSV_4[35]	KSV_4[34]	KSV_4[33]	KSV_4[32]
0x99	0x00	KSV 5_1	rw	KSV_5[7]	KSV_5[6]	KSV_5[5]	KSV_5[4]	KSV_5[3]	KSV_5[2]	KSV_5[1]	KSV_5[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9A	0x00	KSV 5_2	rw	KSV_5[15]	KSV_5[14]	KSV_5[13]	KSV_5[12]	KSV_5[11]	KSV_5[10]	KSV_5[9]	KSV_5[8]
0x9B	0x00	KSV 5_3	rw	KSV_5[23]	KSV_5[22]	KSV_5[21]	KSV_5[20]	KSV_5[19]	KSV_5[18]	KSV_5[17]	KSV_5[16]
0x9C	0x00	KSV 5_4	rw	KSV_5[31]	KSV_5[30]	KSV_5[29]	KSV_5[28]	KSV_5[27]	KSV_5[26]	KSV_5[25]	KSV_5[24]
0x9D	0x00	KSV 5_5	rw	KSV_5[39]	KSV_5[38]	KSV_5[37]	KSV_5[36]	KSV_5[35]	KSV_5[34]	KSV_5[33]	KSV_5[32]
0x9E	0x00	KSV 6_1	rw	KSV_6[7]	KSV_6[6]	KSV_6[5]	KSV_6[4]	KSV_6[3]	KSV_6[2]	KSV_6[1]	KSV_6[0]
0x9F	0x00	KSV 6_2	rw	KSV_6[15]	KSV_6[14]	KSV_6[13]	KSV_6[12]	KSV_6[11]	KSV_6[10]	KSV_6[9]	KSV_6[8]
0xA0	0x00	KSV 6_3	rw	KSV_6[23]	KSV_6[22]	KSV_6[21]	KSV_6[20]	KSV_6[19]	KSV_6[18]	KSV_6[17]	KSV_6[16]
0xA1	0x00	KSV 6_4	rw	KSV_6[31]	KSV_6[30]	KSV_6[29]	KSV_6[28]	KSV_6[27]	KSV_6[26]	KSV_6[25]	KSV_6[24]
0xA2	0x00	KSV 6_5	rw	KSV_6[39]	KSV_6[38]	KSV_6[37]	KSV_6[36]	KSV_6[35]	KSV_6[34]	KSV_6[33]	KSV_6[32]
0xA3	0x00	KSV 7_1	rw	KSV_7[7]	KSV_7[6]	KSV_7[5]	KSV_7[4]	KSV_7[3]	KSV_7[2]	KSV_7[1]	KSV_7[0]
0xA4	0x00	KSV 7_2	rw	KSV_7[15]	KSV_7[14]	KSV_7[13]	KSV_7[12]	KSV_7[11]	KSV_7[10]	KSV_7[9]	KSV_7[8]
0xA5	0x00	KSV 7_3	rw	KSV_7[23]	KSV_7[22]	KSV_7[21]	KSV_7[20]	KSV_7[19]	KSV_7[18]	KSV_7[17]	KSV_7[16]
0xA6	0x00	KSV 7_4	rw	KSV_7[31]	KSV_7[30]	KSV_7[29]	KSV_7[28]	KSV_7[27]	KSV_7[26]	KSV_7[25]	KSV_7[24]
0xA7	0x00	KSV 7_5	rw	KSV_7[39]	KSV_7[38]	KSV_7[37]	KSV_7[36]	KSV_7[35]	KSV_7[34]	KSV_7[33]	KSV_7[32]
0xA8	0x00	KSV 8_1	rw	KSV_8[7]	KSV_8[6]	KSV_8[5]	KSV_8[4]	KSV_8[3]	KSV_8[2]	KSV_8[1]	KSV_8[0]
0xA9	0x00	KSV 8_2	rw	KSV_8[15]	KSV_8[14]	KSV_8[13]	KSV_8[12]	KSV_8[11]	KSV_8[10]	KSV_8[9]	KSV_8[8]
0xAA	0x00	KSV 8_3	rw	KSV_8[23]	KSV_8[22]	KSV_8[21]	KSV_8[20]	KSV_8[19]	KSV_8[18]	KSV_8[17]	KSV_8[16]
0xAB	0x00	KSV 8_4	rw	KSV_8[31]	KSV_8[30]	KSV_8[29]	KSV_8[28]	KSV_8[27]	KSV_8[26]	KSV_8[25]	KSV_8[24]
0xAC	0x00	KSV 8_5	rw	KSV_8[39]	KSV_8[38]	KSV_8[37]	KSV_8[36]	KSV_8[35]	KSV_8[34]	KSV_8[33]	KSV_8[32]
0xAD	0x00	KSV 9_1	rw	KSV_9[7]	KSV_9[6]	KSV_9[5]	KSV_9[4]	KSV_9[3]	KSV_9[2]	KSV_9[1]	KSV_9[0]
0xAE	0x00	KSV 9_2	rw	KSV_9[15]	KSV_9[14]	KSV_9[13]	KSV_9[12]	KSV_9[11]	KSV_9[10]	KSV_9[9]	KSV_9[8]
0xAF	0x00	KSV 9_3	rw	KSV_9[23]	KSV_9[22]	KSV_9[21]	KSV_9[20]	KSV_9[19]	KSV_9[18]	KSV_9[17]	KSV_9[16]
0xB0	0x00	KSV 9_4	rw	KSV_9[31]	KSV_9[30]	KSV_9[29]	KSV_9[28]	KSV_9[27]	KSV_9[26]	KSV_9[25]	KSV_9[24]
0xB1	0x00	KSV 9_5	rw	KSV_9[39]	KSV_9[38]	KSV_9[37]	KSV_9[36]	KSV_9[35]	KSV_9[34]	KSV_9[33]	KSV_9[32]
0xB2	0x00	KSV 10_1	rw	KSV_10[7]	KSV_10[6]	KSV_10[5]	KSV_10[4]	KSV_10[3]	KSV_10[2]	KSV_10[1]	KSV_10[0]
0xB3	0x00	KSV 10_2	rw	KSV_10[15]	KSV_10[14]	KSV_10[13]	KSV_10[12]	KSV_10[11]	KSV_10[10]	KSV_10[9]	KSV_10[8]
0xB4	0x00	KSV 10_3	rw	KSV_10[23]	KSV_10[22]	KSV_10[21]	KSV_10[20]	KSV_10[19]	KSV_10[18]	KSV_10[17]	KSV_10[16]
0xB5	0x00	KSV 10_4	rw	KSV_10[31]	KSV_10[30]	KSV_10[29]	KSV_10[28]	KSV_10[27]	KSV_10[26]	KSV_10[25]	KSV_10[24]
0xB6	0x00	KSV 10_5	rw	KSV_10[39]	KSV_10[38]	KSV_10[37]	KSV_10[36]	KSV_10[35]	KSV_10[34]	KSV_10[33]	KSV_10[32]
0xB7	0x00	KSV 11_1	rw	KSV_11[7]	KSV_11[6]	KSV_11[5]	KSV_11[4]	KSV_11[3]	KSV_11[2]	KSV_11[1]	KSV_11[0]
0xB8	0x00	KSV 11_2	rw	KSV_11[15]	KSV_11[14]	KSV_11[13]	KSV_11[12]	KSV_11[11]	KSV_11[10]	KSV_11[9]	KSV_11[8]
0xB9	0x00	KSV 11_3	rw	KSV_11[23]	KSV_11[22]	KSV_11[21]	KSV_11[20]	KSV_11[19]	KSV_11[18]	KSV_11[17]	KSV_11[16]
0xBA	0x00	KSV 11_4	rw	KSV_11[31]	KSV_11[30]	KSV_11[29]	KSV_11[28]	KSV_11[27]	KSV_11[26]	KSV_11[25]	KSV_11[24]
0xBB	0x00	KSV 11_5	rw	KSV_11[39]	KSV_11[38]	KSV_11[37]	KSV_11[36]	KSV_11[35]	KSV_11[34]	KSV_11[33]	KSV_11[32]
0xBC	0x00	KSV 12_1	rw	KSV_12[7]	KSV_12[6]	KSV_12[5]	KSV_12[4]	KSV_12[3]	KSV_12[2]	KSV_12[1]	KSV_12[0]
0xBD	0x00	KSV 12_2	rw	KSV_12[15]	KSV_12[14]	KSV_12[13]	KSV_12[12]	KSV_12[11]	KSV_12[10]	KSV_12[9]	KSV_12[8]
0xBE	0x00	KSV 12_3	rw	KSV_12[23]	KSV_12[22]	KSV_12[21]	KSV_12[20]	KSV_12[19]	KSV_12[18]	KSV_12[17]	KSV_12[16]
0xBF	0x00	KSV 12_4	rw	KSV_12[31]	KSV_12[30]	KSV_12[29]	KSV_12[28]	KSV_12[27]	KSV_12[26]	KSV_12[25]	KSV_12[24]
0xC0	0x00	KSV 12_5	rw	KSV_12[39]	KSV_12[38]	KSV_12[37]	KSV_12[36]	KSV_12[35]	KSV_12[34]	KSV_12[33]	KSV_12[32]
0xC1	0x00	KSV 13_1	rw	KSV_13[7]	KSV_13[6]	KSV_13[5]	KSV_13[4]	KSV_13[3]	KSV_13[2]	KSV_13[1]	KSV_13[0]
0xC2	0x00	KSV 13_2	rw	KSV_13[15]	KSV_13[14]	KSV_13[13]	KSV_13[12]	KSV_13[11]	KSV_13[10]	KSV_13[9]	KSV_13[8]
0xC3	0x00	KSV 13_3	rw	KSV_13[23]	KSV_13[22]	KSV_13[21]	KSV_13[20]	KSV_13[19]	KSV_13[18]	KSV_13[17]	KSV_13[16]
0xC4	0x00	KSV 13_4	rw	KSV_13[31]	KSV_13[30]	KSV_13[29]	KSV_13[28]	KSV_13[27]	KSV_13[26]	KSV_13[25]	KSV_13[24]
0xC5	0x00	KSV 13_5	rw	KSV_13[39]	KSV_13[38]	KSV_13[37]	KSV_13[36]	KSV_13[35]	KSV_13[34]	KSV_13[33]	KSV_13[32]
0xC6	0x00	KSV 14_1	rw	KSV_14[7]	KSV_14[6]	KSV_14[5]	KSV_14[4]	KSV_14[3]	KSV_14[2]	KSV_14[1]	KSV_14[0]
0xC7	0x00	KSV 14_2	rw	KSV_14[15]	KSV_14[14]	KSV_14[13]	KSV_14[12]	KSV_14[11]	KSV_14[10]	KSV_14[9]	KSV_14[8]
0xC8	0x00	KSV 14_3	rw	KSV_14[23]	KSV_14[22]	KSV_14[21]	KSV_14[20]	KSV_14[19]	KSV_14[18]	KSV_14[17]	KSV_14[16]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xC9	0x00	KSV 14_4	rw	KSV_14[31]	KSV_14[30]	KSV_14[29]	KSV_14[28]	KSV_14[27]	KSV_14[26]	KSV_14[25]	KSV_14[24]
0xCA	0x00	KSV 14_5	rw	KSV_14[39]	KSV_14[38]	KSV_14[37]	KSV_14[36]	KSV_14[35]	KSV_14[34]	KSV_14[33]	KSV_14[32]
0xCB	0x00	KSV 15_1	rw	KSV_15[7]	KSV_15[6]	KSV_15[5]	KSV_15[4]	KSV_15[3]	KSV_15[2]	KSV_15[1]	KSV_15[0]
0xCC	0x00	KSV 15_2	rw	KSV_15[15]	KSV_15[14]	KSV_15[13]	KSV_15[12]	KSV_15[11]	KSV_15[10]	KSV_15[9]	KSV_15[8]
0xCD	0x00	KSV 15_3	rw	KSV_15[23]	KSV_15[22]	KSV_15[21]	KSV_15[20]	KSV_15[19]	KSV_15[18]	KSV_15[17]	KSV_15[16]
0xCE	0x00	KSV 15_4	rw	KSV_15[31]	KSV_15[30]	KSV_15[29]	KSV_15[28]	KSV_15[27]	KSV_15[26]	KSV_15[25]	KSV_15[24]
0xCF	0x00	KSV 15_5	rw	KSV_15[39]	KSV_15[38]	KSV_15[37]	KSV_15[36]	KSV_15[35]	KSV_15[34]	KSV_15[33]	KSV_15[32]
0xD0	0x00	KSV 16_1	rw	KSV_16[7]	KSV_16[6]	KSV_16[5]	KSV_16[4]	KSV_16[3]	KSV_16[2]	KSV_16[1]	KSV_16[0]
0xD1	0x00	KSV 16_2	rw	KSV_16[15]	KSV_16[14]	KSV_16[13]	KSV_16[12]	KSV_16[11]	KSV_16[10]	KSV_16[9]	KSV_16[8]
0xD2	0x00	KSV 16_3	rw	KSV_16[23]	KSV_16[22]	KSV_16[21]	KSV_16[20]	KSV_16[19]	KSV_16[18]	KSV_16[17]	KSV_16[16]
0xD3	0x00	KSV 16_4	rw	KSV_16[31]	KSV_16[30]	KSV_16[29]	KSV_16[28]	KSV_16[27]	KSV_16[26]	KSV_16[25]	KSV_16[24]
0xD4	0x00	KSV 16_5	rw	KSV_16[39]	KSV_16[38]	KSV_16[37]	KSV_16[36]	KSV_16[35]	KSV_16[34]	KSV_16[33]	KSV_16[32]
0xD5	0x00	KSV 17_1	rw	KSV_17[7]	KSV_17[6]	KSV_17[5]	KSV_17[4]	KSV_17[3]	KSV_17[2]	KSV_17[1]	KSV_17[0]
0xD6	0x00	KSV 17_2	rw	KSV_17[15]	KSV_17[14]	KSV_17[13]	KSV_17[12]	KSV_17[11]	KSV_17[10]	KSV_17[9]	KSV_17[8]
0xD7	0x00	KSV 17_3	rw	KSV_17[23]	KSV_17[22]	KSV_17[21]	KSV_17[20]	KSV_17[19]	KSV_17[18]	KSV_17[17]	KSV_17[16]
0xD8	0x00	KSV 17_4	rw	KSV_17[31]	KSV_17[30]	KSV_17[29]	KSV_17[28]	KSV_17[27]	KSV_17[26]	KSV_17[25]	KSV_17[24]
0xD9	0x00	KSV 17_5	rw	KSV_17[39]	KSV_17[38]	KSV_17[37]	KSV_17[36]	KSV_17[35]	KSV_17[34]	KSV_17[33]	KSV_17[32]
0xDA	0x00	KSV 18_1	rw	KSV_18[7]	KSV_18[6]	KSV_18[5]	KSV_18[4]	KSV_18[3]	KSV_18[2]	KSV_18[1]	KSV_18[0]
0xDB	0x00	KSV 18_2	rw	KSV_18[15]	KSV_18[14]	KSV_18[13]	KSV_18[12]	KSV_18[11]	KSV_18[10]	KSV_18[9]	KSV_18[8]
0xDC	0x00	KSV 18_3	rw	KSV_18[23]	KSV_18[22]	KSV_18[21]	KSV_18[20]	KSV_18[19]	KSV_18[18]	KSV_18[17]	KSV_18[16]
0xDD	0x00	KSV 18_4	rw	KSV_18[31]	KSV_18[30]	KSV_18[29]	KSV_18[28]	KSV_18[27]	KSV_18[26]	KSV_18[25]	KSV_18[24]
0xDE	0x00	KSV 18_5	rw	KSV_18[39]	KSV_18[38]	KSV_18[37]	KSV_18[36]	KSV_18[35]	KSV_18[34]	KSV_18[33]	KSV_18[32]
0xDF	0x00	KSV 19_1	rw	KSV_19[7]	KSV_19[6]	KSV_19[5]	KSV_19[4]	KSV_19[3]	KSV_19[2]	KSV_19[1]	KSV_19[0]
0xE0	0x00	KSV 19_2	rw	KSV_19[15]	KSV_19[14]	KSV_19[13]	KSV_19[12]	KSV_19[11]	KSV_19[10]	KSV_19[9]	KSV_19[8]
0xE1	0x00	KSV 19_3	rw	KSV_19[23]	KSV_19[22]	KSV_19[21]	KSV_19[20]	KSV_19[19]	KSV_19[18]	KSV_19[17]	KSV_19[16]
0xE2	0x00	KSV 19_4	rw	KSV_19[31]	KSV_19[30]	KSV_19[29]	KSV_19[28]	KSV_19[27]	KSV_19[26]	KSV_19[25]	KSV_19[24]
0xE3	0x00	KSV 19_5	rw	KSV_19[39]	KSV_19[38]	KSV_19[37]	KSV_19[36]	KSV_19[35]	KSV_19[34]	KSV_19[33]	KSV_19[32]
0xE4	0x00	KSV 20_1	rw	KSV_20[7]	KSV_20[6]	KSV_20[5]	KSV_20[4]	KSV_20[3]	KSV_20[2]	KSV_20[1]	KSV_20[0]
0xE5	0x00	KSV 20_2	rw	KSV_20[15]	KSV_20[14]	KSV_20[13]	KSV_20[12]	KSV_20[11]	KSV_20[10]	KSV_20[9]	KSV_20[8]
0xE6	0x00	KSV 20_3	rw	KSV_20[23]	KSV_20[22]	KSV_20[21]	KSV_20[20]	KSV_20[19]	KSV_20[18]	KSV_20[17]	KSV_20[16]
0xE7	0x00	KSV 20_4	rw	KSV_20[31]	KSV_20[30]	KSV_20[29]	KSV_20[28]	KSV_20[27]	KSV_20[26]	KSV_20[25]	KSV_20[24]
0xE8	0x00	KSV 20_5	rw	KSV_20[39]	KSV_20[38]	KSV_20[37]	KSV_20[36]	KSV_20[35]	KSV_20[34]	KSV_20[33]	KSV_20[32]
0xE9	0x00	KSV 21_1	rw	KSV_21[7]	KSV_21[6]	KSV_21[5]	KSV_21[4]	KSV_21[3]	KSV_21[2]	KSV_21[1]	KSV_21[0]
0xEA	0x00	KSV 21_2	rw	KSV_21[15]	KSV_21[14]	KSV_21[13]	KSV_21[12]	KSV_21[11]	KSV_21[10]	KSV_21[9]	KSV_21[8]
0xEB	0x00	KSV 21_3	rw	KSV_21[23]	KSV_21[22]	KSV_21[21]	KSV_21[20]	KSV_21[19]	KSV_21[18]	KSV_21[17]	KSV_21[16]
0xEC	0x00	KSV 21_4	rw	KSV_21[31]	KSV_21[30]	KSV_21[29]	KSV_21[28]	KSV_21[27]	KSV_21[26]	KSV_21[25]	KSV_21[24]
0xED	0x00	KSV 21_5	rw	KSV_21[39]	KSV_21[38]	KSV_21[37]	KSV_21[36]	KSV_21[35]	KSV_21[34]	KSV_21[33]	KSV_21[32]
0xEE	0x00	KSV 22_1	rw	KSV_22[7]	KSV_22[6]	KSV_22[5]	KSV_22[4]	KSV_22[3]	KSV_22[2]	KSV_22[1]	KSV_22[0]
0xEF	0x00	KSV 22_2	rw	KSV_22[15]	KSV_22[14]	KSV_22[13]	KSV_22[12]	KSV_22[11]	KSV_22[10]	KSV_22[9]	KSV_22[8]
0xF0	0x00	KSV 22_3	rw	KSV_22[23]	KSV_22[22]	KSV_22[21]	KSV_22[20]	KSV_22[19]	KSV_22[18]	KSV_22[17]	KSV_22[16]
0xF1	0x00	KSV 22_4	rw	KSV_22[31]	KSV_22[30]	KSV_22[29]	KSV_22[28]	KSV_22[27]	KSV_22[26]	KSV_22[25]	KSV_22[24]
0xF2	0x00	KSV 22_5	rw	KSV_22[39]	KSV_22[38]	KSV_22[37]	KSV_22[36]	KSV_22[35]	KSV_22[34]	KSV_22[33]	KSV_22[32]
0xF3	0x00	KSV 23_1	rw	KSV_23[7]	KSV_23[6]	KSV_23[5]	KSV_23[4]	KSV_23[3]	KSV_23[2]	KSV_23[1]	KSV_23[0]
0xF4	0x00	KSV 23_2	rw	KSV_23[15]	KSV_23[14]	KSV_23[13]	KSV_23[12]	KSV_23[11]	KSV_23[10]	KSV_23[9]	KSV_23[8]
0xF5	0x00	KSV 23_3	rw	KSV_23[23]	KSV_23[22]	KSV_23[21]	KSV_23[20]	KSV_23[19]	KSV_23[18]	KSV_23[17]	KSV_23[16]
0xF6	0x00	KSV 23_4	rw	KSV_23[31]	KSV_23[30]	KSV_23[29]	KSV_23[28]	KSV_23[27]	KSV_23[26]	KSV_23[25]	KSV_23[24]
0xF7	0x00	KSV 23_5	rw	KSV_23[39]	KSV_23[38]	KSV_23[37]	KSV_23[36]	KSV_23[35]	KSV_23[34]	KSV_23[33]	KSV_23[32]

1.11 INFOFRAME MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	AVI_INF_PB_0_1	r	AVI_INF_PB[7]	AVI_INF_PB[6]	AVI_INF_PB[5]	AVI_INF_PB[4]	AVI_INF_PB[3]	AVI_INF_PB[2]	AVI_INF_PB[1]	AVI_INF_PB[0]
0x01	0x00	AVI_INF_PB_0_2	r	AVI_INF_PB[15]	AVI_INF_PB[14]	AVI_INF_PB[13]	AVI_INF_PB[12]	AVI_INF_PB[11]	AVI_INF_PB[10]	AVI_INF_PB[9]	AVI_INF_PB[8]
0x02	0x00	AVI_INF_PB_0_3	r	AVI_INF_PB[23]	AVI_INF_PB[22]	AVI_INF_PB[21]	AVI_INF_PB[20]	AVI_INF_PB[19]	AVI_INF_PB[18]	AVI_INF_PB[17]	AVI_INF_PB[16]
0x03	0x00	AVI_INF_PB_0_4	r	AVI_INF_PB[31]	AVI_INF_PB[30]	AVI_INF_PB[29]	AVI_INF_PB[28]	AVI_INF_PB[27]	AVI_INF_PB[26]	AVI_INF_PB[25]	AVI_INF_PB[24]
0x04	0x00	AVI_INF_PB_0_5	r	AVI_INF_PB[39]	AVI_INF_PB[38]	AVI_INF_PB[37]	AVI_INF_PB[36]	AVI_INF_PB[35]	AVI_INF_PB[34]	AVI_INF_PB[33]	AVI_INF_PB[32]
0x05	0x00	AVI_INF_PB_0_6	r	AVI_INF_PB[47]	AVI_INF_PB[46]	AVI_INF_PB[45]	AVI_INF_PB[44]	AVI_INF_PB[43]	AVI_INF_PB[42]	AVI_INF_PB[41]	AVI_INF_PB[40]
0x06	0x00	AVI_INF_PB_0_7	r	AVI_INF_PB[55]	AVI_INF_PB[54]	AVI_INF_PB[53]	AVI_INF_PB[52]	AVI_INF_PB[51]	AVI_INF_PB[50]	AVI_INF_PB[49]	AVI_INF_PB[48]
0x07	0x00	AVI_INF_PB_0_8	r	AVI_INF_PB[63]	AVI_INF_PB[62]	AVI_INF_PB[61]	AVI_INF_PB[60]	AVI_INF_PB[59]	AVI_INF_PB[58]	AVI_INF_PB[57]	AVI_INF_PB[56]
0x08	0x00	AVI_INF_PB_0_9	r	AVI_INF_PB[71]	AVI_INF_PB[70]	AVI_INF_PB[69]	AVI_INF_PB[68]	AVI_INF_PB[67]	AVI_INF_PB[66]	AVI_INF_PB[65]	AVI_INF_PB[64]
0x09	0x00	AVI_INF_PB_0_10	r	AVI_INF_PB[79]	AVI_INF_PB[78]	AVI_INF_PB[77]	AVI_INF_PB[76]	AVI_INF_PB[75]	AVI_INF_PB[74]	AVI_INF_PB[73]	AVI_INF_PB[72]
0x0A	0x00	AVI_INF_PB_0_11	r	AVI_INF_PB[87]	AVI_INF_PB[86]	AVI_INF_PB[85]	AVI_INF_PB[84]	AVI_INF_PB[83]	AVI_INF_PB[82]	AVI_INF_PB[81]	AVI_INF_PB[80]
0x0B	0x00	AVI_INF_PB_0_12	r	AVI_INF_PB[95]	AVI_INF_PB[94]	AVI_INF_PB[93]	AVI_INF_PB[92]	AVI_INF_PB[91]	AVI_INF_PB[90]	AVI_INF_PB[89]	AVI_INF_PB[88]
0x0C	0x00	AVI_INF_PB_0_13	r	AVI_INF_PB[103]	AVI_INF_PB[102]	AVI_INF_PB[101]	AVI_INF_PB[100]	AVI_INF_PB[99]	AVI_INF_PB[98]	AVI_INF_PB[97]	AVI_INF_PB[96]
0x0D	0x00	AVI_INF_PB_0_14	r	AVI_INF_PB[111]	AVI_INF_PB[110]	AVI_INF_PB[109]	AVI_INF_PB[108]	AVI_INF_PB[107]	AVI_INF_PB[106]	AVI_INF_PB[105]	AVI_INF_PB[104]
0x0E	0x00	AVI_INF_PB_0_15	r	AVI_INF_PB[119]	AVI_INF_PB[118]	AVI_INF_PB[117]	AVI_INF_PB[116]	AVI_INF_PB[115]	AVI_INF_PB[114]	AVI_INF_PB[113]	AVI_INF_PB[112]
0x0F	0x00	AVI_INF_PB_0_16	r	AVI_INF_PB[127]	AVI_INF_PB[126]	AVI_INF_PB[125]	AVI_INF_PB[124]	AVI_INF_PB[123]	AVI_INF_PB[122]	AVI_INF_PB[121]	AVI_INF_PB[120]
0x10	0x00	AVI_INF_PB_0_17	r	AVI_INF_PB[135]	AVI_INF_PB[134]	AVI_INF_PB[133]	AVI_INF_PB[132]	AVI_INF_PB[131]	AVI_INF_PB[130]	AVI_INF_PB[129]	AVI_INF_PB[128]
0x11	0x00	AVI_INF_PB_0_18	r	AVI_INF_PB[143]	AVI_INF_PB[142]	AVI_INF_PB[141]	AVI_INF_PB[140]	AVI_INF_PB[139]	AVI_INF_PB[138]	AVI_INF_PB[137]	AVI_INF_PB[136]
0x12	0x00	AVI_INF_PB_0_19	r	AVI_INF_PB[151]	AVI_INF_PB[150]	AVI_INF_PB[149]	AVI_INF_PB[148]	AVI_INF_PB[147]	AVI_INF_PB[146]	AVI_INF_PB[145]	AVI_INF_PB[144]
0x13	0x00	AVI_INF_PB_0_20	r	AVI_INF_PB[159]	AVI_INF_PB[158]	AVI_INF_PB[157]	AVI_INF_PB[156]	AVI_INF_PB[155]	AVI_INF_PB[154]	AVI_INF_PB[153]	AVI_INF_PB[152]
0x14	0x00	AVI_INF_PB_0_21	r	AVI_INF_PB[167]	AVI_INF_PB[166]	AVI_INF_PB[165]	AVI_INF_PB[164]	AVI_INF_PB[163]	AVI_INF_PB[162]	AVI_INF_PB[161]	AVI_INF_PB[160]
0x15	0x00	AVI_INF_PB_0_22	r	AVI_INF_PB[175]	AVI_INF_PB[174]	AVI_INF_PB[173]	AVI_INF_PB[172]	AVI_INF_PB[171]	AVI_INF_PB[170]	AVI_INF_PB[169]	AVI_INF_PB[168]
0x16	0x00	AVI_INF_PB_0_23	r	AVI_INF_PB[183]	AVI_INF_PB[182]	AVI_INF_PB[181]	AVI_INF_PB[180]	AVI_INF_PB[179]	AVI_INF_PB[178]	AVI_INF_PB[177]	AVI_INF_PB[176]
0x17	0x00	AVI_INF_PB_0_24	r	AVI_INF_PB[191]	AVI_INF_PB[190]	AVI_INF_PB[189]	AVI_INF_PB[188]	AVI_INF_PB[187]	AVI_INF_PB[186]	AVI_INF_PB[185]	AVI_INF_PB[184]
0x18	0x00	AVI_INF_PB_0_25	r	AVI_INF_PB[199]	AVI_INF_PB[198]	AVI_INF_PB[197]	AVI_INF_PB[196]	AVI_INF_PB[195]	AVI_INF_PB[194]	AVI_INF_PB[193]	AVI_INF_PB[192]
0x19	0x00	AVI_INF_PB_0_26	r	AVI_INF_PB[207]	AVI_INF_PB[206]	AVI_INF_PB[205]	AVI_INF_PB[204]	AVI_INF_PB[203]	AVI_INF_PB[202]	AVI_INF_PB[201]	AVI_INF_PB[200]
0x1A	0x00	AVI_INF_PB_0_27	r	AVI_INF_PB[215]	AVI_INF_PB[214]	AVI_INF_PB[213]	AVI_INF_PB[212]	AVI_INF_PB[211]	AVI_INF_PB[210]	AVI_INF_PB[209]	AVI_INF_PB[208]
0x1B	0x00	AVI_INF_PB_0_28	r	AVI_INF_PB[223]	AVI_INF_PB[222]	AVI_INF_PB[221]	AVI_INF_PB[220]	AVI_INF_PB[219]	AVI_INF_PB[218]	AVI_INF_PB[217]	AVI_INF_PB[216]
0x1C	0x00	AUD_INF_PB_0_1	r	AUD_INF_PB[7]	AUD_INF_PB[6]	AUD_INF_PB[5]	AUD_INF_PB[4]	AUD_INF_PB[3]	AUD_INF_PB[2]	AUD_INF_PB[1]	AUD_INF_PB[0]
0x1D	0x00	AUD_INF_PB_0_2	r	AUD_INF_PB[15]	AUD_INF_PB[14]	AUD_INF_PB[13]	AUD_INF_PB[12]	AUD_INF_PB[11]	AUD_INF_PB[10]	AUD_INF_PB[9]	AUD_INF_PB[8]
0x1E	0x00	AUD_INF_PB_0_3	r	AUD_INF_PB[23]	AUD_INF_PB[22]	AUD_INF_PB[21]	AUD_INF_PB[20]	AUD_INF_PB[19]	AUD_INF_PB[18]	AUD_INF_PB[17]	AUD_INF_PB[16]
0x1F	0x00	AUD_INF_PB_0_4	r	AUD_INF_PB[31]	AUD_INF_PB[30]	AUD_INF_PB[29]	AUD_INF_PB[28]	AUD_INF_PB[27]	AUD_INF_PB[26]	AUD_INF_PB[25]	AUD_INF_PB[24]
0x20	0x00	AUD_INF_PB_0_5	r	AUD_INF_PB[39]	AUD_INF_PB[38]	AUD_INF_PB[37]	AUD_INF_PB[36]	AUD_INF_PB[35]	AUD_INF_PB[34]	AUD_INF_PB[33]	AUD_INF_PB[32]
0x21	0x00	AUD_INF_PB_0_6	r	AUD_INF_PB[47]	AUD_INF_PB[46]	AUD_INF_PB[45]	AUD_INF_PB[44]	AUD_INF_PB[43]	AUD_INF_PB[42]	AUD_INF_PB[41]	AUD_INF_PB[40]
0x22	0x00	AUD_INF_PB_0_7	r	AUD_INF_PB[55]	AUD_INF_PB[54]	AUD_INF_PB[53]	AUD_INF_PB[52]	AUD_INF_PB[51]	AUD_INF_PB[50]	AUD_INF_PB[49]	AUD_INF_PB[48]
0x23	0x00	AUD_INF_PB_0_8	r	AUD_INF_PB[63]	AUD_INF_PB[62]	AUD_INF_PB[61]	AUD_INF_PB[60]	AUD_INF_PB[59]	AUD_INF_PB[58]	AUD_INF_PB[57]	AUD_INF_PB[56]
0x24	0x00	AUD_INF_PB_0_9	r	AUD_INF_PB[71]	AUD_INF_PB[70]	AUD_INF_PB[69]	AUD_INF_PB[68]	AUD_INF_PB[67]	AUD_INF_PB[66]	AUD_INF_PB[65]	AUD_INF_PB[64]
0x25	0x00	AUD_INF_PB_0_10	r	AUD_INF_PB[79]	AUD_INF_PB[78]	AUD_INF_PB[77]	AUD_INF_PB[76]	AUD_INF_PB[75]	AUD_INF_PB[74]	AUD_INF_PB[73]	AUD_INF_PB[72]
0x26	0x00	AUD_INF_PB_0_11	r	AUD_INF_PB[87]	AUD_INF_PB[86]	AUD_INF_PB[85]	AUD_INF_PB[84]	AUD_INF_PB[83]	AUD_INF_PB[82]	AUD_INF_PB[81]	AUD_INF_PB[80]
0x27	0x00	AUD_INF_PB_0_12	r	AUD_INF_PB[95]	AUD_INF_PB[94]	AUD_INF_PB[93]	AUD_INF_PB[92]	AUD_INF_PB[91]	AUD_INF_PB[90]	AUD_INF_PB[89]	AUD_INF_PB[88]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x28	0x00	AUD_INF_PB_0_13	r	AUD_INF_PB[103]	AUD_INF_PB[102]	AUD_INF_PB[101]	AUD_INF_PB[100]	AUD_INF_PB[99]	AUD_INF_PB[98]	AUD_INF_PB[97]	AUD_INF_PB[96]
0x29	0x00	AUD_INF_PB_0_14	r	AUD_INF_PB[111]	AUD_INF_PB[110]	AUD_INF_PB[109]	AUD_INF_PB[108]	AUD_INF_PB[107]	AUD_INF_PB[106]	AUD_INF_PB[105]	AUD_INF_PB[104]
0x2A	0x00	SPD_INF_PB_0_1	r	SPD_INF_PB[7]	SPD_INF_PB[6]	SPD_INF_PB[5]	SPD_INF_PB[4]	SPD_INF_PB[3]	SPD_INF_PB[2]	SPD_INF_PB[1]	SPD_INF_PB[0]
0x2B	0x00	SPD_INF_PB_0_2	r	SPD_INF_PB[15]	SPD_INF_PB[14]	SPD_INF_PB[13]	SPD_INF_PB[12]	SPD_INF_PB[11]	SPD_INF_PB[10]	SPD_INF_PB[9]	SPD_INF_PB[8]
0x2C	0x00	SPD_INF_PB_0_3	r	SPD_INF_PB[23]	SPD_INF_PB[22]	SPD_INF_PB[21]	SPD_INF_PB[20]	SPD_INF_PB[19]	SPD_INF_PB[18]	SPD_INF_PB[17]	SPD_INF_PB[16]
0x2D	0x00	SPD_INF_PB_0_4	r	SPD_INF_PB[31]	SPD_INF_PB[30]	SPD_INF_PB[29]	SPD_INF_PB[28]	SPD_INF_PB[27]	SPD_INF_PB[26]	SPD_INF_PB[25]	SPD_INF_PB[24]
0x2E	0x00	SPD_INF_PB_0_5	r	SPD_INF_PB[39]	SPD_INF_PB[38]	SPD_INF_PB[37]	SPD_INF_PB[36]	SPD_INF_PB[35]	SPD_INF_PB[34]	SPD_INF_PB[33]	SPD_INF_PB[32]
0x2F	0x00	SPD_INF_PB_0_6	r	SPD_INF_PB[47]	SPD_INF_PB[46]	SPD_INF_PB[45]	SPD_INF_PB[44]	SPD_INF_PB[43]	SPD_INF_PB[42]	SPD_INF_PB[41]	SPD_INF_PB[40]
0x30	0x00	SPD_INF_PB_0_7	r	SPD_INF_PB[55]	SPD_INF_PB[54]	SPD_INF_PB[53]	SPD_INF_PB[52]	SPD_INF_PB[51]	SPD_INF_PB[50]	SPD_INF_PB[49]	SPD_INF_PB[48]
0x31	0x00	SPD_INF_PB_0_8	r	SPD_INF_PB[63]	SPD_INF_PB[62]	SPD_INF_PB[61]	SPD_INF_PB[60]	SPD_INF_PB[59]	SPD_INF_PB[58]	SPD_INF_PB[57]	SPD_INF_PB[56]
0x32	0x00	SPD_INF_PB_0_9	r	SPD_INF_PB[71]	SPD_INF_PB[70]	SPD_INF_PB[69]	SPD_INF_PB[68]	SPD_INF_PB[67]	SPD_INF_PB[66]	SPD_INF_PB[65]	SPD_INF_PB[64]
0x33	0x00	SPD_INF_PB_0_10	r	SPD_INF_PB[79]	SPD_INF_PB[78]	SPD_INF_PB[77]	SPD_INF_PB[76]	SPD_INF_PB[75]	SPD_INF_PB[74]	SPD_INF_PB[73]	SPD_INF_PB[72]
0x34	0x00	SPD_INF_PB_0_11	r	SPD_INF_PB[87]	SPD_INF_PB[86]	SPD_INF_PB[85]	SPD_INF_PB[84]	SPD_INF_PB[83]	SPD_INF_PB[82]	SPD_INF_PB[81]	SPD_INF_PB[80]
0x35	0x00	SPD_INF_PB_0_12	r	SPD_INF_PB[95]	SPD_INF_PB[94]	SPD_INF_PB[93]	SPD_INF_PB[92]	SPD_INF_PB[91]	SPD_INF_PB[90]	SPD_INF_PB[89]	SPD_INF_PB[88]
0x36	0x00	SPD_INF_PB_0_13	r	SPD_INF_PB[103]	SPD_INF_PB[102]	SPD_INF_PB[101]	SPD_INF_PB[100]	SPD_INF_PB[99]	SPD_INF_PB[98]	SPD_INF_PB[97]	SPD_INF_PB[96]
0x37	0x00	SPD_INF_PB_0_14	r	SPD_INF_PB[111]	SPD_INF_PB[110]	SPD_INF_PB[109]	SPD_INF_PB[108]	SPD_INF_PB[107]	SPD_INF_PB[106]	SPD_INF_PB[105]	SPD_INF_PB[104]
0x38	0x00	SPD_INF_PB_0_15	r	SPD_INF_PB[119]	SPD_INF_PB[118]	SPD_INF_PB[117]	SPD_INF_PB[116]	SPD_INF_PB[115]	SPD_INF_PB[114]	SPD_INF_PB[113]	SPD_INF_PB[112]
0x39	0x00	SPD_INF_PB_0_16	r	SPD_INF_PB[127]	SPD_INF_PB[126]	SPD_INF_PB[125]	SPD_INF_PB[124]	SPD_INF_PB[123]	SPD_INF_PB[122]	SPD_INF_PB[121]	SPD_INF_PB[120]
0x3A	0x00	SPD_INF_PB_0_17	r	SPD_INF_PB[135]	SPD_INF_PB[134]	SPD_INF_PB[133]	SPD_INF_PB[132]	SPD_INF_PB[131]	SPD_INF_PB[130]	SPD_INF_PB[129]	SPD_INF_PB[128]
0x3B	0x00	SPD_INF_PB_0_18	r	SPD_INF_PB[143]	SPD_INF_PB[142]	SPD_INF_PB[141]	SPD_INF_PB[140]	SPD_INF_PB[139]	SPD_INF_PB[138]	SPD_INF_PB[137]	SPD_INF_PB[136]
0x3C	0x00	SPD_INF_PB_0_19	r	SPD_INF_PB[151]	SPD_INF_PB[150]	SPD_INF_PB[149]	SPD_INF_PB[148]	SPD_INF_PB[147]	SPD_INF_PB[146]	SPD_INF_PB[145]	SPD_INF_PB[144]
0x3D	0x00	SPD_INF_PB_0_20	r	SPD_INF_PB[159]	SPD_INF_PB[158]	SPD_INF_PB[157]	SPD_INF_PB[156]	SPD_INF_PB[155]	SPD_INF_PB[154]	SPD_INF_PB[153]	SPD_INF_PB[152]
0x3E	0x00	SPD_INF_PB_0_21	r	SPD_INF_PB[167]	SPD_INF_PB[166]	SPD_INF_PB[165]	SPD_INF_PB[164]	SPD_INF_PB[163]	SPD_INF_PB[162]	SPD_INF_PB[161]	SPD_INF_PB[160]
0x3F	0x00	SPD_INF_PB_0_22	r	SPD_INF_PB[175]	SPD_INF_PB[174]	SPD_INF_PB[173]	SPD_INF_PB[172]	SPD_INF_PB[171]	SPD_INF_PB[170]	SPD_INF_PB[169]	SPD_INF_PB[168]
0x40	0x00	SPD_INF_PB_0_23	r	SPD_INF_PB[183]	SPD_INF_PB[182]	SPD_INF_PB[181]	SPD_INF_PB[180]	SPD_INF_PB[179]	SPD_INF_PB[178]	SPD_INF_PB[177]	SPD_INF_PB[176]
0x41	0x00	SPD_INF_PB_0_24	r	SPD_INF_PB[191]	SPD_INF_PB[190]	SPD_INF_PB[189]	SPD_INF_PB[188]	SPD_INF_PB[187]	SPD_INF_PB[186]	SPD_INF_PB[185]	SPD_INF_PB[184]
0x42	0x00	SPD_INF_PB_0_25	r	SPD_INF_PB[199]	SPD_INF_PB[198]	SPD_INF_PB[197]	SPD_INF_PB[196]	SPD_INF_PB[195]	SPD_INF_PB[194]	SPD_INF_PB[193]	SPD_INF_PB[192]
0x43	0x00	SPD_INF_PB_0_26	r	SPD_INF_PB[207]	SPD_INF_PB[206]	SPD_INF_PB[205]	SPD_INF_PB[204]	SPD_INF_PB[203]	SPD_INF_PB[202]	SPD_INF_PB[201]	SPD_INF_PB[200]
0x44	0x00	SPD_INF_PB_0_27	r	SPD_INF_PB[215]	SPD_INF_PB[214]	SPD_INF_PB[213]	SPD_INF_PB[212]	SPD_INF_PB[211]	SPD_INF_PB[210]	SPD_INF_PB[209]	SPD_INF_PB[208]
0x45	0x00	SPD_INF_PB_0_28	r	SPD_INF_PB[223]	SPD_INF_PB[222]	SPD_INF_PB[221]	SPD_INF_PB[220]	SPD_INF_PB[219]	SPD_INF_PB[218]	SPD_INF_PB[217]	SPD_INF_PB[216]
0x46	0x00	MS_INF_PB_0_1	r	MS_INF_PB[7]	MS_INF_PB[6]	MS_INF_PB[5]	MS_INF_PB[4]	MS_INF_PB[3]	MS_INF_PB[2]	MS_INF_PB[1]	MS_INF_PB[0]
0x47	0x00	MS_INF_PB_0_2	r	MS_INF_PB[15]	MS_INF_PB[14]	MS_INF_PB[13]	MS_INF_PB[12]	MS_INF_PB[11]	MS_INF_PB[10]	MS_INF_PB[9]	MS_INF_PB[8]
0x48	0x00	MS_INF_PB_0_3	r	MS_INF_PB[23]	MS_INF_PB[22]	MS_INF_PB[21]	MS_INF_PB[20]	MS_INF_PB[19]	MS_INF_PB[18]	MS_INF_PB[17]	MS_INF_PB[16]
0x49	0x00	MS_INF_PB_0_4	r	MS_INF_PB[31]	MS_INF_PB[30]	MS_INF_PB[29]	MS_INF_PB[28]	MS_INF_PB[27]	MS_INF_PB[26]	MS_INF_PB[25]	MS_INF_PB[24]
0x4A	0x00	MS_INF_PB_0_5	r	MS_INF_PB[39]	MS_INF_PB[38]	MS_INF_PB[37]	MS_INF_PB[36]	MS_INF_PB[35]	MS_INF_PB[34]	MS_INF_PB[33]	MS_INF_PB[32]
0x4B	0x00	MS_INF_PB_0_6	r	MS_INF_PB[47]	MS_INF_PB[46]	MS_INF_PB[45]	MS_INF_PB[44]	MS_INF_PB[43]	MS_INF_PB[42]	MS_INF_PB[41]	MS_INF_PB[40]
0x4C	0x00	MS_INF_PB_0_7	r	MS_INF_PB[55]	MS_INF_PB[54]	MS_INF_PB[53]	MS_INF_PB[52]	MS_INF_PB[51]	MS_INF_PB[50]	MS_INF_PB[49]	MS_INF_PB[48]
0x4D	0x00	MS_INF_PB_0_8	r	MS_INF_PB[63]	MS_INF_PB[62]	MS_INF_PB[61]	MS_INF_PB[60]	MS_INF_PB[59]	MS_INF_PB[58]	MS_INF_PB[57]	MS_INF_PB[56]
0x4E	0x00	MS_INF_PB_0_9	r	MS_INF_PB[71]	MS_INF_PB[70]	MS_INF_PB[69]	MS_INF_PB[68]	MS_INF_PB[67]	MS_INF_PB[66]	MS_INF_PB[65]	MS_INF_PB[64]
0x4F	0x00	MS_INF_PB_0_10	r	MS_INF_PB[79]	MS_INF_PB[78]	MS_INF_PB[77]	MS_INF_PB[76]	MS_INF_PB[75]	MS_INF_PB[74]	MS_INF_PB[73]	MS_INF_PB[72]
0x50	0x00	MS_INF_PB_0_11	r	MS_INF_PB[87]	MS_INF_PB[86]	MS_INF_PB[85]	MS_INF_PB[84]	MS_INF_PB[83]	MS_INF_PB[82]	MS_INF_PB[81]	MS_INF_PB[80]
0x51	0x00	MS_INF_PB_0_12	r	MS_INF_PB[95]	MS_INF_PB[94]	MS_INF_PB[93]	MS_INF_PB[92]	MS_INF_PB[91]	MS_INF_PB[90]	MS_INF_PB[89]	MS_INF_PB[88]
0x52	0x00	MS_INF_PB_0_13	r	MS_INF_PB[103]	MS_INF_PB[102]	MS_INF_PB[101]	MS_INF_PB[100]	MS_INF_PB[99]	MS_INF_PB[98]	MS_INF_PB[97]	MS_INF_PB[96]
0x53	0x00	MS_INF_PB_0_14	r	MS_INF_PB[111]	MS_INF_PB[110]	MS_INF_PB[109]	MS_INF_PB[108]	MS_INF_PB[107]	MS_INF_PB[106]	MS_INF_PB[105]	MS_INF_PB[104]
0x54	0x00	VS_INF_PB_0_1	r	VS_INF_PB[7]	VS_INF_PB[6]	VS_INF_PB[5]	VS_INF_PB[4]	VS_INF_PB[3]	VS_INF_PB[2]	VS_INF_PB[1]	VS_INF_PB[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x55	0x00	VS_INF_PB_0_2	r	VS_INF_PB[15]	VS_INF_PB[14]	VS_INF_PB[13]	VS_INF_PB[12]	VS_INF_PB[11]	VS_INF_PB[10]	VS_INF_PB[9]	VS_INF_PB[8]
0x56	0x00	VS_INF_PB_0_3	r	VS_INF_PB[23]	VS_INF_PB[22]	VS_INF_PB[21]	VS_INF_PB[20]	VS_INF_PB[19]	VS_INF_PB[18]	VS_INF_PB[17]	VS_INF_PB[16]
0x57	0x00	VS_INF_PB_0_4	r	VS_INF_PB[31]	VS_INF_PB[30]	VS_INF_PB[29]	VS_INF_PB[28]	VS_INF_PB[27]	VS_INF_PB[26]	VS_INF_PB[25]	VS_INF_PB[24]
0x58	0x00	VS_INF_PB_0_5	r	VS_INF_PB[39]	VS_INF_PB[38]	VS_INF_PB[37]	VS_INF_PB[36]	VS_INF_PB[35]	VS_INF_PB[34]	VS_INF_PB[33]	VS_INF_PB[32]
0x59	0x00	VS_INF_PB_0_6	r	VS_INF_PB[47]	VS_INF_PB[46]	VS_INF_PB[45]	VS_INF_PB[44]	VS_INF_PB[43]	VS_INF_PB[42]	VS_INF_PB[41]	VS_INF_PB[40]
0x5A	0x00	VS_INF_PB_0_7	r	VS_INF_PB[55]	VS_INF_PB[54]	VS_INF_PB[53]	VS_INF_PB[52]	VS_INF_PB[51]	VS_INF_PB[50]	VS_INF_PB[49]	VS_INF_PB[48]
0x5B	0x00	VS_INF_PB_0_8	r	VS_INF_PB[63]	VS_INF_PB[62]	VS_INF_PB[61]	VS_INF_PB[60]	VS_INF_PB[59]	VS_INF_PB[58]	VS_INF_PB[57]	VS_INF_PB[56]
0x5C	0x00	VS_INF_PB_0_9	r	VS_INF_PB[71]	VS_INF_PB[70]	VS_INF_PB[69]	VS_INF_PB[68]	VS_INF_PB[67]	VS_INF_PB[66]	VS_INF_PB[65]	VS_INF_PB[64]
0x5D	0x00	VS_INF_PB_0_10	r	VS_INF_PB[79]	VS_INF_PB[78]	VS_INF_PB[77]	VS_INF_PB[76]	VS_INF_PB[75]	VS_INF_PB[74]	VS_INF_PB[73]	VS_INF_PB[72]
0x5E	0x00	VS_INF_PB_0_11	r	VS_INF_PB[87]	VS_INF_PB[86]	VS_INF_PB[85]	VS_INF_PB[84]	VS_INF_PB[83]	VS_INF_PB[82]	VS_INF_PB[81]	VS_INF_PB[80]
0x5F	0x00	VS_INF_PB_0_12	r	VS_INF_PB[95]	VS_INF_PB[94]	VS_INF_PB[93]	VS_INF_PB[92]	VS_INF_PB[91]	VS_INF_PB[90]	VS_INF_PB[89]	VS_INF_PB[88]
0x60	0x00	VS_INF_PB_0_13	r	VS_INF_PB[103]	VS_INF_PB[102]	VS_INF_PB[101]	VS_INF_PB[100]	VS_INF_PB[99]	VS_INF_PB[98]	VS_INF_PB[97]	VS_INF_PB[96]
0x61	0x00	VS_INF_PB_0_14	r	VS_INF_PB[111]	VS_INF_PB[110]	VS_INF_PB[109]	VS_INF_PB[108]	VS_INF_PB[107]	VS_INF_PB[106]	VS_INF_PB[105]	VS_INF_PB[104]
0x62	0x00	VS_INF_PB_0_15	r	VS_INF_PB[119]	VS_INF_PB[118]	VS_INF_PB[117]	VS_INF_PB[116]	VS_INF_PB[115]	VS_INF_PB[114]	VS_INF_PB[113]	VS_INF_PB[112]
0x63	0x00	VS_INF_PB_0_16	r	VS_INF_PB[127]	VS_INF_PB[126]	VS_INF_PB[125]	VS_INF_PB[124]	VS_INF_PB[123]	VS_INF_PB[122]	VS_INF_PB[121]	VS_INF_PB[120]
0x64	0x00	VS_INF_PB_0_17	r	VS_INF_PB[135]	VS_INF_PB[134]	VS_INF_PB[133]	VS_INF_PB[132]	VS_INF_PB[131]	VS_INF_PB[130]	VS_INF_PB[129]	VS_INF_PB[128]
0x65	0x00	VS_INF_PB_0_18	r	VS_INF_PB[143]	VS_INF_PB[142]	VS_INF_PB[141]	VS_INF_PB[140]	VS_INF_PB[139]	VS_INF_PB[138]	VS_INF_PB[137]	VS_INF_PB[136]
0x66	0x00	VS_INF_PB_0_19	r	VS_INF_PB[151]	VS_INF_PB[150]	VS_INF_PB[149]	VS_INF_PB[148]	VS_INF_PB[147]	VS_INF_PB[146]	VS_INF_PB[145]	VS_INF_PB[144]
0x67	0x00	VS_INF_PB_0_20	r	VS_INF_PB[159]	VS_INF_PB[158]	VS_INF_PB[157]	VS_INF_PB[156]	VS_INF_PB[155]	VS_INF_PB[154]	VS_INF_PB[153]	VS_INF_PB[152]
0x68	0x00	VS_INF_PB_0_21	r	VS_INF_PB[167]	VS_INF_PB[166]	VS_INF_PB[165]	VS_INF_PB[164]	VS_INF_PB[163]	VS_INF_PB[162]	VS_INF_PB[161]	VS_INF_PB[160]
0x69	0x00	VS_INF_PB_0_22	r	VS_INF_PB[175]	VS_INF_PB[174]	VS_INF_PB[173]	VS_INF_PB[172]	VS_INF_PB[171]	VS_INF_PB[170]	VS_INF_PB[169]	VS_INF_PB[168]
0x6A	0x00	VS_INF_PB_0_23	r	VS_INF_PB[183]	VS_INF_PB[182]	VS_INF_PB[181]	VS_INF_PB[180]	VS_INF_PB[179]	VS_INF_PB[178]	VS_INF_PB[177]	VS_INF_PB[176]
0x6B	0x00	VS_INF_PB_0_24	r	VS_INF_PB[191]	VS_INF_PB[190]	VS_INF_PB[189]	VS_INF_PB[188]	VS_INF_PB[187]	VS_INF_PB[186]	VS_INF_PB[185]	VS_INF_PB[184]
0x6C	0x00	VS_INF_PB_0_25	r	VS_INF_PB[199]	VS_INF_PB[198]	VS_INF_PB[197]	VS_INF_PB[196]	VS_INF_PB[195]	VS_INF_PB[194]	VS_INF_PB[193]	VS_INF_PB[192]
0x6D	0x00	VS_INF_PB_0_26	r	VS_INF_PB[207]	VS_INF_PB[206]	VS_INF_PB[205]	VS_INF_PB[204]	VS_INF_PB[203]	VS_INF_PB[202]	VS_INF_PB[201]	VS_INF_PB[200]
0x6E	0x00	VS_INF_PB_0_27	r	VS_INF_PB[215]	VS_INF_PB[214]	VS_INF_PB[213]	VS_INF_PB[212]	VS_INF_PB[211]	VS_INF_PB[210]	VS_INF_PB[209]	VS_INF_PB[208]
0x6F	0x00	VS_INF_PB_0_28	r	VS_INF_PB[223]	VS_INF_PB[222]	VS_INF_PB[221]	VS_INF_PB[220]	VS_INF_PB[219]	VS_INF_PB[218]	VS_INF_PB[217]	VS_INF_PB[216]
0x70	0x00	ACP_PB_0_1	r	ACP_PB[7]	ACP_PB[6]	ACP_PB[5]	ACP_PB[4]	ACP_PB[3]	ACP_PB[2]	ACP_PB[1]	ACP_PB[0]
0x71	0x00	ACP_PB_0_2	r	ACP_PB[15]	ACP_PB[14]	ACP_PB[13]	ACP_PB[12]	ACP_PB[11]	ACP_PB[10]	ACP_PB[9]	ACP_PB[8]
0x72	0x00	ACP_PB_0_3	r	ACP_PB[23]	ACP_PB[22]	ACP_PB[21]	ACP_PB[20]	ACP_PB[19]	ACP_PB[18]	ACP_PB[17]	ACP_PB[16]
0x73	0x00	ACP_PB_0_4	r	ACP_PB[31]	ACP_PB[30]	ACP_PB[29]	ACP_PB[28]	ACP_PB[27]	ACP_PB[26]	ACP_PB[25]	ACP_PB[24]
0x74	0x00	ACP_PB_0_5	r	ACP_PB[39]	ACP_PB[38]	ACP_PB[37]	ACP_PB[36]	ACP_PB[35]	ACP_PB[34]	ACP_PB[33]	ACP_PB[32]
0x75	0x00	ACP_PB_0_6	r	ACP_PB[47]	ACP_PB[46]	ACP_PB[45]	ACP_PB[44]	ACP_PB[43]	ACP_PB[42]	ACP_PB[41]	ACP_PB[40]
0x76	0x00	ACP_PB_0_7	r	ACP_PB[55]	ACP_PB[54]	ACP_PB[53]	ACP_PB[52]	ACP_PB[51]	ACP_PB[50]	ACP_PB[49]	ACP_PB[48]
0x77	0x00	ACP_PB_0_8	r	ACP_PB[63]	ACP_PB[62]	ACP_PB[61]	ACP_PB[60]	ACP_PB[59]	ACP_PB[58]	ACP_PB[57]	ACP_PB[56]
0x78	0x00	ACP_PB_0_9	r	ACP_PB[71]	ACP_PB[70]	ACP_PB[69]	ACP_PB[68]	ACP_PB[67]	ACP_PB[66]	ACP_PB[65]	ACP_PB[64]
0x79	0x00	ACP_PB_0_10	r	ACP_PB[79]	ACP_PB[78]	ACP_PB[77]	ACP_PB[76]	ACP_PB[75]	ACP_PB[74]	ACP_PB[73]	ACP_PB[72]
0x7A	0x00	ACP_PB_0_11	r	ACP_PB[87]	ACP_PB[86]	ACP_PB[85]	ACP_PB[84]	ACP_PB[83]	ACP_PB[82]	ACP_PB[81]	ACP_PB[80]
0x7B	0x00	ACP_PB_0_12	r	ACP_PB[95]	ACP_PB[94]	ACP_PB[93]	ACP_PB[92]	ACP_PB[91]	ACP_PB[90]	ACP_PB[89]	ACP_PB[88]
0x7C	0x00	ACP_PB_0_13	r	ACP_PB[103]	ACP_PB[102]	ACP_PB[101]	ACP_PB[100]	ACP_PB[99]	ACP_PB[98]	ACP_PB[97]	ACP_PB[96]
0x7D	0x00	ACP_PB_0_14	r	ACP_PB[111]	ACP_PB[110]	ACP_PB[109]	ACP_PB[108]	ACP_PB[107]	ACP_PB[106]	ACP_PB[105]	ACP_PB[104]
0x7E	0x00	ACP_PB_0_15	r	ACP_PB[119]	ACP_PB[118]	ACP_PB[117]	ACP_PB[116]	ACP_PB[115]	ACP_PB[114]	ACP_PB[113]	ACP_PB[112]
0x7F	0x00	ACP_PB_0_16	r	ACP_PB[127]	ACP_PB[126]	ACP_PB[125]	ACP_PB[124]	ACP_PB[123]	ACP_PB[122]	ACP_PB[121]	ACP_PB[120]
0x80	0x00	ACP_PB_0_17	r	ACP_PB[135]	ACP_PB[134]	ACP_PB[133]	ACP_PB[132]	ACP_PB[131]	ACP_PB[130]	ACP_PB[129]	ACP_PB[128]
0x81	0x00	ACP_PB_0_18	r	ACP_PB[143]	ACP_PB[142]	ACP_PB[141]	ACP_PB[140]	ACP_PB[139]	ACP_PB[138]	ACP_PB[137]	ACP_PB[136]
0x82	0x00	ACP_PB_0_19	r	ACP_PB[151]	ACP_PB[150]	ACP_PB[149]	ACP_PB[148]	ACP_PB[147]	ACP_PB[146]	ACP_PB[145]	ACP_PB[144]
0x83	0x00	ACP_PB_0_20	r	ACP_PB[159]	ACP_PB[158]	ACP_PB[157]	ACP_PB[156]	ACP_PB[155]	ACP_PB[154]	ACP_PB[153]	ACP_PB[152]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x84	0x00	ACP_PB_0_21	r	ACP_PB[167]	ACP_PB[166]	ACP_PB[165]	ACP_PB[164]	ACP_PB[163]	ACP_PB[162]	ACP_PB[161]	ACP_PB[160]
0x85	0x00	ACP_PB_0_22	r	ACP_PB[175]	ACP_PB[174]	ACP_PB[173]	ACP_PB[172]	ACP_PB[171]	ACP_PB[170]	ACP_PB[169]	ACP_PB[168]
0x86	0x00	ACP_PB_0_23	r	ACP_PB[183]	ACP_PB[182]	ACP_PB[181]	ACP_PB[180]	ACP_PB[179]	ACP_PB[178]	ACP_PB[177]	ACP_PB[176]
0x87	0x00	ACP_PB_0_24	r	ACP_PB[191]	ACP_PB[190]	ACP_PB[189]	ACP_PB[188]	ACP_PB[187]	ACP_PB[186]	ACP_PB[185]	ACP_PB[184]
0x88	0x00	ACP_PB_0_25	r	ACP_PB[199]	ACP_PB[198]	ACP_PB[197]	ACP_PB[196]	ACP_PB[195]	ACP_PB[194]	ACP_PB[193]	ACP_PB[192]
0x89	0x00	ACP_PB_0_26	r	ACP_PB[207]	ACP_PB[206]	ACP_PB[205]	ACP_PB[204]	ACP_PB[203]	ACP_PB[202]	ACP_PB[201]	ACP_PB[200]
0x8A	0x00	ACP_PB_0_27	r	ACP_PB[215]	ACP_PB[214]	ACP_PB[213]	ACP_PB[212]	ACP_PB[211]	ACP_PB[210]	ACP_PB[209]	ACP_PB[208]
0x8B	0x00	ACP_PB_0_28	r	ACP_PB[223]	ACP_PB[222]	ACP_PB[221]	ACP_PB[220]	ACP_PB[219]	ACP_PB[218]	ACP_PB[217]	ACP_PB[216]
0x8C	0x00	ISRC1_PB_0_1	r	ISRC1_PB[7]	ISRC1_PB[6]	ISRC1_PB[5]	ISRC1_PB[4]	ISRC1_PB[3]	ISRC1_PB[2]	ISRC1_PB[1]	ISRC1_PB[0]
0x8D	0x00	ISRC1_PB_0_2	r	ISRC1_PB[15]	ISRC1_PB[14]	ISRC1_PB[13]	ISRC1_PB[12]	ISRC1_PB[11]	ISRC1_PB[10]	ISRC1_PB[9]	ISRC1_PB[8]
0x8E	0x00	ISRC1_PB_0_3	r	ISRC1_PB[23]	ISRC1_PB[22]	ISRC1_PB[21]	ISRC1_PB[20]	ISRC1_PB[19]	ISRC1_PB[18]	ISRC1_PB[17]	ISRC1_PB[16]
0x8F	0x00	ISRC1_PB_0_4	r	ISRC1_PB[31]	ISRC1_PB[30]	ISRC1_PB[29]	ISRC1_PB[28]	ISRC1_PB[27]	ISRC1_PB[26]	ISRC1_PB[25]	ISRC1_PB[24]
0x90	0x00	ISRC1_PB_0_5	r	ISRC1_PB[39]	ISRC1_PB[38]	ISRC1_PB[37]	ISRC1_PB[36]	ISRC1_PB[35]	ISRC1_PB[34]	ISRC1_PB[33]	ISRC1_PB[32]
0x91	0x00	ISRC1_PB_0_6	r	ISRC1_PB[47]	ISRC1_PB[46]	ISRC1_PB[45]	ISRC1_PB[44]	ISRC1_PB[43]	ISRC1_PB[42]	ISRC1_PB[41]	ISRC1_PB[40]
0x92	0x00	ISRC1_PB_0_7	r	ISRC1_PB[55]	ISRC1_PB[54]	ISRC1_PB[53]	ISRC1_PB[52]	ISRC1_PB[51]	ISRC1_PB[50]	ISRC1_PB[49]	ISRC1_PB[48]
0x93	0x00	ISRC1_PB_0_8	r	ISRC1_PB[63]	ISRC1_PB[62]	ISRC1_PB[61]	ISRC1_PB[60]	ISRC1_PB[59]	ISRC1_PB[58]	ISRC1_PB[57]	ISRC1_PB[56]
0x94	0x00	ISRC1_PB_0_9	r	ISRC1_PB[71]	ISRC1_PB[70]	ISRC1_PB[69]	ISRC1_PB[68]	ISRC1_PB[67]	ISRC1_PB[66]	ISRC1_PB[65]	ISRC1_PB[64]
0x95	0x00	ISRC1_PB_0_10	r	ISRC1_PB[79]	ISRC1_PB[78]	ISRC1_PB[77]	ISRC1_PB[76]	ISRC1_PB[75]	ISRC1_PB[74]	ISRC1_PB[73]	ISRC1_PB[72]
0x96	0x00	ISRC1_PB_0_11	r	ISRC1_PB[87]	ISRC1_PB[86]	ISRC1_PB[85]	ISRC1_PB[84]	ISRC1_PB[83]	ISRC1_PB[82]	ISRC1_PB[81]	ISRC1_PB[80]
0x97	0x00	ISRC1_PB_0_12	r	ISRC1_PB[95]	ISRC1_PB[94]	ISRC1_PB[93]	ISRC1_PB[92]	ISRC1_PB[91]	ISRC1_PB[90]	ISRC1_PB[89]	ISRC1_PB[88]
0x98	0x00	ISRC1_PB_0_13	r	ISRC1_PB[103]	ISRC1_PB[102]	ISRC1_PB[101]	ISRC1_PB[100]	ISRC1_PB[99]	ISRC1_PB[98]	ISRC1_PB[97]	ISRC1_PB[96]
0x99	0x00	ISRC1_PB_0_14	r	ISRC1_PB[111]	ISRC1_PB[110]	ISRC1_PB[109]	ISRC1_PB[108]	ISRC1_PB[107]	ISRC1_PB[106]	ISRC1_PB[105]	ISRC1_PB[104]
0x9A	0x00	ISRC1_PB_0_15	r	ISRC1_PB[119]	ISRC1_PB[118]	ISRC1_PB[117]	ISRC1_PB[116]	ISRC1_PB[115]	ISRC1_PB[114]	ISRC1_PB[113]	ISRC1_PB[112]
0x9B	0x00	ISRC1_PB_0_16	r	ISRC1_PB[127]	ISRC1_PB[126]	ISRC1_PB[125]	ISRC1_PB[124]	ISRC1_PB[123]	ISRC1_PB[122]	ISRC1_PB[121]	ISRC1_PB[120]
0x9C	0x00	ISRC1_PB_0_17	r	ISRC1_PB[135]	ISRC1_PB[134]	ISRC1_PB[133]	ISRC1_PB[132]	ISRC1_PB[131]	ISRC1_PB[130]	ISRC1_PB[129]	ISRC1_PB[128]
0x9D	0x00	ISRC1_PB_0_18	r	ISRC1_PB[143]	ISRC1_PB[142]	ISRC1_PB[141]	ISRC1_PB[140]	ISRC1_PB[139]	ISRC1_PB[138]	ISRC1_PB[137]	ISRC1_PB[136]
0x9E	0x00	ISRC1_PB_0_19	r	ISRC1_PB[151]	ISRC1_PB[150]	ISRC1_PB[149]	ISRC1_PB[148]	ISRC1_PB[147]	ISRC1_PB[146]	ISRC1_PB[145]	ISRC1_PB[144]
0x9F	0x00	ISRC1_PB_0_20	r	ISRC1_PB[159]	ISRC1_PB[158]	ISRC1_PB[157]	ISRC1_PB[156]	ISRC1_PB[155]	ISRC1_PB[154]	ISRC1_PB[153]	ISRC1_PB[152]
0xA0	0x00	ISRC1_PB_0_21	r	ISRC1_PB[167]	ISRC1_PB[166]	ISRC1_PB[165]	ISRC1_PB[164]	ISRC1_PB[163]	ISRC1_PB[162]	ISRC1_PB[161]	ISRC1_PB[160]
0xA1	0x00	ISRC1_PB_0_22	r	ISRC1_PB[175]	ISRC1_PB[174]	ISRC1_PB[173]	ISRC1_PB[172]	ISRC1_PB[171]	ISRC1_PB[170]	ISRC1_PB[169]	ISRC1_PB[168]
0xA2	0x00	ISRC1_PB_0_23	r	ISRC1_PB[183]	ISRC1_PB[182]	ISRC1_PB[181]	ISRC1_PB[180]	ISRC1_PB[179]	ISRC1_PB[178]	ISRC1_PB[177]	ISRC1_PB[176]
0xA3	0x00	ISRC1_PB_0_24	r	ISRC1_PB[191]	ISRC1_PB[190]	ISRC1_PB[189]	ISRC1_PB[188]	ISRC1_PB[187]	ISRC1_PB[186]	ISRC1_PB[185]	ISRC1_PB[184]
0xA4	0x00	ISRC1_PB_0_25	r	ISRC1_PB[199]	ISRC1_PB[198]	ISRC1_PB[197]	ISRC1_PB[196]	ISRC1_PB[195]	ISRC1_PB[194]	ISRC1_PB[193]	ISRC1_PB[192]
0xA5	0x00	ISRC1_PB_0_26	r	ISRC1_PB[207]	ISRC1_PB[206]	ISRC1_PB[205]	ISRC1_PB[204]	ISRC1_PB[203]	ISRC1_PB[202]	ISRC1_PB[201]	ISRC1_PB[200]
0xA6	0x00	ISRC1_PB_0_27	r	ISRC1_PB[215]	ISRC1_PB[214]	ISRC1_PB[213]	ISRC1_PB[212]	ISRC1_PB[211]	ISRC1_PB[210]	ISRC1_PB[209]	ISRC1_PB[208]
0xA7	0x00	ISRC1_PB_0_28	r	ISRC1_PB[223]	ISRC1_PB[222]	ISRC1_PB[221]	ISRC1_PB[220]	ISRC1_PB[219]	ISRC1_PB[218]	ISRC1_PB[217]	ISRC1_PB[216]
0xA8	0x00	ISRC2_PB_0_1	r	ISRC2_PB[7]	ISRC2_PB[6]	ISRC2_PB[5]	ISRC2_PB[4]	ISRC2_PB[3]	ISRC2_PB[2]	ISRC2_PB[1]	ISRC2_PB[0]
0xA9	0x00	ISRC2_PB_0_2	r	ISRC2_PB[15]	ISRC2_PB[14]	ISRC2_PB[13]	ISRC2_PB[12]	ISRC2_PB[11]	ISRC2_PB[10]	ISRC2_PB[9]	ISRC2_PB[8]
0xAA	0x00	ISRC2_PB_0_3	r	ISRC2_PB[23]	ISRC2_PB[22]	ISRC2_PB[21]	ISRC2_PB[20]	ISRC2_PB[19]	ISRC2_PB[18]	ISRC2_PB[17]	ISRC2_PB[16]
0xAB	0x00	ISRC2_PB_0_4	r	ISRC2_PB[31]	ISRC2_PB[30]	ISRC2_PB[29]	ISRC2_PB[28]	ISRC2_PB[27]	ISRC2_PB[26]	ISRC2_PB[25]	ISRC2_PB[24]
0xAC	0x00	ISRC2_PB_0_5	r	ISRC2_PB[39]	ISRC2_PB[38]	ISRC2_PB[37]	ISRC2_PB[36]	ISRC2_PB[35]	ISRC2_PB[34]	ISRC2_PB[33]	ISRC2_PB[32]
0xAD	0x00	ISRC2_PB_0_6	r	ISRC2_PB[47]	ISRC2_PB[46]	ISRC2_PB[45]	ISRC2_PB[44]	ISRC2_PB[43]	ISRC2_PB[42]	ISRC2_PB[41]	ISRC2_PB[40]
0xAE	0x00	ISRC2_PB_0_7	r	ISRC2_PB[55]	ISRC2_PB[54]	ISRC2_PB[53]	ISRC2_PB[52]	ISRC2_PB[51]	ISRC2_PB[50]	ISRC2_PB[49]	ISRC2_PB[48]
0xAF	0x00	ISRC2_PB_0_8	r	ISRC2_PB[63]	ISRC2_PB[62]	ISRC2_PB[61]	ISRC2_PB[60]	ISRC2_PB[59]	ISRC2_PB[58]	ISRC2_PB[57]	ISRC2_PB[56]
0xB0	0x00	ISRC2_PB_0_9	r	ISRC2_PB[71]	ISRC2_PB[70]	ISRC2_PB[69]	ISRC2_PB[68]	ISRC2_PB[67]	ISRC2_PB[66]	ISRC2_PB[65]	ISRC2_PB[64]
0xB1	0x00	ISRC2_PB_0_10	r	ISRC2_PB[79]	ISRC2_PB[78]	ISRC2_PB[77]	ISRC2_PB[76]	ISRC2_PB[75]	ISRC2_PB[74]	ISRC2_PB[73]	ISRC2_PB[72]
0xB2	0x00	ISRC2_PB_0_11	r	ISRC2_PB[87]	ISRC2_PB[86]	ISRC2_PB[85]	ISRC2_PB[84]	ISRC2_PB[83]	ISRC2_PB[82]	ISRC2_PB[81]	ISRC2_PB[80]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB3	0x00	ISRC2_PB_0_12	r	ISRC2_PB[95]	ISRC2_PB[94]	ISRC2_PB[93]	ISRC2_PB[92]	ISRC2_PB[91]	ISRC2_PB[90]	ISRC2_PB[89]	ISRC2_PB[88]
0xB4	0x00	ISRC2_PB_0_13	r	ISRC2_PB[103]	ISRC2_PB[102]	ISRC2_PB[101]	ISRC2_PB[100]	ISRC2_PB[99]	ISRC2_PB[98]	ISRC2_PB[97]	ISRC2_PB[96]
0xB5	0x00	ISRC2_PB_0_14	r	ISRC2_PB[111]	ISRC2_PB[110]	ISRC2_PB[109]	ISRC2_PB[108]	ISRC2_PB[107]	ISRC2_PB[106]	ISRC2_PB[105]	ISRC2_PB[104]
0xB6	0x00	ISRC2_PB_0_15	r	ISRC2_PB[119]	ISRC2_PB[118]	ISRC2_PB[117]	ISRC2_PB[116]	ISRC2_PB[115]	ISRC2_PB[114]	ISRC2_PB[113]	ISRC2_PB[112]
0xB7	0x00	ISRC2_PB_0_16	r	ISRC2_PB[127]	ISRC2_PB[126]	ISRC2_PB[125]	ISRC2_PB[124]	ISRC2_PB[123]	ISRC2_PB[122]	ISRC2_PB[121]	ISRC2_PB[120]
0xB8	0x00	ISRC2_PB_0_17	r	ISRC2_PB[135]	ISRC2_PB[134]	ISRC2_PB[133]	ISRC2_PB[132]	ISRC2_PB[131]	ISRC2_PB[130]	ISRC2_PB[129]	ISRC2_PB[128]
0xB9	0x00	ISRC2_PB_0_18	r	ISRC2_PB[143]	ISRC2_PB[142]	ISRC2_PB[141]	ISRC2_PB[140]	ISRC2_PB[139]	ISRC2_PB[138]	ISRC2_PB[137]	ISRC2_PB[136]
0xBA	0x00	ISRC2_PB_0_19	r	ISRC2_PB[151]	ISRC2_PB[150]	ISRC2_PB[149]	ISRC2_PB[148]	ISRC2_PB[147]	ISRC2_PB[146]	ISRC2_PB[145]	ISRC2_PB[144]
0xBB	0x00	ISRC2_PB_0_20	r	ISRC2_PB[159]	ISRC2_PB[158]	ISRC2_PB[157]	ISRC2_PB[156]	ISRC2_PB[155]	ISRC2_PB[154]	ISRC2_PB[153]	ISRC2_PB[152]
0xBC	0x00	ISRC2_PB_0_21	r	ISRC2_PB[167]	ISRC2_PB[166]	ISRC2_PB[165]	ISRC2_PB[164]	ISRC2_PB[163]	ISRC2_PB[162]	ISRC2_PB[161]	ISRC2_PB[160]
0xBD	0x00	ISRC2_PB_0_22	r	ISRC2_PB[175]	ISRC2_PB[174]	ISRC2_PB[173]	ISRC2_PB[172]	ISRC2_PB[171]	ISRC2_PB[170]	ISRC2_PB[169]	ISRC2_PB[168]
0xBE	0x00	ISRC2_PB_0_23	r	ISRC2_PB[183]	ISRC2_PB[182]	ISRC2_PB[181]	ISRC2_PB[180]	ISRC2_PB[179]	ISRC2_PB[178]	ISRC2_PB[177]	ISRC2_PB[176]
0xBF	0x00	ISRC2_PB_0_24	r	ISRC2_PB[191]	ISRC2_PB[190]	ISRC2_PB[189]	ISRC2_PB[188]	ISRC2_PB[187]	ISRC2_PB[186]	ISRC2_PB[185]	ISRC2_PB[184]
0xC0	0x00	ISRC2_PB_0_25	r	ISRC2_PB[199]	ISRC2_PB[198]	ISRC2_PB[197]	ISRC2_PB[196]	ISRC2_PB[195]	ISRC2_PB[194]	ISRC2_PB[193]	ISRC2_PB[192]
0xC1	0x00	ISRC2_PB_0_26	r	ISRC2_PB[207]	ISRC2_PB[206]	ISRC2_PB[205]	ISRC2_PB[204]	ISRC2_PB[203]	ISRC2_PB[202]	ISRC2_PB[201]	ISRC2_PB[200]
0xC2	0x00	ISRC2_PB_0_27	r	ISRC2_PB[215]	ISRC2_PB[214]	ISRC2_PB[213]	ISRC2_PB[212]	ISRC2_PB[211]	ISRC2_PB[210]	ISRC2_PB[209]	ISRC2_PB[208]
0xC3	0x00	ISRC2_PB_0_28	r	ISRC2_PB[223]	ISRC2_PB[222]	ISRC2_PB[221]	ISRC2_PB[220]	ISRC2_PB[219]	ISRC2_PB[218]	ISRC2_PB[217]	ISRC2_PB[216]
0xC4	0x00	GAMUT_MDATA_PB_0_1	r	GBD[7]	GBD[6]	GBD[5]	GBD[4]	GBD[3]	GBD[2]	GBD[1]	GBD[0]
0xC5	0x00	GAMUT_MDATA_PB_0_2	r	GBD[15]	GBD[14]	GBD[13]	GBD[12]	GBD[11]	GBD[10]	GBD[9]	GBD[8]
0xC6	0x00	GAMUT_MDATA_PB_0_3	r	GBD[23]	GBD[22]	GBD[21]	GBD[20]	GBD[19]	GBD[18]	GBD[17]	GBD[16]
0xC7	0x00	GAMUT_MDATA_PB_0_4	r	GBD[31]	GBD[30]	GBD[29]	GBD[28]	GBD[27]	GBD[26]	GBD[25]	GBD[24]
0xC8	0x00	GAMUT_MDATA_PB_0_5	r	GBD[39]	GBD[38]	GBD[37]	GBD[36]	GBD[35]	GBD[34]	GBD[33]	GBD[32]
0xC9	0x00	GAMUT_MDATA_PB_0_6	r	GBD[47]	GBD[46]	GBD[45]	GBD[44]	GBD[43]	GBD[42]	GBD[41]	GBD[40]
0xCA	0x00	GAMUT_MDATA_PB_0_7	r	GBD[55]	GBD[54]	GBD[53]	GBD[52]	GBD[51]	GBD[50]	GBD[49]	GBD[48]
0xCB	0x00	GAMUT_MDATA_PB_0_8	r	GBD[63]	GBD[62]	GBD[61]	GBD[60]	GBD[59]	GBD[58]	GBD[57]	GBD[56]
0xCC	0x00	GAMUT_MDATA_PB_0_9	r	GBD[71]	GBD[70]	GBD[69]	GBD[68]	GBD[67]	GBD[66]	GBD[65]	GBD[64]
0xCD	0x00	GAMUT_MDATA_PB_0_10	r	GBD[79]	GBD[78]	GBD[77]	GBD[76]	GBD[75]	GBD[74]	GBD[73]	GBD[72]
0xCE	0x00	GAMUT_MDATA_PB_0_11	r	GBD[87]	GBD[86]	GBD[85]	GBD[84]	GBD[83]	GBD[82]	GBD[81]	GBD[80]
0xCF	0x00	GAMUT_MDATA_PB_0_12	r	GBD[95]	GBD[94]	GBD[93]	GBD[92]	GBD[91]	GBD[90]	GBD[89]	GBD[88]
0xD0	0x00	GAMUT_MDATA_PB_0_13	r	GBD[103]	GBD[102]	GBD[101]	GBD[100]	GBD[99]	GBD[98]	GBD[97]	GBD[96]
0xD1	0x00	GAMUT_MDATA_PB_0_14	r	GBD[111]	GBD[110]	GBD[109]	GBD[108]	GBD[107]	GBD[106]	GBD[105]	GBD[104]
0xD2	0x00	GAMUT_MDATA_PB_0_15	r	GBD[119]	GBD[118]	GBD[117]	GBD[116]	GBD[115]	GBD[114]	GBD[113]	GBD[112]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xD3	0x00	GAMUT_MDATA_PB_0_16	r	GBD[127]	GBD[126]	GBD[125]	GBD[124]	GBD[123]	GBD[122]	GBD[121]	GBD[120]
0xD4	0x00	GAMUT_MDATA_PB_0_17	r	GBD[135]	GBD[134]	GBD[133]	GBD[132]	GBD[131]	GBD[130]	GBD[129]	GBD[128]
0xD5	0x00	GAMUT_MDATA_PB_0_18	r	GBD[143]	GBD[142]	GBD[141]	GBD[140]	GBD[139]	GBD[138]	GBD[137]	GBD[136]
0xD6	0x00	GAMUT_MDATA_PB_0_19	r	GBD[151]	GBD[150]	GBD[149]	GBD[148]	GBD[147]	GBD[146]	GBD[145]	GBD[144]
0xD7	0x00	GAMUT_MDATA_PB_0_20	r	GBD[159]	GBD[158]	GBD[157]	GBD[156]	GBD[155]	GBD[154]	GBD[153]	GBD[152]
0xD8	0x00	GAMUT_MDATA_PB_0_21	r	GBD[167]	GBD[166]	GBD[165]	GBD[164]	GBD[163]	GBD[162]	GBD[161]	GBD[160]
0xD9	0x00	GAMUT_MDATA_PB_0_22	r	GBD[175]	GBD[174]	GBD[173]	GBD[172]	GBD[171]	GBD[170]	GBD[169]	GBD[168]
0xDA	0x00	GAMUT_MDATA_PB_0_23	r	GBD[183]	GBD[182]	GBD[181]	GBD[180]	GBD[179]	GBD[178]	GBD[177]	GBD[176]
0xDB	0x00	GAMUT_MDATA_PB_0_24	r	GBD[191]	GBD[190]	GBD[189]	GBD[188]	GBD[187]	GBD[186]	GBD[185]	GBD[184]
0xDC	0x00	GAMUT_MDATA_PB_0_25	r	GBD[199]	GBD[198]	GBD[197]	GBD[196]	GBD[195]	GBD[194]	GBD[193]	GBD[192]
0xDD	0x00	GAMUT_MDATA_PB_0_26	r	GBD[207]	GBD[206]	GBD[205]	GBD[204]	GBD[203]	GBD[202]	GBD[201]	GBD[200]
0xDE	0x00	GAMUT_MDATA_PB_0_27	r	GBD[215]	GBD[214]	GBD[213]	GBD[212]	GBD[211]	GBD[210]	GBD[209]	GBD[208]
0xDF	0x00	GAMUT_MDATA_PB_0_28	r	GBD[223]	GBD[222]	GBD[221]	GBD[220]	GBD[219]	GBD[218]	GBD[217]	GBD[216]
0xE0	0x82	AVI_PACKET_ID	rw	AVI_PACKET_ID[7]	AVI_PACKET_ID[6]	AVI_PACKET_ID[5]	AVI_PACKET_ID[4]	AVI_PACKET_ID[3]	AVI_PACKET_ID[2]	AVI_PACKET_ID[1]	AVI_PACKET_ID[0]
0xE1	0x00	AVI_INF_VERS	r	AVI_INF_VERS[7]	AVI_INF_VERS[6]	AVI_INF_VERS[5]	AVI_INF_VERS[4]	AVI_INF_VERS[3]	AVI_INF_VERS[2]	AVI_INF_VERS[1]	AVI_INF_VERS[0]
0xE2	0x00	AVI_INF_LEN	r	AVI_INF_LEN[7]	AVI_INF_LEN[6]	AVI_INF_LEN[5]	AVI_INF_LEN[4]	AVI_INF_LEN[3]	AVI_INF_LEN[2]	AVI_INF_LEN[1]	AVI_INF_LEN[0]
0xE3	0x84	AUD_PACKET_ID	rw	AUD_PACKET_ID[7]	AUD_PACKET_ID[6]	AUD_PACKET_ID[5]	AUD_PACKET_ID[4]	AUD_PACKET_ID[3]	AUD_PACKET_ID[2]	AUD_PACKET_ID[1]	AUD_PACKET_ID[0]
0xE4	0x00	AUD_INF_VERS	r	AUD_INF_VERS[7]	AUD_INF_VERS[6]	AUD_INF_VERS[5]	AUD_INF_VERS[4]	AUD_INF_VERS[3]	AUD_INF_VERS[2]	AUD_INF_VERS[1]	AUD_INF_VERS[0]
0xE5	0x00	AUD_INF_LEN	r	AUD_INF_LEN[7]	AUD_INF_LEN[6]	AUD_INF_LEN[5]	AUD_INF_LEN[4]	AUD_INF_LEN[3]	AUD_INF_LEN[2]	AUD_INF_LEN[1]	AUD_INF_LEN[0]
0xE6	0x83	SPD_PACKET_ID	rw	SPD_PACKET_ID[7]	SPD_PACKET_ID[6]	SPD_PACKET_ID[5]	SPD_PACKET_ID[4]	SPD_PACKET_ID[3]	SPD_PACKET_ID[2]	SPD_PACKET_ID[1]	SPD_PACKET_ID[0]
0xE7	0x00	SPD_INF_VERS	r	SPD_INF_VERS[7]	SPD_INF_VERS[6]	SPD_INF_VERS[5]	SPD_INF_VERS[4]	SPD_INF_VERS[3]	SPD_INF_VERS[2]	SPD_INF_VERS[1]	SPD_INF_VERS[0]
0xE8	0x00	SPD_INF_LEN	r	SPD_INF_LEN[7]	SPD_INF_LEN[6]	SPD_INF_LEN[5]	SPD_INF_LEN[4]	SPD_INF_LEN[3]	SPD_INF_LEN[2]	SPD_INF_LEN[1]	SPD_INF_LEN[0]
0xE9	0x85	MS_PACKET_ID	rw	MS_PACKET_ID[7]	MS_PACKET_ID[6]	MS_PACKET_ID[5]	MS_PACKET_ID[4]	MS_PACKET_ID[3]	MS_PACKET_ID[2]	MS_PACKET_ID[1]	MS_PACKET_ID[0]
0xEA	0x00	MS_INF_VERS	r	MS_INF_VERS[7]	MS_INF_VERS[6]	MS_INF_VERS[5]	MS_INF_VERS[4]	MS_INF_VERS[3]	MS_INF_VERS[2]	MS_INF_VERS[1]	MS_INF_VERS[0]
0xEB	0x00	MS_INF_LEN	r	MS_INF_LEN[7]	MS_INF_LEN[6]	MS_INF_LEN[5]	MS_INF_LEN[4]	MS_INF_LEN[3]	MS_INF_LEN[2]	MS_INF_LEN[1]	MS_INF_LEN[0]
0xEC	0x81	VS_PACKET_ID	rw	VS_PACKET_ID[7]	VS_PACKET_ID[6]	VS_PACKET_ID[5]	VS_PACKET_ID[4]	VS_PACKET_ID[3]	VS_PACKET_ID[2]	VS_PACKET_ID[1]	VS_PACKET_ID[0]
0xED	0x00	VS_INF_VERS	r	VS_INF_VERS[7]	VS_INF_VERS[6]	VS_INF_VERS[5]	VS_INF_VERS[4]	VS_INF_VERS[3]	VS_INF_VERS[2]	VS_INF_VERS[1]	VS_INF_VERS[0]
0xEE	0x00	VS_INF_LEN	r	VS_INF_LEN[7]	VS_INF_LEN[6]	VS_INF_LEN[5]	VS_INF_LEN[4]	VS_INF_LEN[3]	VS_INF_LEN[2]	VS_INF_LEN[1]	VS_INF_LEN[0]
0xEF	0x04	ACP_PACKET_ID	rw	ACP_PACKET_ID[7]	ACP_PACKET_ID[6]	ACP_PACKET_ID[5]	ACP_PACKET_ID[4]	ACP_PACKET_ID[3]	ACP_PACKET_ID[2]	ACP_PACKET_ID[1]	ACP_PACKET_ID[0]
0xF0	0x00	ACP_TYPE	r	ACP_TYPE[7]	ACP_TYPE[6]	ACP_TYPE[5]	ACP_TYPE[4]	ACP_TYPE[3]	ACP_TYPE[2]	ACP_TYPE[1]	ACP_TYPE[0]
0xF1	0x00	ACP_HEADER2	r	ACP_HEADER2[7]	ACP_HEADER2[6]	ACP_HEADER2[5]	ACP_HEADER2[4]	ACP_HEADER2[3]	ACP_HEADER2[2]	ACP_HEADER2[1]	ACP_HEADER2[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xF2	0x05	ISRC1_PACKET_ID	rw	ISRC1_PACKET_ID[7]	ISRC1_PACKET_ID[6]	ISRC1_PACKET_ID[5]	ISRC1_PACKET_ID[4]	ISRC1_PACKET_ID[3]	ISRC1_PACKET_ID[2]	ISRC1_PACKET_ID[1]	ISRC1_PACKET_ID[0]
0xF3	0x00	ISRC1_HEADER1	r	ISRC1_HEADER1[7]	ISRC1_HEADER1[6]	ISRC1_HEADER1[5]	ISRC1_HEADER1[4]	ISRC1_HEADER1[3]	ISRC1_HEADER1[2]	ISRC1_HEADER1[1]	ISRC1_HEADER1[0]
0xF4	0x00	ISRC1_HEADER2	r	ISRC1_HEADER2[7]	ISRC1_HEADER2[6]	ISRC1_HEADER2[5]	ISRC1_HEADER2[4]	ISRC1_HEADER2[3]	ISRC1_HEADER2[2]	ISRC1_HEADER2[1]	ISRC1_HEADER2[0]
0xF5	0x06	ISRC2_PACKET_ID	rw	ISRC2_PACKET_ID[7]	ISRC2_PACKET_ID[6]	ISRC2_PACKET_ID[5]	ISRC2_PACKET_ID[4]	ISRC2_PACKET_ID[3]	ISRC2_PACKET_ID[2]	ISRC2_PACKET_ID[1]	ISRC2_PACKET_ID[0]
0xF6	0x00	ISRC2_HEADER1	r	ISRC2_HEADER1[7]	ISRC2_HEADER1[6]	ISRC2_HEADER1[5]	ISRC2_HEADER1[4]	ISRC2_HEADER1[3]	ISRC2_HEADER1[2]	ISRC2_HEADER1[1]	ISRC2_HEADER1[0]
0xF7	0x00	ISRC2_HEADER2	r	ISRC2_HEADER2[7]	ISRC2_HEADER2[6]	ISRC2_HEADER2[5]	ISRC2_HEADER2[4]	ISRC2_HEADER2[3]	ISRC2_HEADER2[2]	ISRC2_HEADER2[1]	ISRC2_HEADER2[0]
0xF8	0x0A	GAMUT_PACKET_ID	rw	GAMUT_PACKET_ID[7]	GAMUT_PACKET_ID[6]	GAMUT_PACKET_ID[5]	GAMUT_PACKET_ID[4]	GAMUT_PACKET_ID[3]	GAMUT_PACKET_ID[2]	GAMUT_PACKET_ID[1]	GAMUT_PACKET_ID[0]
0xF9	0x00	GAMUT_HEADER1	r	GAMUT_HEADER1[7]	GAMUT_HEADER1[6]	GAMUT_HEADER1[5]	GAMUT_HEADER1[4]	GAMUT_HEADER1[3]	GAMUT_HEADER1[2]	GAMUT_HEADER1[1]	GAMUT_HEADER1[0]
0xFA	0x00	GAMUT_HEADER2	r	GAMUT_HEADER2[7]	GAMUT_HEADER2[6]	GAMUT_HEADER2[5]	GAMUT_HEADER2[4]	GAMUT_HEADER2[3]	GAMUT_HEADER2[2]	GAMUT_HEADER2[1]	GAMUT_HEADER2[0]

1.12 DPLL MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB5	0x01	MCLK FS	rw	-	-	-	-	-	MCLK_FS_N[2]	MCLK_FS_N[1]	MCLK_FS_N[0]
0xC8	0x00	DLL CONTROL_2	rw	-	-	DLL_PHASE[5]	DLL_PHASE[4]	DLL_PHASE[3]	DLL_PHASE[2]	DLL_PHASE[1]	DLL_PHASE[0]
0xC9	0x00	FB CONTROL	rw	-	-	-	-	FB_PHASE_ADJUST[3]	FB_PHASE_ADJUST[2]	FB_PHASE_ADJUST[1]	FB_PHASE_ADJUST[0]

2 SIGNAL DOCUMENTATION

2.1 IO MAP

Reg	Bits	Description	
VID_STD[5:0]			R/W
0x00	00001000	Sets the expected video standard and desired oversampling mode. The configuration values vary with PRIM_MODE[3:0] setting. A detailed table with Primary Mode and Video Standard settings is available in the hardware manual. 001000 - Default value	
ADC_HDMI_SIMULT_MODE			R/W
0x01	00000110	This control is used to enable ADC and HDMI simultaneous mode. In this mode certain HDMI functionality is available when processing analog inputs. 0 - Disables simultaneous mode 1 - Enables simultaneous mode	
V_FREQ[2:0]			R/W
0x01	00000110	A control to set vertical frequency of HD component standards. 000 - 60 Hz 001 - 50 Hz 010 - 30 Hz 011 - 25 Hz 100 - 24 Hz 101 - Reserved 110 - Reserved 111 - Reserved	
PRIM_MODE[3:0]			R/W
0x01	00000110	A control to selects the primary mode of operation of the decoder. To be used with VID_STD[5:0]. 0000 - SDP mode 0001 - Component Mode 0010 - Graphics mode 0011 - Reserved 0100 - CVBS & HDMI AUDIO Mode 0101 - HDMI-Comp 0110 - HDMI-GR 0111 - 1111 - Reserved	
INP_COLOR_SPACE[3:0]			R/W
0x02	11110000	A control to set the colorspace of the input video. To be used in conjunction with ALT_GAMMA and RGB_OUT to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space base on the primary mode and video standard settings. Settings 1000 to 1110 are undefined. 0000 - Forces RGB (range 16 to 235) input 0001 - Forces RGB (range 0 to 255) input 0010 - Forces YCrCb input (601 color space) (range 16 to 235) 0011 - Forces YCrCb input (709 color space) (range 16 to 235) 0100 - Forces XVYCC 601 0101 - Forces XVYCC 709 0110 - Forces YCrCb input (601 color space) (range 0 to 255) 0111 - Forces YCrCb input (709 color space) (range 0 to 255) 1111 - In analog mode, input color space depends on Primary Mode and Video Standard. In HDMI mode, input color space depends on color space reported by HDMI block.	
ALT_GAMMA			R/W
0x02	11110000	A control to select the type of YPbPr colorspace conversion. This bit is to be used in conjunction with INP_COLOR_SPACE[3:0] and RGB_OUT. If ALT_GAMMA is set to 1 and RGB_OUT= 0 a colorspace conversion is applied to convert from 601 to 709 or 709 to 601. Valid only if RGB_OUT set to 0. 0 - No conversion 1 - YUV601 to YUV709 conversion applied if input is YUV601. YUV709 to YUV601 conversion applied if input is YUV709	
OP_656_RANGE			R/W
0x02	11110000	A control to set the output range of the digital data. It also automatically sets the gain setting, the offset setting, and the data saturator setting. 0 - Enables full output range (0 to 255) 1 - Enables limited output range (16 to 235)	

Reg	Bits	Description
RGB_OUT		R/W
0x02	1111000**0**	A control to select output color space and the correct digital blank level and offsets on the RGB or YPrPb outputs. It is used in conjunction with the INP_COLOR_SPACE[3:0] and ALT_GAMMA bits to select the applied CSC. 0 - YPbPr color space output 1 - RGB color space output
ALT_DATA_SAT		R/W
0x02	1111000**0**	A control to disable the data saturator that limits the output range independently of OP_656_RANGE. This bit is used to support extended data range modes. 0 - Data saturator enabled or disabled according to OP_656_RANGE setting. 1 - Reverses OP_656_RANGE decision to enable or disable the data saturator
OP_FORMAT_SEL[7:0]		R/W
0x03	**00000000**	A control to select the data format and pixel bus configuration. Refer to the pixel port configuration spreadsheet tool for full information on pixel port modes and configuration settings. 0x00 - 8-bit SDR ITU-656 mode 0x01 - 10-bit SDR ITU-656 mode 0x02 - 12-bit SDR ITU-656 mode 0 0x06 - 12-bit SDR ITU-656 mode 1 0x0A - 12-bit SDR ITU mode 2 0x20 - 8-bit 4:2:2 DDR mode 0x21 - 10-bit 4:2:2 DDR mode 0x22 - 12-bit 4:2:2 DDR mode 0 0x23 - 12-bit 4:2:2 DDR mode 1 0x24 - 12-bit 4:2:2 DDR mode 2 0x40 - 24-bit 4:4:4 SDR mode 0x41 - 30-bit 4:4:4 SDR mode 0x42 - 36-bit 4:4:4 SDR mode 0 0x46 - 36-bit SDR 4:4:4 mode 1 0x4C - 24-bit SDR 4:4:4 mode 3 0x50 - 24-bit SDR 4:4:4 mode 4 0x51 - 30-bit SDR 4:4:4 mode 4 0x52 - 36-bit SDR 4:4:4 mode 4 0x60 - 24-bit 4:4:4 DDR mode 0x61 - 30-bit 4:4:4 DDR mode 0x62 - 36-bit 4:4:4 DDR mode 0x80 - 16-bit ITU-656 SDR mode 0x81 - 20-bit ITU-656 SDR mode 0x82 - 24-bit ITU-656 SDR mode 0 0x86 - 24-bit ITU-656 SDR mode 1 0x8A - 24-bit ITU-656 SDR mode 2 0x8D - 20-bit SDR 4:2:2 mode 3 0x90 - 16-bit SDR 4:2:2 mode 4 0x91 - 20-bit SDR 4:2:2 mode 4 0x92 - 24-bit SDR 4:2:2 mode 4 0xC0 - 8-bit PAR mode 0 0xC1 - 10-bit PAR mode 0 0xC2 - 12-bit PAR mode 0
OP_CH_SEL[2:0]		R/W
0x04	**011**00010	A control to select the configuration of the pixel data bus on the pixel pins. Refer to the pixel port configuration spreadsheet tool for full information on pixel port modes and configuration settings. 000 - P[35:24] Y/G, P[23:12] U/CrCb/B, P[11:0] V/R 001 - P[35:24] Y/G, P[23:12] V/R, P[11:0] U/CrCb/B 010 - P[35:24] U/CrCb/B, P[23:12] Y/G, P[11:0] V/R 011 - P[35:24] V/R, P[23:12] Y/G, P[11:0] U/CrCb/B 100 - P[35:24] U/CrCb/B, P[23:12] V/R, P[11:0]Y/G 101 - P[35:24] V/R, P[23:12] U/CrCb/B, P[11:0] Y/G 110 - Reserved 111 - Reserved
F_OUT_SEL		R/W
0x05	0010**0**1100	This control is used to select a DE signal or a Field signal to be output on the FIELD/DE pin. 0 - DE output selected 1 - Field output selected
DATA_BLANK_EN		R/W
0x05	0010**1**1100	A control to blank data during video blanking sections. 0 - Do not blank data during horizontal and vertical blanking periods. 1 - Blank data during horizontal and vertical blanking periods.

Reg	Bits	Description	
AVCODE_INSERT_EN			R/W
0x05	00101100	A control to select AV code insertion into the data stream 0 - Does not insert AV codes into data stream 1 - Inserts AV codes into data stream	
REPL_AV_CODE			R/W
0x05	00101100	A control to select the duplication of the AV codes and insertion on all data channels of the output data stream 0 - Outputs complete SAV/EAV codes on all Channels, Channel A, Channel B and Channel C. 1 - Spreads AV code across the three channels. Channel B and Channel C contain the first two ten bit words, 0x3FF and 0x000. Channel A contains the final two ten bit words 0x00 and 0xXYZ.	
OP_SWAP_CB_CR			R/W
0x05	00101100	A controls the swapping of Cr and Cb data on the pixel buses. 0 - Outputs Cr and Cb as per OP_FORMAT_SEL 1 - Inverts the order of Cb and Cr in the interleaved data stream	
VS_OUT_SEL			R/W
0x06	10100000	This control is used to select a VSync signal or Field signal to be output on the VS/Field pin. 0 - Field output on VS/FIELD pin 1 - VSync output on VS/FIELD pin	
HS_OUT_SEL[1:0]			R/W
0x06	10100000	This control is used to select the signal to be output on the HS/CS output pin. 00 - Regenerates CSync signal, synchronous to LLC 01 - Regenerates HSync signal, synchronous to LLC 10 - Asynchronous HSync 11 - Depending on result of SSPD, signal output on HS/CS pin is: Logic AND of HS and VS input after polarity correction, if HS/VS detected by SSPD. CS input if CS/VS detected by SSPD Sliced embedded sync if embedded synchronization detected by SSPD	
INV_SYNC_OUT_POL			R/W
0x06	10100000	This control is used to set the polarity of the SYNC_OUT signal. This bit is not valid in power-save mode. 0 - Negative polarity SYNC_OUT signal 1 - Positive polarity SYNC_OUT signal	
INV_F_POL			R/W
0x06	10100000	This control is used to select the polarity of the FIELD/DE signal. 0 - Negative FIELD/DE polarity 1 - Positive FIELD/DE polarity	
INV_VS_POL			R/W
0x06	10100000	This control is used to select the polarity of the VS/FIELD signal 0 - Negative polarity VS/FIELD 1 - Positive polarity VS/FIELD	
INV_HS_POL			R/W
0x06	10100000	This control is used to select the polarity of the HS/CS signal. 0 - Negative polarity HS/CS 1 - Positive polarity HS/CS	
INV_LLC_POL			R/W
0x06	10100000	This control is used to invert the polarity of the LLC. 0 - Does not invert LLC 1 - Inverts LLC	
SYNC_CH_AUTO_MODE			R/W
0x07	01000000	A control to set automatic synchronization channel selection to CP core. Auto mode selects which synchronization channel drives the CP based on the free run status of each channel. The priority of selection is determined by SYNC_CH1_PRIORITY when both channels are in free run mode. 0 - Disables auto mode. Priority of channels determined by SYNC_CH1_PRIORITY. 1 - Enables auto mode. Automatically selects which synchronization channel drives the CP core based on the free-run status.	
SYNC_CH1_PRIORITY			R/W
0x07	01000000	A control to select which sync channel has priority to CP core. 0 - sync channel 2 sync processing result takes priority 1 - sync channel 1 sync processing result takes priority	

Reg	Bits	Description
SYNC_CH1_HS_SEL[1:0]		R/W
0x07	0100 0000	A control to select the HSync input to sync channel 1. 00 - Auto-select mode; HS_IN1 or HSync from HDMI (HDMI-HS) set to channel 1 based on primary mode set in PRIM_MODE[3:0]. HDMI-HS in HDMI mode. HS1 input in Component or Graphics mode. 01 - Select HS_IN1 10 - Select HS_IN2 11 - HDMI-HS
SYNC_CH1_VS_SEL[1:0]		R/W
0x07	0100 0000	A control to select the VSync input to sync channel 1. 00 - Auto-select mode; VS_IN1 or VSync from HDMI (HDMI-VS) set to channel 1 based on primary mode set in PRIM_MODE[3:0]. HDMI-VS in HDMI mode. VS1 input in Component or Graphics mode. 01 - Select VS_IN1 input 10 - Select VS_IN2 input 11 - HDMI-VS
SYNC_CH1_EMB_SYNC_SEL[1:0]		R/W
0x07	0100 0000	A control to select from the outputs of the two synchronization sources as input to sync channel 1. 00 - Auto-select mode; EMB_SYNC_SEL1 in component or graphics mode or tied LO in HDMI mode. The selection is based on primary mode. 01 - EMB_SYNC_SEL1 10 - EMB_SYNC_SEL2 11 - Tie to GND
SYNC_CH2_HS_SEL[1:0]		R/W
0x08	0001 0100	A control to select the HSync input to sync channel 2. 00 - Select HS2 input 01 - Select HS1 input 10 - Select HS2 input 11 - Select HDMI HS
SYNC_CH2_VS_SEL[1:0]		R/W
0x08	0001 0100	A control to select the VSync input to Sync Channel 2 00 - Select VS2 input 01 - Select VS1 input 10 - Select VS2 input 11 - Select HDMI VS
SYNC_CH2_EMB_SYNC_SEL[1:0]		R/W
0x08	0001 0100	A control to select from the outputs of the two Sync Slicers as input to Sync Channel 2 00 - EMB_SYNC_SEL2 01 - EMB_SYNC_SEL1 10 - EMB_SYNC_SEL2 11 - Tie To GND
SEL_RAW_CS		R/W
0x0B	0100 0100	A control to select the type of signal applied to SYNC_OUT. 0 - Raw HSync type signal through SYNC_OUT pad 1 - Raw CSync type signal through SYNC_OUT pad
CORE_PDN		R/W
0x0B	0100 0100	This is a power-down control for the DPP, CP core and digital sections of the HDMI core. 0 - Powers up DPP, CP, SDP and digital sections of HDMI block 1 - Powers down the DPP, CP, SDP and digital section of HDMI block. STDI and SSPD are still active when CORE_PDN is set.
XTAL_PDN		R/W
0x0B	0100 0100	This is a power-down control for the XTAL in the digital blocks. 0 - Powers up XTAL buffer to digital core 1 - Powers down XTAL buffer to digital core
POWER_DOWN		R/W
0x0C	0110 0010	This control enables power-down mode. It is the main I2C power-down control. 0 - Chip is operational 1 - Enables chip power down
CP_PWRDN		R/W
0x0C	0110 0010	This is a power-down control for the CP core. 0 - Powers up the clock to the CP core. 1 - Powers down the clock to the CP core. VDP, SDP and HDMI blocks are not affected by this bit.

Reg	Bits	Description
VDP_PDN		R/W
0x0C	0110001<u>1</u>0	This is a power-down control for the VDP. It is recommended to power-down the VDP when this feature is not required. 0 - Powers up the VDP section 1 - Powers down the VDP section
PADS_PDN		R/W
0x0C	0110001<u>0</u>	A power down control for pads of the digital output pins. When enabled pads are tristated and the input path is disabled. This control applies to the FIELD/DE, HS, VS/FIELD, INT, SYNC_OUT, LLC pads and the pixel pads P0 to P35, 0 - Powers up the pads of the digital output pins 1 - Powers down the pads of the digital output pins
SEL_SYNC_CHANNEL		R
0x12	<u>0</u>0000000	A readback to indicate the currently selected sync processing channel applied to CP core 0 - Sync Channel 2 is being processed by CP core 1 - Sync Channel 1 is being processed by CP core
CP_STDI_INTERLACED		R
0x12	0000<u>0</u>000	A readback to indicate the interlaced status of the currently selected STDI block applied to the CP core. 0 - Selected STDI has detected a progressive input 1 - Selected STDI has detected a interlaced input.
CP_INTERLACED		R
0x12	0000<u>0</u>000	A readback to indicate the interlaced status of the CP core based on configuration of Video standard and INTERLACED bit in the CP map. 0 - CP core is processing the input as a progressive input. 1 - CP core is processing the input as a interlaced input.
CP_PROG_PARM_FOR_INT		R
0x12	00000<u>0</u>00	A readback to indicate the if the CP core is processing for progressive standard while are the Video standard and the INTERLACED bit in the CP Map are configured for an interlaced standard. 0 - CP core processing for a progressive standard while Video standard and the INTERLACED bits are configured for an interlaced standard 1 - CP core processing for a progressive standard while Video standard and the INTERLACED bits are configured for an progressive standard
CP_FORCE_INTERLACED		R
0x12	000000<u>0</u>0	A readback to indicate forced-interlaced status of the CP core based on configuration of Video standard and INTERLACED bit in the CP Map. 0 - Input is detected as interlaced and the CP is programmed in an interlaced mode via VID_STD[5:0] 1 - Input is detected as progressive and the CP is programmed in an interlaced mode.
CP_NON_STD_VIDEO		R
0x12	0000000<u>0</u>	A control to indicate that the CP core has detected a non standard number of lines on the incoming video compared to the standard specified by VID_STD[5:0] 0 - Input has same number of lines as that of the format programmed 1 - Input has different number of lines to that of format programmed
CP_CURRENT_SYNC_SRC[1:0]		R
0x13	000000<u>00</u>	A readback of the synchronization source currently being used by CP core 00 - Invalid 01 - Separate HSync and VSync on HS_IN and VS_IN pins 10 - External CSync on HS_IN pin 11 - Embedded synchronization (SOG/SOY)
DR_STR[1:0]		R/W
0x14	01<u>10</u>1010	This control is used to set the drive strength of the data output drivers. 00 - Low (1x) 01 - Medium low (2x) 10 - Medium high (3x) 11 - High (4x)
DR_STR_CLK[1:0]		R/W
0x14	0110<u>10</u>10	This control is used to set the drive strength control for the output pixel clock out signal on the LLC pin. 00 - Low (1x) 01 - Medium low (2x) for LLC up to 60 MHz 10 - Medium high (3x) for LLC from 44 MHz to 105 MHz 11 - High (4x) for LLC greater than 100 MHz

Reg	Bits	Description	
DR_STR_SYNC[1:0]			R/W
0x14	01101010	This control is used to set the drive strength of the synchronization pins, HS/CS, VS/FIELD, FIELD/DE and SYNC_OUT. 00 - Low (1x) 01 - Medium low (2x) 10 - Medium high (3x) 11 - High (4x)	
TRI_SYNC_OUT			R/W
0x15	10111110	Tristate control for SYNC_OUT pin. 0 - SYNC_OUT pin active 1 - Tristate SYNC_OUT pin	
TRI_AUDIO			R/W
0x15	10111110	This control is used to tristate the audio output interface pins, AP[5:0], SCLK and MCLK. 0 - Audio output pins active 1 - Tristates audio output pins	
TRI_SYNCS			R/W
0x15	10111110	Synchronization output pins tristate control. The synchronization pins under this control are HS/CS, VS/FIELD, and FIELD/DE. 0 - Sync output pins active 1 - Tristate sync output pins	
TRI_LLC			R/W
0x15	10111110	This control is used to tristate the output pixel clock on the LLC pin. 0 - LLC pin active 1 - Tristates LLC pin	
TRI_PIX			R/W
0x15	10111110	This control is used to tristate the pixel data on the pixel pins P[35:0]. 0 - Pixel bus active 1 - Tristates pixel bus	
PLL_DIV_MAN_EN			R/W
0x16	01000011	This control is used to manually override the PLL divider ratio value. 0 - Disables manual PLL divider ratio settings. PLL divider ratio set by PRIM_MODE[3:0] and VID_STD[5:0] 1 - Manually sets PLL_DIV ratio as defined by PLL_DIV[12:0]	
PLL_DIV_RATIO[12:0]			R/W
0x16 0x17	01000011 01011010	This control is used to manually set the PLL divide ratio. These registers are sequenced and require sequential writes in order to update the value. xxxxxxxxxxxxx - Synthesizer feedback value. PLL_DIV_MAN_EN must be set for this value to be active.	
LLC_DLL_EN			R/W
0x19	00000000	A control to enable the Delay Locked Loop for output pixel clock. LLC_DLL_MUX must be set to 1 for this setting to be effective. 1 - Enable LLC DLL 0 - Disable LLC DLL	
LLC_DLL_DOUBLE			R/W
0x19	00000000	A control to double the LLC clock frequency. LLC_DLL_MUX must be set to 1 for this setting to be effective. 0 - Nominal LLC Clock frequency 1 - Double LLC clock frequency	
LLC_DLL_PHASE[4:0]			R/W
0x19	00000000	A control to adjust LLC DLL phase in increments of 1/32 of a clock period. LLC_DLL_MUX must be set to 1 for this setting to be effective. 00000 - Default xxxxx - Sets on of 32 phases of DLL to vary LLC CLK	
SUBI2C_EN			R/W
0x1A	00000010	A control to enable the secondary I2C interface used for fast access to VBI data. 0 - Disable secondary I2C interface 1 - Enable secondary I2C interface	
VDP_ON_SUB_I2C			R/W
0x1A	00000010	A control to allow VDP Map read access from secondary I2C interface. 0 - Disable VDP Map read access from sub I2C 1 - Enable VDP Map read access from sub I2C	

Reg	Bits	Description	
HPA_MAN_VALUE_A			R/W
0x20	1110000	A manual control for the value of HPA on Port A. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_A pin. 1 - High level applied to HPA_A pin.	
HPA_MAN_VALUE_B			R/W
0x20	111 0000	A manual control for the value of HPA on Port B. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_B pin. 1 - High level applied to HPA_B pin.	
HPA_TRISTATE_A			R/W
0x20	1111000	Tristate HPA output pin for Port A. 0 - HPA_A pin active. 1 - Tristate HPA_A pin	
HPA_TRISTATE_B			R/W
0x20	1111000	Tristate HPA output pin for Port B. 0 - HPA_B pin active 1 - Tristate HPA_B pin.	
HPA_STATUS_PORT_A			R
0x21	0000000	Readback of HPA status for Port A 0 - +5V not applied to HPA_A pin by chip. 1 - +5V applied to HPA_A pin by chip.	
HPA_STATUS_PORT_B			R
0x21	0000000	Readback of HPA status for Port B 0 - +5V not applied to HPA_B pin by chip 1 - +5V applied to HPA_B pin by chip	
PIXBUS_MSB_TO_LSB_REORDER			R/W
0x30	1001000	A control to swap the MSB to LSB orientation on the pixel bus. 0 - Output bus goes from MSB to LSB 1 - Output bus goes from LSB to MSB	
LLC_DLL_MUX			R/W
0x33	0000000	A control to apply the pixel clock DLL to the pixel clock output on the LLC pin. 0 - Bypasses the DLL 1 - Muxes the DLL output on LLC output	
INTRQ_RAW			R
0x3F	0000000	Status of the interrupt signal on INT1 interrupt pin. If an interrupt event that has been enabled for the INT1 pin has occurred this bit will be set to 1. Interrupts for INT1 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT1 are cleared. 0 - No interrupt on INT1 1 - An interrupt event for INT 1 has occurred.	
INTRQ2_RAW			R
0x3F	0000000	Status of the interrupt signal on INT2 interrupt pin. If an interrupt event that has been enabled for the INT2 pin has occurred this bit will be set to 1. Interrupts for INT2 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT2 are cleared. 0 - No interrupt on INT2 1 - An interrupt event for INT2 has occurred.	
INTRQ_DUR_SEL[1:0]			R/W
0x40	00100000	A control to select the interrupt signal duration for the interrupt signal on INT1 00 - 4 Xtal periods 01 - 16 Xtal periods 10 - 64 Xtal periods 11 - Active until cleared	
STORE_UNMASKED_IRQS			R/W
0x40	0010000	STORE_MASKED_IRQS allows the HDMI status flags for any HDMI interrupt to be triggered regardless of whether the mask bits are set. This bit allows a HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur. 0 - Does not allow x_ST flag of any HDMI interrupt to be set independently of mask bits 1 - Allows x_ST flag of any HDMI interrupt to be set independently of mask bits	

Reg	Bits	Description	
EN_MUTE_OUT_INTRQ			R/W
0x40	00100000	A control to apply the audio mute signal on INT1 interrupt pin. 0 - Does not output audio mute signal on INT1 1 - Outputs audio mute signal on INT1	
MPU_STIM_INTRQ			R/W
0x40	00100000	Manual interrupt set control. This feature should be used for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin 0 - Disables manual interrupt mode 1 - Enables manual interrupt mode	
INTRQ_OP_SEL[1:0]			R/W
0x40	00100000	Interrupt signal configuration control for INT1 00 - Open drain 01 - Drives low when active 10 - Drives high when active 11 - Disabled	
INTRQ2_DUR_SEL[1:0]			R/W
0x41	00110000	A control to select the interrupt signal duration for the interrupt signal on INT2 00 - 4 Xtal periods 01 - 16 Xtal periods 10 - 64 Xtal periods 11 - Active until cleared	
CP_LOCK_UNLOCK_EDGE_SEL			R/W
0x41	00110000	A control to configure the functionality of the CP_LOCK and CP_UNLOCK interrupts. The interrupts can be generated when their respective status, CP_LOCK, CP_UNLOCK are valid. Or alternatively an interrupt can be generated when a change in their respective status occurs. 0 - Generate interrupt for a LOW to HIGH change only for the CP_LOCK and CP_UNLOCK interrupts. 1 - Generate interrupt for a LOW to HIGH or a HIGH to LOW change for the the CP_LOCK and CP_UNLOCK interrupts.	
STDI_DATA_VALID_EDGE_SEL			R/W
0x41	00110000	A control to configure the functionality of the STDI_DATA_VALID interrupt. The interrupt can be generated for the case when STDI changes to an STDI valid state. Alternatively it can be generated to indicate a change in STDI_VALID status. 0 - Generate interrupt for a LOW to HIGH change in STDI_VALID status 1 - Generate interrupt for a LOW to HIGH or a HIGH to LOW change in STDI_VALID status	
EN_MUTE_OUT_INTRQ2			R/W
0x41	00110000	A control to apply the internal audio mute signal on INT2 interrupt pin. 0 - Does not output audio mute signal on INT2 1 - Outputs audio mute signal on INT2	
INT2_EN			R/W
0x41	00110000	A control to enable INT2. 0 - Disable INT2 1 - Enable INT2	
INTRQ2_OP_SEL[1:0]			R/W
0x41	00110000	Interrupt signal configuration control for INT2 00 - Open drain 01 - Drives low when active 10 - Drives high when active 11 - Disabled	
SSPD_RSLT_CHNGD_RAW			R
0x42	00000000	Status of the SSPD Result Changed interrupt signal. When set to 1 it indicates a change in SSPD result of the currently selected sync channel. A change in SSPD result can be either due to a polarity or source change. The currently selected channel refers to sync channel currently applied to the CP core. Once set, this bit will remain high until it is cleared via SSPD_RSLT_CHNGD_CLR. 0 - No change in the SSPD result. 1 - A change has occurred in SSPD result.	
MV_PS_DET_RAW			R
0x42	00000000	Raw signal status of the Macrovision Pseudo -Sync detected signal. 0 - No Macrovision pseudo syncs detected. 1 - Macrovision pseudo sync detected.	

Reg	Bits	Description
STDI_DATA_VALID_RAW		R
0x42	0000**0**0000	STDI_DATA_VALID interrupt can be either an edge sensitive or level sensitive interrupt depending on the configuration of STDI_DATA_VALID_EDGE_SEL register. When STDI_DATA_VALID_EDGE_SEL set to 1 it is a level sensitive interrupt and STDI_DATA_VALID_RAW is the raw signal status of the STDI Data Valid signal. When STDI_DATA_VALID_EDGE_SEL set to 0 it is a edge sensitive interrupt and STDI_DATA_VALID_RAW is a sampled -status of the STDI Data Valid signal following a change in the signal. Once set, this bit will remain high until it is cleared via STDI_DATA_VALID_CLR. 0 - STDI data is not valid. 1 - STDI data is valid.
CP_UNLOCK_RAW		R
0x42	00000**0**000	Status of the CP_UNLOCK interrupt signal. When set to 1 it indicates a change in unlock status of the CP core. Once set, this bit will remain high until it is cleared via CP_UNLOCK_CLR. 0 - CP is locked 1 - CP is unlocked.
CP_LOCK_RAW		R
0x42	000000**0**00	Status of the CP_LOCK interrupt signal. When set to 1 it indicates a change in lock status of the CP core. Once set, this bit will remain high until it is cleared via CP_LOCK_CLR. 0 - CP is unlocked 1 - CP is locked.
AFE_INTERRUPT_RAW		R
0x42	0000000**0**	Raw signal status of the Analog Front end interrupt signal. 0 - No AFE interrupt pending 1 - AFE interrupt present
SSPD_RSLT_CHNGD_ST		R
0x43	**0**0000000	Latched signal status of SSPD Result Changed interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SSPD_RSLT_CHNGD_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No SSPD result changed interrupt event occurred. 1 - A SSPD result changed interrupt event has occurred..
MV_PS_DET_ST		R
0x43	0**0**000000	Latched signal status of Macrovision Pseudo sync detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MV_PS_DET_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No Macrovision pseudo sync detection interrupt event has occurred. 1 - A Macrovision pseudo sync detected interrupt event has occurred.
STDI_DATA_VALID_ST		R
0x43	0000**0**0000	Latched signal status of STDI valid interrupt signal. Once set this bit will remain high until the interrupt has been cleared via STDI_DATA_VALID_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No STDI valid interrupt has occurred. 1 - A STDI valid interrupt has occurred.
CP_UNLOCK_ST		R
0x43	00000**0**000	Latched signal status of CP Unlock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CP_UNLOCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No CP UNLOCK interrupt event has occurred. 1 - A CP UNLOCK interrupt event has occurred.
CP_LOCK_ST		R
0x43	000000**0**00	Latched signal status of the CP Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CP_LOCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No CP LOCK interrupt event has occurred. 1 - A CP LOCK interrupt event has occurred.
AFE_INTERRUPT_ST		R
0x43	0000000**0**	Latched signal status of the AFE interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AFE_INTERRUPT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No AFE interrupt event has occurred. 1 - AFE interrupt event has occurred.
SSPD_RSLT_CHNGD_CLR		SC
0x44	**0**0000000	Clear bit for SSPD Result Changed interrupt signal. 0 - Does not clear SSPD_RESULT_ST bit 1 - Clears SSPD_RESULT_ST bit

Reg	Bits	Description
MV_PS_DET_CLR		SC
0x44	0[0]000000	Clear bit for Macrovision Pseudo -sync detected interrupt signal. 0 - Does not clear MV_PS_DET_ST bit 1 - Clears MV_PS_DET_ST bit
STDI_DATA_VALID_CLR		SC
0x44	000[0]0000	Clear bit for STDI Data valid interrupt signal. 0 - Does not clear STDI_DVALID_ST bit 1 - Clears STDI_DVALID_ST bit
CP_UNLOCK_CLR		SC
0x44	0000[0]000	Clear bit for CP unlock interrupt signal. 0 - Does not clear CP_UNLOCK_ST bit 1 - Clears CP_UNLOCK_ST bit
CP_LOCK_CLR		SC
0x44	00000[0]00	Clear bit for CP Lock interrupt signal. 0 - Does not clear CP_LOCK_ST bit 1 - Clears CP_LOCK_ST bit
AFE_INTERRUPT_CLR		SC
0x44	0000000[0]	Clear bit for Analog Front end interrupt signal. 0 - Does not clear AFE_INTERRUPT_ST bit 1 - Clears AFE_INTERRUPT_ST bit
SSPD_RSLT_CHNGD_MB2		R/W
0x45	[0]0000000	INT2 interrupt mask for SSPD Result Changed interrupt. When set the SSPD Result changed interrupt will trigger the INT2 interrupt and SSPD_RSLT_CHNGD_ST will indicate the interrupt status. 0 - Disables SSPD Changed interrupt for INT2 1 - Enables SSPD Changed interrupt for INT2
MV_PS_DET_MB2		R/W
0x45	0[0]000000	INT2 interrupt mask for Macrovision Pseudo-sync detected interrupt. When set the Macrovision Pseudo-sync detected interrupt will trigger the INT2 interrupt and MV_PS_DET_ST will indicate the interrupt status. 0 - Disables Macrovision Pseudo-sync detected interrupt for INT2 1 - Enables Macrovision Pseudo-sync detected interrupt for INT2
STDI_DATA_VALID_MB2		R/W
0x45	000[0]0000	INT2 interrupt mask for STDI Data valid interrupt. When set the STDI Data valid interrupt will trigger the INT2 interrupt and STDI_DATA_VALID_ST will indicate the interrupt status. 0 - Disables STDI Data valid interrupt for INT2 1 - Enables STDI Data valid interrupt for INT2
CP_UNLOCK_MB2		R/W
0x45	0000[0]000	INT2 interrupt mask for CP Unlock interrupt. When set the CP Unlock interrupt will trigger the INT2 interrupt and CP_UNLOCK_ST will indicate the interrupt status. 0 - Disable CP Unlock interrupt for INT2 1 - Enable CP Unlock interrupt for INT2
CP_LOCK_MB2		R/W
0x45	00000[0]00	INT2 interrupt mask for CP Lock interrupt. When set the CP Lock interrupt will trigger the INT2 interrupt and CP_LOCK_ST will indicate the interrupt status. 0 - Disable CP Lock interrupt for INT2 1 - Enable CP Lock interrupt for INT2
AFE_INTERRUPT_MB2		R/W
0x45	0000000[0]	INT2 interrupt mask for Analog Front end interrupt. When set the Analog Front end interrupt will trigger the INT2 interrupt and AFE_INTERRUPT_ST will indicate the interrupt status. 0 - Disable Analog Front end interrupt for INT2 1 - Enable Analog Front end interrupt for INT2
SSPD_RSLT_CHNGD_MB1		R/W
0x46	[0]0000000	INT1 interrupt mask for SSPD Result Changed interrupt. When set the SSPD Result changed interrupt will trigger the INT1 interrupt and SSPD_RSLT_CHNGD_ST will indicate the interrupt status. 0 - Disables SSPD Changed interrupt for INT1 1 - Enables SSPD Changed interrupt for INT1

Reg	Bits	Description	
MV_PS_DET_MB1			R/W
0x46	01000000	INT1 interrupt mask for Macrovision Pseudo-sync detected interrupt. When set the Macrovision Pseudo-sync detected interrupt will trigger the INT1 interrupt and MV_PS_DET_ST will indicate the interrupt status. 0 - Disables Macrovision Pseudo-sync detected interrupt for INT1 1 - Enables Macrovision Pseudo-sync detected interrupt for INT1	
STDI_DATA_VALID_MB1			R/W
0x46	00010000	INT1 interrupt mask for STDI Data valid interrupt. When set the STDI Data valid interrupt will trigger the INT1 interrupt and STDI_DATA_VALID_ST will indicate the interrupt status. 0 - Disables STDI Data valid interrupt for INT1 1 - Enables STDI Data valid interrupt for INT1	
CP_UNLOCK_MB1			R/W
0x46	00001000	INT1 interrupt mask for CP Unlock interrupt. When set the CP Unlock interrupt will trigger the INT1 interrupt and CP_UNLOCK_ST will indicate the interrupt status. 0 - Disable CP Unlock interrupt for INT1 1 - Enable CP Unlock interrupt for INT1	
CP_LOCK_MB1			R/W
0x46	00000100	INT1 interrupt mask for CP Lock interrupt. When set the CP Lock interrupt will trigger the INT1 interrupt and CP_LOCK_ST will indicate the interrupt status. 0 - Disable CP Lock interrupt for INT1 1 - Enable CP Lock interrupt for INT1	
AFE_INTERRUPT_MB1			R/W
0x46	00000001	INT1 interrupt mask for Analog Front end interrupt. When set the Analog Front end interrupt will trigger the INT1 interrupt and AFE_INTERRUPT_ST will indicate the interrupt status. 0 - Disable Analog Front end interrupt for INT1 1 - Enable Analog Front end interrupt for INT1	
MPU_STIM_INTRQ_RAW			R
0x47	10000000	Raw status of manual forced interrupt signal. 0 - Manual forced interrupt not applied 1 - Manual forced interrupt applied	
MV_AGC_DET_RAW			R
0x47	01000000	Raw status of Macrovision AGC detection signal. 0 - Macrovision AGC not detected 1 - Macrovision AGC detected	
MV_CS_DET_RAW			R
0x47	00100000	Raw status of Macrovision Color-stripe detection signal. 0 - Macrovision Color-stripe not detected 1 - Macrovision Color-stripe detected	
CP_CGMS_CHNGD_RAW			R
0x47	00000100	Status of the CP CGMS data changed interrupt signal. When set to 1 it indicates a change in CGMS data or a change in CGMS data availability. Once set this bit will remain high until the interrupt has been cleared via CP_CGMS_CHNGD_CLR. 0 - No change in CGMS data or CGMS availability has occurred 1 - A change in CGMS data or CGMS availability has occurred.	
MPU_STIM_INTRQ_ST			R
0x48	10000000	Latched signal status of Manual Forced interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MPU_STIM_INTRQ_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Forced manual interrupt event has not occurred. 1 - Force manual interrupt even has occurred.	
MV_AGC_DET_ST			R
0x48	01000000	Latched signal status of Macrovision AGC detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MV_AGC_DET_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - A Macrovision AGC detected interrupt event has not occurred. 1 - A Macrovision AGC detected interrupt event has occurred.	
MV_CS_DET_ST			R
0x48	00100000	Latched signal status of Macrovision Color-stripe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MV_CS_DET_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - A Macrovision Color-stripe detected interrupt event has not occurred. 1 - A Macrovision Color-stripe detected interrupt event has occurred.	

Reg	Bits	Description	
CP_CGMS_CHNGD_ST			R
0x48	00000000	Latched signal status of CP CGMS Changed interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CP_CGMS_CHNGD_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - A CGMS data changed interrupt event has not occurred. 1 - A CGMS data changed interrupt event has occurred.	
MPU_STIM_INTRQ_CLR			SC
0x49	00000000	Clear bit for Manual Forced interrupt signal. 0 - Does not clear MPU_STIM_INT_ST bit 1 - Clears MPU_STIM_INT_ST bit	
MV_AGC_DET_CLR			SC
0x49	00000000	Clear bit for Macrovision AGC detected interrupt signal. 0 - Does not clear MV_AGC_DET_ST bit 1 - Clears MV_AGC_DET_ST bit	
MV_CS_DET_CLR			SC
0x49	00000000	Clear bit for Macrovision Color-stripe detected interrupt signal. 0 - Does not clear MV_CS_DET_ST bit 1 - Clears MV_CS_DET_ST bit	
CP_CGMS_CHNGD_CLR			SC
0x49	00000000	Clear bit for CP CGMS Changed interrupt signal. 0 - Does not clear CP_CGMS_CHNGD bit 1 - Clears CP_CGMS_CHNGD bit	
MPU_STIM_INTRQ_MB2			R/W
0x4A	00000000	INT2 interrupt mask for Manual forced interrupt signal. When set the Manual Forced interrupt will trigger the INT2 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status. 0 - Disables Manual forced interrupt for INT2 1 - Enables Manual forced interrupt for INT2	
MV_AGC_DET_MB2			R/W
0x4A	00000000	INT2 interrupt mask for Macrovision AGC detected interrupt signal. When set the Macrovision AGC detected interrupt will trigger the INT2 interrupt and MV_AGC_DET_ST will indicate the interrupt status. 0 - Disables Macrovision AGC detected interrupt for INT2 1 - Enables Macrovision AGC detected interrupt for INT2	
MV_CS_DET_MB2			R/W
0x4A	00000000	INT2 interrupt mask for Macrovision Color-stripe detected interrupt signal. When set the Macrovision Color-stripe detected interrupt will trigger the INT2 interrupt and MV_CS_DET_ST will indicate the interrupt status. 0 - Disables Macrovision CS detected interrupt for INT2 1 - Enables Macrovision CS detected interrupt for INT2	
CP_CGMS_CHNGD_MB2			R/W
0x4A	00000000	INT2 interrupt mask for CP CGMS changed interrupt signal. When set the CP CGMS Changed interrupt will trigger the INT2 interrupt and CP_CGMS_CHNGD_ST will indicate the interrupt status. 0 - Disables CP CGMS changed interrupt for INT2 1 - Enables CP CGMS changed interrupt for INT2	
MPU_STIM_INTRQ_MB1			R/W
0x4B	00000000	INT1 interrupt mask for Manual forced interrupt signal. When set the Manual Forced interrupt will trigger the INT1 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status. 0 - Disables Manual forced interrupt for INT1 1 - Enables Manual forced interrupt for INT1	
MV_AGC_DET_MB1			R/W
0x4B	00000000	INT1 interrupt mask for Macrovision AGC detected interrupt signal. When set the Macrovision AGC detected interrupt will trigger the INT1 interrupt and MV_AGC_DET_ST will indicate the interrupt status. 0 - Disables Macrovision AGC detected interrupt for INT1 1 - Enables Macrovision AGC detected interrupt for INT1	
MV_CS_DET_MB1			R/W
0x4B	00000000	INT1 interrupt mask for Macrovision Color-stripe detected interrupt signal. When set the Macrovision Color-stripe detected interrupt will trigger the INT1 interrupt and MV_CS_DET_ST will indicate the interrupt status. 0 - Disables Macrovision CS detected interrupt for INT1 1 - Enables Macrovision CS detected interrupt for INT1	

Reg	Bits	Description	
CP_CGMS_CHNGD_MB1			R/W
0x4B	00000000	INT1 interrupt mask for CP CGMS changed interrupt signal. When set the CP CGMS Changed interrupt will trigger the INT1 interrupt and CP_CGMS_CHNGD_ST will indicate the interrupt status. 0 - Disables CP CGMS changed interrupt for INT1 1 - Enables CP CGMS changed interrupt for INT1	
AVLINK_RX_READY_RAW			R
0x4C	00000000	Raw status of AV.link Receiver Ready signal. 0 - No change 1 - AV.link Rx has received a complete message which is ready to be read by the host.	
AVLINK_TX_RETRY_TIMEOUT_RAW			R
0x4C	00000000	Raw status of AV.link Transmitter retry timeout signal. 0 - No change to transmitter time-out detected. 1 - AV.link transmitter time-out detected. AV.link TX has tried to send the current message the number of times indicated by the TX_RETRY_REGISTER but it was unsuccessful every time	
AVLINK_TX_ARBITRATION_LOST_RAW			R
0x4C	00000000	Raw status of AV.link transmitter arbitration lost signal. 0 - No AV.link transmitter arbitration loss detected. 1 - AV.link transmitter arbitration loss detected. AV.link Transmitter has lost arbitration to another Transmitter.	
AVLINK_TX_READY_RAW			R
0x4C	00000000	Raw status of AV.link Transmitter 'ready to send message' signal. This bit will be high whenever the TX is ready to send a message. This bit can be used as a "message sent" bit because it will return high when the current message has been sent. 0 - AV.link TX is busy (not ready to send a message) 1 - AV.link TX is ready to send a message	
AVLINK_RX_READY_ST			R
0x4D	00000000	Latched status of AV.link Receiver ready interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AVLINK_RX_READY_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - AV.link message received interrupt has not occurred. 1 - AV.link message received interrupt has occurred.	
AVLINK_TX_RETRY_TIMEOUT_ST			R
0x4D	00000000	Latched status of AVLINK_TX_RETRY_TIMEOUT_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the AV.link TX fails to send the current message within the number of retry attempts specified by AVL_TX_RETRY this bit is set. Once set this bit will remain high until the interrupt has been cleared via AVLINK_TX_RETRY_TIMEOUT_CLR. 0 - No change 1 - AV.link TX has tried but failed to resend the current message for the number of times specified by AVL_TX_RETRY	
AVLINK_TX_ARBITRATION_LOST_ST			R
0x4D	00000000	Latched status of AVLINK_TX_ARBITRATION_LOST_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the AV.link TX loses arbitration while trying to send a message this bit is set. Once set this bit will remain high until the interrupt has been cleared via AVLINK_TX_ARBITRATION_LOST_CLR. 0 - No change 1 - The AV.link TX lost arbitration to another TX	
AVLINK_TX_READY_ST			R
0x4D	00000000	Latched status of AVLINK_TX_READY_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When the AV.link TX successfully sends the current message this bit is set. Once set this bit will remain high until the interrupt has been cleared via AVLINK_TX_READY_CLR. 0 - No change 1 - Message transmitted successfully	
AVLINK_RX_READY_CLR			SC
0x4E	00000000	Clear bit for AV.link Receiver ready interrupt signal. 0 - Does not clear AVLINK_RX_READY_ST 1 - Clears AVLINK_RX_READY_ST	
AVLINK_TX_RETRY_TIMEOUT_CLR			SC
0x4E	00000000	Clear bit for AV.link Transmitter retry timeout interrupt signal. 0 - Does not clear AVLINK_TX_RETRY_TIMEOUT_ST 1 - Clears AVLINK_TX_RETRY_TIMEOUT_ST	
AVLINK_TX_ARBITRATION_LOST_CLR			SC
0x4E	00000000	Clear bit for AV.link Transmitter arbitration loss interrupt signal. 0 - Does not clear AVLINK_TX_ARBITRATION_LOST_ST 1 - Clears AVLINK_TX_ARBITRATION_LOST_ST	

Reg	Bits	Description	
AVLINK_TX_READY_CLR			SC
0x4E	0000000<u>0</u>	Clear bit for AV.link Transmitter ready interrupt signal 0 - Does not clear AVLINK_TX_READY_ST 1 - Clears AVLINK_TX_READY_ST	
AVLINK_RX_READY_MB2			R/W
0x4F	0000<u>0</u>000	INT2 interrupt mask for AV.link Receiver ready interrupt signal. When set the AV.link Receiver ready interrupt will trigger the INT2 interrupt and AVLINK_RX_READY_ST will indicate the interrupt status. 0 - Disables AV.link Receiver ready interrupt for INT2 1 - Enables AV.link Receiver ready interrupt for INT2	
AVLINK_TX_RETRY_TIMEOUT_MB2			R/W
0x4F	00000<u>0</u>00	INT2 interrupt mask for AV.link Transmitter retry timeout interrupt signal. When set the AV.link Transmitter retry timeout interrupt will trigger the INT2 interrupt and AVLINK_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables AV.link Transmitter retry timeout interrupt for INT2 1 - Enables AV.link Transmitter retry timeout interrupt for INT2	
AVLINK_TX_ARBITRATION_LOST_MB2			R/W
0x4F	000000<u>0</u>0	INT2 interrupt mask for AV.link Transmitter arbitration lost interrupt signal. When set the AV.link Transmitter arbitration lost interrupt will trigger the INT2 interrupt and AVLINK_TX_ARBITATION_LOST_ST will indicate the interrupt status. 0 - Disables AV.link Transmitter arbitration lost interrupt for INT2 1 - Enables AV.link Transmitter arbitration lost interrupt for INT2	
AVLINK_TX_READY_MB2			R/W
0x4F	0000000<u>0</u>	INT2 interrupt mask for AV.link Transmitter ready interrupt signal. When set the AV.link Transmitter ready interrupt will trigger the INT2 interrupt and AVLINK_TX_READY_ST will indicate the interrupt status. 0 - Disables AV.link Transmitter ready interrupt for INT2 1 - Enables AV.link Transmitter ready interrupt for INT2	
AVLINK_RX_READY_MB1			R/W
0x50	0000<u>0</u>000	INT1 interrupt mask for AV.link Receiver ready interrupt signal. When set the AV.link Receiver ready interrupt will trigger the INT1 interrupt and AVLINK_RX_READY_ST will indicate the interrupt status. 0 - Disables AV.link Receiver ready interrupt for INT1 1 - Enables AV.link Receiver ready interrupt for INT1	
AVLINK_TX_RETRY_TIMEOUT_MB1			R/W
0x50	00000<u>0</u>00	INT1 interrupt mask for AV.link Transmitter retry timeout interrupt signal. When set the AV.link Transmitter retry timeout interrupt will trigger the INT1 interrupt and AVLINK_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables AV.link Transmitter retry timeout interrupt for INT1 1 - Enables AV.link Transmitter retry timeout interrupt for INT1	
AVLINK_TX_ARBITRATION_LOST_MB1			R/W
0x50	000000<u>0</u>0	INT1 interrupt mask for AV.link Transmitter arbitration lost interrupt signal. When set the AV.link Transmitter arbitration lost interrupt will trigger the INT1 interrupt and AVLINK_TX_ARBITATION_LOST_ST will indicate the interrupt status. 0 - Disables AV.link Transmitter arbitration lost interrupt for INT1 1 - Enables AV.link Transmitter arbitration lost interrupt for INT1	
AVLINK_TX_READY_MB1			R/W
0x50	0000000<u>0</u>	INT1 interrupt mask for AV.link Transmitter ready interrupt signal. When set the AV.link Transmitter ready interrupt will trigger the INT1 interrupt and AVLINK_TX_READY_ST will indicate the interrupt status. 0 - Disables AV.link Transmitter ready interrupt for INT1 1 - Enables AV.link Transmitter ready interrupt for INT1	
TTXT_AVL_RAW			R
0x51	<u>0</u>0000000	Raw status of the Teletext data available signal. 0 - Teletext not detected/available 1 - Teletext detected/available	
VITC_AVL_RAW			R
0x51	0<u>0</u>000000	Raw status of the VITC data available signal 0 - VITC data not detected/available 1 - VITC data detected/available	
GS_DATA_TYPE_RAW			R
0x51	00<u>0</u>00000	Raw status of the GemStar type available signal. 0 - GemStar data type not detected/available 1 - GemStar data type detected/available	

Reg	Bits	Description
GS_PDC_VPS_UTC_AVL_RAW		R
0x51	0000**0**0000	Raw status of the Gemstar/PDC/VPS/UTC data available signal. 0 - GemStar/PDC/VPS/UTC data not detected/available 1 - GemStar/PDC/VPS/UTC data detected/available
FASTI2C_DATA_RDY_RAW		R
0x51	00000**0**00	1 -> Data ready to be read from fast i2c registers
CGMS_WSS_AVL_RAW		R
0x51	000000**0**0	Raw status of the CGMS/WSS data available signal. 0 - CGMS/WSS data not detected/available 1 - CGMS/WSS data detected/available
CCAP_EVEN_FIELD_RAW		R
0x51	0000000**0**	Raw status of the Closed Captioning detected on even field signal 0 - CCAP even field data not detected/available 1 - CCAP even field data detected/available
CCAP_AVL_RAW		R
0x51	00000000**0**	Raw status of the Closed captioning data available signal. 0 - Closed captioning data not available 1 - Closed captioning data available
TTXT_AVL_ST		R
0x52	**0**0000000	Latched status of Teletext data available interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TTXT_AVL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No Teletext data available interrupt event has occurred. 1 - No Teletext data available interrupt event has occurred.
VITC_AVL_ST		R
0x52	0**0**000000	Latched status of VITC data available interrupt signal. Once set this bit will remain high until the interrupt has been cleared via VITC_AVL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No VITC data available interrupt event has occurred. 1 - A VITC data available interrupt event has occurred.
GS_DATA_TYPE_ST		R
0x52	00**0**00000	Latched status of Gemstar type available interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GS_DATA_TYPE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No Gemstar data type interrupt event has occurred. 1 - A Gemstar data type interrupt event has occurred.
GS_PDC_VPS_UTC_AVL_ST		R
0x52	0000**0**000	Latched status of Gemstar/ PDC/ VPS/UTC data available interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GS_PDC_VPS_UTC_AVL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No GemStar/PDC/VPS/UTC data available interrupt event has occurred. 1 - A GemStar/PDC/VPS/UTC data available interrupt event has occurred.
FASTI2C_DATA_RDY_ST		R
0x52	00000**0**00	0 - Positive Edge not detected on FAST_I2C_DATA_RDY 1 - Positive Edge detected on FAST_I2C_DATA_RDY
CGMS_WSS_AVL_ST		R
0x52	000000**0**0	Latched status of CGMS/WSS data available interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CGMS_WSS_AVL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No CGMS/WSS data available interrupt event has occurred. 1 - CGMS/WSS data available interrupt event has occurred.
CCAP_EVEN_FIELD_ST		R
0x52	0000000**0**	Latched status of Closed captioning detected on even field interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CCAP_EVEN_FIELD_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No closed captioning detected on even field interrupt event has occurred. 1 - A closed captioning detected on even field interrupt event has occurred.
CCAP_AVL_ST		R
0x52	00000000**0**	Latched status of Closed captioning data available interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CCAP_AVL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No Closed Captioning data available interrupt event has occurred. 1 - A Closed Captioning data available interrupt event has occurred.

Reg	Bits	Description	
TTXT_AVL_CLR			SC
0x53	00000000	Clear bit for Teletext data available interrupt signal. 0 - Does not clear TTX_AVL_ST 1 - Clear TTX_AVL_ST	
VITC_AVL_CLR			SC
0x53	00000000	Clear bit for VITC data available interrupt signal. 0 - Does not clear VITC_AVL_ST 1 - Clears VITC_AVL_ST	
GS_DATA_TYPE_CLR			SC
0x53	00000000	Clear bit for Gemstar data type interrupt signal. 0 - Does not clear GS_DATA_TYPE_ST 1 - Clears GS_DATA_TYPE_ST	
GS_PDC_VPS_UTC_AVL_CLR			SC
0x53	00000000	Clear bit for Gemstar/PDC/VPS/UTC data available interrupt signal. 0 - Does not clear 1 - Clears GS_VPS_PDC_UTC_AVL_ST	
FASTI2C_DATA_RDY_CLR			SC
0x53	00000000	Clear interrupt on fasti2c_data_rdy	
CGMS_WSS_AVL_CLR			SC
0x53	00000000	Clear bit for CGMS/WSS data available interrupt signal. 0 - Does not clear CGMS_WSS_AVL_ST 1 - Clears CGMS_WSS_AVL_ST	
CCAP_EVEN_FIELD_CLR			SC
0x53	00000000	Clear bit for Closed Captioning detected on interrupt signal. 0 - Does not clear CCAP_EVEN_FIELD_ST 1 - Clears CCAP_EVEN_FIELD_ST	
CCAP_AVL_CLR			SC
0x53	00000000	Clear bit for Closed Captioning data available interrupt signal. 0 - Does not clear CCAP_AVL_ST 1 - Clears CCAP_AVL_ST	
TTXT_AVL_MB2			R/W
0x54	00000000	INT2 interrupt mask for Teletext data available interrupt signal. When set the Teletext data available interrupt will trigger the INT2 interrupt and TTXT_AVL_ST will indicate the interrupt status. 0 - Disables Teletext data available interrupt on INT2 1 - Enables Teletext data available interrupt on INT2	
VITC_AVL_MB2			R/W
0x54	00000000	INT2 interrupt mask for VITC data available interrupt signal. When set the VITC data available interrupt will trigger the INT2 interrupt and VITC_AVL_ST will indicate the interrupt status. 0 - Disables VITC data available interrupt on INT2 1 - Enables VITC data available interrupt on INT2	
GS_DATA_TYPE_MB2			R/W
0x54	00000000	INT2 interrupt mask for Gemstar data type interrupt signal. When set the Gemstar data type available interrupt will trigger the INT2 interrupt and GS_TYPE_ST will indicate the interrupt status. 0 - Disables Gemstar data type interrupt on INT2 1 - Enables Gemstar data type available interrupt on INT2	
GS_PDC_VPS_UTC_AVL_MB2			R/W
0x54	00000000	INT2 interrupt mask for Gemstar/PDC/VPS/UTC data available interrupt signal. When set the Gemstar/PDC/VPS/UTC data available interrupt will trigger the INT2 interrupt and GS_PDC_VPS_UTC_AVL_ST will indicate the interrupt status. 0 - Disables Gemstar/PDC/VPS/UTC data available interrupt on INT2 1 - Enables Gemstar/PDC/VPS/UTC data available interrupt on INT2	
FASTI2C_DATA_RDY_MB2			R/W
0x54	00000000	Enable INT2 on fasti2c_data_rdy	
CGMS_WSS_AVL_MB2			R/W
0x54	00000000	INT2 interrupt mask for CGMS/WSS data available interrupt signal. When set the CGMS/WSS data available interrupt will trigger the INT2 interrupt and GS_TYPE_ST will indicate the interrupt status. 0 - Disables CGMS/WSS data available interrupt on INT2 1 - Enables CGMS/WSS data available interrupt on INT2	

Reg	Bits	Description	
CCAP_EVEN_FIELD_MB2			R/W
0x54	0000000<u>0</u>	INT2 interrupt mask for CCAP Even field detected interrupt signal. When set the CCAP Even field detected interrupt will trigger the INT2 interrupt and CCAP_EVEN_FIELD_ST will indicate the interrupt status. 0 - Disables Closed Caption on even field detected interrupt on INT2 1 - Enables Closed Caption on even field detected interrupt on INT2	
CCAP_AVL_MB2			R/W
0x54	0000000<u>0</u>	INT2 interrupt mask for CCAP data available interrupt signal. When set the CCAP data available interrupt will trigger the INT2 interrupt and CCAP_AVL_ST will indicate the interrupt status. 0 - Disables Closed caption data available interrupt on INT2 1 - Enables Closed caption data available interrupt on INT2	
TTXT_AVL_MB1			R/W
0x55	<u>0</u>0000000	INT1 interrupt mask for Teletext data available interrupt signal. When set the Teletext data available interrupt will trigger the INT1 interrupt and TTXT_AVL_ST will indicate the interrupt status. 0 - Disables Teletext data available interrupt on INT1 1 - Enables Teletext data available interrupt on INT1	
VITC_AVL_MB1			R/W
0x55	0<u>0</u>000000	INT2 interrupt mask for VITC data available interrupt signal. When set the VITC data available interrupt will trigger the INT2 interrupt and VITC_AVL_ST will indicate the interrupt status. 0 - Disables VITC data available interrupt on INT1 1 - Enables VITC data available interrupt on INT1	
GS_DATA_TYPE_MB1			R/W
0x55	00<u>0</u>00000	INT1 interrupt mask for Gemstar data type interrupt signal. When set the Gemstar data type available interrupt will trigger the INT1 interrupt and GS_TYPE_ST will indicate the interrupt status. 0 - Disables Gemstar data type interrupt on INT1 1 - Enables Gemstar data type available interrupt on INT1	
GS_PDC_VPS_UTC_AVL_MB1			R/W
0x55	000<u>0</u>0000	INT1 interrupt mask for Gemstar/PDC/VPS/UTC data available interrupt signal. When set the Gemstar/PDC/VPS/UTC data available interrupt will trigger the INT1 interrupt and GS_PDC_VPS_UTC_AVL_ST will indicate the interrupt status. 0 - Disables Gemstar/PDC/VPS/UTC data available interrupt on INT1 1 - Enables Gemstar/PDC/VPS/UTC data available interrupt on INT1	
FASTI2C_DATA_RDY_MB1			R/W
0x55	0000<u>0</u>000	Enable INT1 on fasti2c_data_rdy	
CGMS_WSS_AVL_MB1			R/W
0x55	00000<u>0</u>00	INT1 interrupt mask for CGMS/WSS data available interrupt signal. When set the CGMS/WSS data available interrupt will trigger the INT1 interrupt and GS_TYPE_ST will indicate the interrupt status. 0 - Disables CGMS/WSS data available interrupt on INT1 1 - Enables CGMS/WSS data available interrupt on INT1	
CCAP_EVEN_FIELD_MB1			R/W
0x55	0000000<u>0</u>	INT1 interrupt mask for CCAP Even field detected interrupt signal. When set the CCAP Even field detected interrupt will trigger the INT1 interrupt and CCAP_EVEN_FIELD_ST will indicate the interrupt status. 0 - Disables Closed Caption on even field detected interrupt on INT1 1 - Enables Closed Caption on even field detected interrupt on INT1	
CCAP_AVL_MB1			R/W
0x55	0000000<u>0</u>	INT1 interrupt mask for CCAP data available interrupt signal. When set the CCAP data available interrupt will trigger the INT1 interrupt and CCAP_AVL_ST will indicate the interrupt status. 0 - Disables Closed caption data available interrupt on INT1 1 - Enables Closed caption data available interrupt on INT1	
SDP_PROGRESSIVE_RAW			R
0x56	<u>0</u>0000000	0 - Progressive vs. interlaced detection by ESDP 1 - Interlaced vs. interlaced detection by ESDP	
SDP_PR_DET_RAW			R
0x56	0<u>0</u>000000	0 - Interlaced video detected by the ESDP block 1 - Progressive video detected by the ESDP block	
SDP_SD_DET_RAW			R
0x56	00<u>0</u>00000	0 - Progressive video detected by the ESDP block 1 - Interlaced video detected by the ESDP block	
SDP_50HZ_DET_RAW			R
0x56	000<u>0</u>0000	0 - 60 Hz signal detected by the ESDP block 1 - 50 Hz signal detected by the ESDP block	

Reg	Bits	Description	
SDP_PROGRESSIVE_ST			R
0x57	0000000	0 - No change. An interrupt has not been generated from this register. 1 - ESDP_PROGRESSIVE_RAW has changed and generated an interrupt.	
SDP_PR_DET_ST			R
0x57	000000	0 - No change. An interrupt has not been generated from this register. 1 - ESDP_PR_DET_RAW has changed and generated an interrupt.	
SDP_SD_DET_ST			R
0x57	00000	0 - No change. An interrupt has not been generated from this register. 1 - ESDP_SD_DET_RAW has changed and generated an interrupt.	
SDP_50HZ_DET_ST			R
0x57	0000	0 - No change. An interrupt has not been generated from this register. 1 - ESDP_50HZ_DET_RAW has changed and generated an interrupt.	
SDP_PROGRESSIVE_CLR			SC
0x58	0000000	0 - Does not clear 1 - Clears ESDP_PROGRESSIVE_ST	
SDP_PR_DET_CLR			SC
0x58	000000	0 - Does not clear 1 - Clears ESDP_PR_DET_ST	
SDP_SD_DET_CLR			SC
0x58	00000	0 - Does not clear 1 - Clears ESDP_SD_DET_ST	
SDP_50HZ_DET_CLR			SC
0x58	0000	0 - Does not clear 1 - Clears ESDP_50HZ_DET_ST	
SDP_PROGRESSIVE_MB2			R/W
0x59	0000000	0 - Disables interrupt on INT2 for ESDP_PROGRESSIVE_DET signal 1 - Enables interrupt on INT2 for ESDP_PR_DET signal	
SDP_PR_DET_MB2			R/W
0x59	000000	0 - Disables interrupt on INT2 for ESDP_PR_DET signal 1 - Enables interrupt on INT2 for ESDP_PROGRESSIVE_DET signal	
SDP_SD_DET_MB2			R/W
0x59	00000	0 - Disables interrupt on INT2 for ESDP_SD_DET signal 1 - Enables interrupt on INT2 for ESDP_SD_DET signal	
SDP_50HZ_DET_MB2			R/W
0x59	0000	0 - Disables interrupt on INT2 for ESDP_50HZ_DET signal 1 - Enables interrupt on INT2 for ESDP_50HZ_DET signal	
SDP_PROGRESSIVE_MB1			R/W
0x5A	0000000	0 - Disables interrupt on INT1 for ESDP_PROGRESSIVE_DET signal 1 - Enables interrupt on INT1 for ESDP_PROGRESSIVE_DET signal	
SDP_PR_DET_MB1			R/W
0x5A	000000	0 - Disables interrupt on INT1 for ESDP_PR_DET signal 1 - Enables interrupt on INT1 for ESDP_PR_DET signal	
SDP_SD_DET_MB1			R/W
0x5A	00000	0 - Disables interrupt on INT1 for ESDP_SD_DET signal 1 - Enables interrupt on INT1 for ESDP_SD_DET signal	
SDP_50HZ_DET_MB1			R/W
0x5A	0000	0 - Disables interrupt on INT1 for ESDP_50HZ_DET signal 1 - Enables interrupt on INT1 for ESDP_50HZ_DET signal	
CP_LOCK_CH2_RAW			R
0x5B	0000000	0 - No change 1 - Channel 2 CP input has changed from an unlocked state to a locked state	
CP_UNLOCK_CH2_RAW			R
0x5B	000000	0 - No change 1 - Channel 2 CP input has changed from a locked state to an unlocked state	
STDI_DVALID_CH2_RAW			R
0x5B	00000	Raw status of STDI Data Valid for sync channel 2 signal. 0 - STDI Data is not valid on sync channel 2 1 - STDI Data is valid on sync channel 2	

Reg	Bits	Description
SSPD_RSLT_CHNGD_CH2_RAW		R
0x5B	0000**0**0000	Status of the SSPD Result Changed on sync channel 2 interrupt signal. When set to 1 it indicates a change in SSPD result of the currently selected sync channel. A change in SSPD result can be either due to a polarity or source change. Once set, this bit will remain high until it is cleared via SSPD_RSLT_CHNGD_CH2_CLR. 0 - No change in the SSPD result for sync channel 2 1 - A change has occurred in SSPD result for sync channel 2
CP_LOCK_CH1_RAW		R
0x5B	00000**0**00	0 - No change 1 - Channel 1 input has changed from an unlocked state to a locked state
CP_UNLOCK_CH1_RAW		R
0x5B	000000**0**0	0 - No change 1 - Channel 1 CP input has changed from a locked state to an unlocked state
STDI_DVALID_CH1_RAW		R
0x5B	0000000**0**	Raw status of STDI Data Valid for sync channel 1 signal. 0 - STDI Data is not valid for sync channel 1 1 - STDI Data is valid for sync channel 1
SSPD_RSLT_CHNGD_CH1_RAW		R
0x5B	0000000**0**	Status of the SSPD Result Changed on sync channel 1 interrupt signal. When set to 1 it indicates a change in SSPD result of the currently selected sync channel. A change in SSPD result can be either due to a polarity or source change. Once set, this bit will remain high until it is cleared via SSPD_RSLT_CHNGD_CH1_CLR. 0 - No change in the SSPD result for sync channel 1 1 - A change has occurred in SSPD result for sync channel 1
CP_LOCK_CH2_ST		R
0x5C	**0**0000000	0 - No change. An interrupt has not been generated from this register. 1 - Channel 2 CP input has caused the decoder to go from an unlocked state to a locked state
CP_UNLOCK_CH2_ST		R
0x5C	0**0**000000	0 - No change. An interrupt has not been generated from this register. 1 - CP input has caused the decoder to go from a locked state to an unlocked state
STDI_DVALID_CH2_ST		R
0x5C	00**0**00000	Latched signal status of STDI valid for sync channel 2 interrupt signal. Once set this bit will remain high until the interrupt has been cleared via STDI_DATA_VALID_CH2_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No STDI valid for sync channel 2 interrupt has occurred. 1 - A STDI valid for sync channel 2 interrupt has occurred.
SSPD_RSLT_CHNGD_CH2_ST		R
0x5C	000**0**0000	Latched signal status of SSPD Result Changed for sync channel 2 interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SSPD_RSLT_CHNGD_CH2_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No SSPD result changed for sync channel 2 interrupt event occurred. 1 - A SSPD result changed for sync channel 2 interrupt event has occurred.
CP_LOCK_CH1_ST		R
0x5C	0000**0**000	0 - No change. An interrupt has not been generated from this register. 1 - Channel 1 CP input has caused the decoder to go from an unlocked state to a locked state
CP_UNLOCK_CH1_ST		R
0x5C	000000**0**0	0 - No change. An interrupt has not been generated from this register. 1 - Channel 1 CP input has changed from a locked state to an unlocked state and has triggered an interrupt
STDI_DVALID_CH1_ST		R
0x5C	0000000**0**	Latched signal status of STDI valid for sync channel 1 interrupt signal. Once set this bit will remain high until the interrupt has been cleared via STDI_DATA_VALID_CH1_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No STDI valid for sync channel 1 interrupt has occurred. 1 - A STDI valid for sync channel 1 interrupt has occurred.
SSPD_RSLT_CHNGD_CH1_ST		R
0x5C	0000000**0**	Latched signal status of SSPD Result Changed for sync channel 1 interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SSPD_RSLT_CHNGD_CH1_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No SSPD result changed for sync channel 1 interrupt event occurred. 1 - A SSPD result changed for sync channel 1 interrupt event has occurred..
CP_LOCK_CH2_CLR		SC
0x5D	**0**0000000	0 - Does not clear 1 - Clears CP_LOCK_CH2_ST

Reg	Bits	Description	
CP_UNLOCK_CH2_CLR			SC
0x5D	0[0]000000	0 - Does not clear 1 - Clears CP_UNLOCK_CH2_ST	
STDI_DVALID_CH2_CLR			SC
0x5D	00[0]00000	Clear bit for STDI Data valid on sync channel 2 interrupt signal. 0 - Does not clear STDI_DATA_VALID_CH2_ST 1 - Clears STDI_DATA_VALID_CH2_ST	
SSPD_RSLT_CHNGD_CH2_CLR			SC
0x5D	000[0]0000	Clear bit for SSPD Result Changed on sync channel 2 interrupt signal. 0 - Does not clear SSPD_RSLT_CHNGD_CH2_ST 1 - Clears SSPD_RSLT_CHNGD_CH2_ST	
CP_LOCK_CH1_CLR			SC
0x5D	0000[0]000	0 - Does not clear 1 - Clears CP_LOCK_CH1_ST	
CP_UNLOCK_CH1_CLR			SC
0x5D	00000[0]00	0 - Does not clear 1 - Clears CP_UNLOCK_CH1_ST	
STDI_DVALID_CH1_CLR			SC
0x5D	000000[0]0	Clear bit for STDI Data valid on sync channel 1 interrupt signal. 0 - Does not clear STDI_DATA_VALID_CH1_ST 1 - Clears STDI_DATA_VALID_CH1_ST	
SSPD_RSLT_CHNGD_CH1_CLR			SC
0x5D	0000000[0]	Clear bit for SSPD Result Changed on sync channel 1 interrupt signal. 0 - Does not clear SSPD_RSLT_CHNGD_CH1_ST 1 - Clears SSPD_RSLT_CHNGD_CH1_ST	
CP_LOCK_CH2_MB2			R/W
0x5E	[0]0000000	0 - Masks CP_LOCK_CH2_ST 1 - Unmasks CP_LOCK_CH2_ST	
CP_UNLOCK_CH2_MB2			R/W
0x5E	0[0]000000	0 - Masks CP_UNLOCK_CH2_ST 1 - Unmasks CP_UNLOCK_CH2_ST	
STDI_DVALID_CH2_MB2			R/W
0x5E	00[0]00000	INT2 interrupt mask for STDI Data valid for sync channel 2 interrupt. When set the STDI Data valid for sync channel 2 interrupt will trigger the INT2 interrupt and STDI_DATA_VALID_CH2_ST will indicate the interrupt status. 0 - Disables STDI Data valid for sync channel 2 interrupt for INT2 1 - Enables STDI Data valid for sync channel 2 interrupt for INT2	
SSPD_RSLT_CHNGD_CH2_MB2			R/W
0x5E	000[0]0000	INT2 interrupt mask for SSPD Result Changed on sync channel 2 interrupt. When set the SSPD Result changed for sync channel 2 interrupt will trigger the INT2 interrupt and SSPD_RSLT_CHNGD_CH2_ST will indicate the interrupt status. 0 - Disables SSPD Changed for sync channel 2 interrupt for INT2 1 - Enables SSPD Changed for sync channel 2 interrupt for INT2	
CP_LOCK_CH1_MB2			R/W
0x5E	0000[0]000	0 - Masks CP_LOCK_CH1_ST 1 - Unmasks CP_LOCK_CH1_ST	
CP_UNLOCK_CH1_MB2			R/W
0x5E	00000[0]00	0 - Masks CP_UNLOCK_CH1_ST 1 - Unmasks CP_UNLOCK_CH1_ST	
STDI_DVALID_CH1_MB2			R/W
0x5E	000000[0]0	INT2 interrupt mask for STDI Data valid for sync channel 1 interrupt. When set the STDI Data valid for sync channel 1 interrupt will trigger the INT2 interrupt and STDI_DATA_VALID_CH1_ST will indicate the interrupt status. 0 - Disables STDI Data valid for sync channel 1 interrupt for INT2 1 - Enables STDI Data valid for sync channel 1 interrupt for INT2	
SSPD_RSLT_CHNGD_CH1_MB2			R/W
0x5E	0000000[0]	INT2 interrupt mask for SSPD Result Changed on sync channel 1 interrupt. When set the SSPD Result changed for sync channel 2 interrupt will trigger the INT2 interrupt and SSPD_RSLT_CHNGD_CH1_ST will indicate the interrupt status. 0 - Disables SSPD Changed for sync channel 1 interrupt for INT2 1 - Enables SSPD Changed for sync channel 1 interrupt for INT2	
CP_LOCK_CH2_MB1			R/W
0x5F	[0]0000000	0 - Masks CP_LOCK_CH2_ST 1 - Unmasks CP_LOCK_CH2_ST	

Reg	Bits	Description	
CP_UNLOCK_CH2_MB1			R/W
0x5F	0**0**000000	0 - Masks CP_UNLOCK_CH2_ST 1 - Unmasks CP_UNLOCK_CH2_ST	
STDI_DVALID_CH2_MB1			R/W
0x5F	00**0**00000	INT1 interrupt mask for STDI Data valid for sync channel 2 interrupt. When set the STDI Data valid for sync channel 2 interrupt will trigger the INT1 interrupt and STDI_DATA_VALID_CH2_ST will indicate the interrupt status. 0 - Disables STDI Data valid for sync channel 2 interrupt for INT1 1 - Enables STDI Data valid for sync channel 2 interrupt for INT1	
SSPD_RSLT_CHNGD_CH2_MB1			R/W
0x5F	000**0**0000	INT1 interrupt mask for SSPD Result Changed on sync channel 2 interrupt. When set the SSPD Result changed for sync channel 2 interrupt will trigger the INT1 interrupt and SSPD_RSLT_CHNGD_CH2_ST will indicate the interrupt status. 0 - Disables SSPD Changed for sync channel 2 interrupt for INT1 1 - Enables SSPD Changed for sync channel 2 interrupt for INT1	
CP_LOCK_CH1_MB1			R/W
0x5F	0000**0**000	0 - Masks CP_LOCK_CH1_ST 1 - Unmasks CP_LOCK_CH1_ST	
CP_UNLOCK_CH1_MB1			R/W
0x5F	00000**0**00	0 - Masks CP_UNLOCK_CH1_ST 1 - Unmasks CP_UNLOCK_CH1_ST	
STDI_DVALID_CH1_MB1			R/W
0x5F	000000**0**0	INT1 interrupt mask for STDI Data valid for sync channel 1 interrupt. When set the STDI Data valid for sync channel 1 interrupt will trigger the INT1 interrupt and STDI_DATA_VALID_CH1_ST will indicate the interrupt status. 0 - Disables STDI Data valid for sync channel 1 interrupt for INT1 1 - Enables STDI Data valid for sync channel 1 interrupt for INT1	
SSPD_RSLT_CHNGD_CH1_MB1			R/W
0x5F	0000000**0**	INT1 interrupt mask for SSPD Result Changed on sync channel 1 interrupt. When set the SSPD Result changed for sync channel 2 interrupt will trigger the INT1 interrupt and SSPD_RSLT_CHNGD_CH1_ST will indicate the interrupt status. 0 - Disables SSPD Changed for sync channel 1 interrupt for INT1 1 - Enables SSPD Changed for sync channel 1 interrupt for INT1	
ISRC2_PCKT_RAW			R
0x60	**0**0000000	Raw status signal of International Standard Recording Code 2 (ISRC2) Packet detection signal. 0 - No ISRC2 packets received since the last HDMI packet detection reset. 1 - ISRC2 packets have been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to ISRC2_PACKET_ID.	
ISRC1_PCKT_RAW			R
0x60	0**0**000000	Raw status signal of International Standard Recording Code 1 (ISRC1) Packet detection signal. 0 - No ISRC1 packets received since the last HDMI packet detection reset. 1 - ISRC1 packets have been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to ISRC1_PACKET_ID.	
ACP_PCKT_RAW			R
0x60	00**0**00000	Raw status signal of Audio Content Protection Packet detection signal. 0 - No ACP packet received within the last 600 ms or since the last HDMI packet detection reset. 1 - ACP packets have been received within the last 600 ms. This bit will reset to zero after an HDMI packet detection reset or upon writing to ACP_PACKET_ID.	
VS_INFO_RAW			R
0x60	000**0**0000	Raw status signal of Vendor specific Infoframe detection signal. 0 - No new VS infoframe has been received since the last HDMI packet detection reset. 1 - A new VS infoframe has been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to VS_PACKET_ID.	
MS_INFO_RAW			R
0x60	0000**0**000	Raw status signal of MPEG Source Infoframe detection signal. 0 - No source product description Infoframe received within the last three VSyncs or since the last HDMI packet detection reset. 1 - MPEG Source InfoFrame received. This bit will reset to zero after an HDMI packet detection reset or upon writing to MS_PACKET_ID.	
SPD_INFO_RAW			R
0x60	00000**0**00	Raw status of SPD Infoframe detected signal. 0 - No source product description InfoFrame received since the last HDMI packet detection reset. 1 - Source product description InfoFrame received. This bit will reset to zero after an HDMI packet detection reset or upon writing to SPD_PACKET_ID.	

Reg	Bits	Description	
AUDIO_INFO_RAW			R
0x60	0000000<u>0</u>	Raw status of Audio InfoFrame detected signal. 0 - No AVI InfoFrame has been received within the last three VSyncs or since the last HDMI packet detection reset. 1 - An Audio InfoFrame has been received within the last three VSyncs. This bit will reset to zero on the fourth VSync leading edge following an Audio InfoFrame, after an HDMI packet detection reset or upon writing to AUD_PACKET_ID.	
AVI_INFO_RAW			R
0x60	0000000<u>0</u>	Raw status of AVI InfoFrame detected signal. This bit is set to one when an AVI InfoFrame is received and is reset to zero if no AVI InfoFrame is received for more than 7 VSyncs (on the eighth VSync leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID. 0 - No AVI InfoFrame has been received within the last seven VSyncs or since the last HDMI packet detection reset 1 - An AVI InfoFrame has been received within the last seven VSyncs	
ISRC2_PCKT_ST			R
0x61	<u>0</u>0000000	Latched status of ISRC2 Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ISRC2_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ISRC2_PCKT_RAW has changed. Interrupt has been generated.	
ISRC1_PCKT_ST			R
0x61	0<u>0</u>000000	Latched status of ISRC1 Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ISRC1_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ISRC1_PCKT_RAW has changed. Interrupt has been generated.	
ACP_PCKT_ST			R
0x61	00<u>0</u>00000	Latched status of Audio Content Protection Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ACP_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ACP_PCKT_RAW has changed. Interrupt has been generated.	
VS_INFO_ST			R
0x61	000<u>0</u>0000	Latched status of Vendor Specific Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via VS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - VS_INFO_RAW has changed. Interrupt has been generated.	
MS_INFO_ST			R
0x61	0000<u>0</u>000	Latched status of MPEG Source Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - MS_INFO_RAW has changed. Interrupt has been generated.	
SPD_INFO_ST			R
0x61	00000<u>0</u>00	Latched status of SPD Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SPD_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - SPD_INFO_RAW has changed. Interrupt has been generated.	
AUDIO_INFO_ST			R
0x61	000000<u>0</u>0	Latched status of Audio Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - AUDIO_INFO_RAW has changed. Interrupt has been generated.	
AVI_INFO_ST			R
0x61	0000000<u>0</u>	Latched status of AVI_INFO_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set this bit will remain high until the interrupt has been cleared via AVI_INFO_CLR. 0 - AVI_INFO_RAW has not changed state 1 - AVI_INFO_RAW has changed state	
ISRC2_PCKT_CLR			SC
0x62	<u>0</u>0000000	Clear bit for ISRC2 Packet detection interrupt signal. 0 - Does not clear 1 - Clears ISRC1_PCKT_ST	
ISRC1_PCKT_CLR			SC
0x62	0<u>0</u>000000	Clear bit for ISRC1 Packet detection interrupt signal. 0 - Does not clear ISRC1_INFO_ST 1 - Clears ISRC1_INFO_ST	

Reg	Bits	Description	
ACP_PCKT_CLR			SC
0x62	00**0**00000	Clear bit for Audio Content Protection Packet detected interrupt signal. 0 - Does not clear ACP_INFO_ST 1 - Clears ACP_INFO_ST	
VS_INFO_CLR			SC
0x62	000**0**0000	Clear bit for Vendor Specific Infoframe interrupt signal. 0 - Does not clear VS_INFO_ST 1 - Clears VS_INFO_ST	
MS_INFO_CLR			SC
0x62	0000**0**000	Clear bit for MPEG Source Infoframe interrupt signal. 0 - Does not clear MS_INFO_ST 1 - Clears MS_INFO_ST	
SPD_INFO_CLR			SC
0x62	00000**0**00	Clear bit for SPD Infoframe interrupt signal. 0 - Does not clear SPD_INFO_ST 1 - Clears SPD_INFO_ST	
AUDIO_INFO_CLR			SC
0x62	000000**0**0	Clear bit for Audio Infoframe interrupt signal. 0 - Does not clear AUDIO_INFO_ST 1 - Clears AUDIO_INFO_ST	
AVI_INFO_CLR			SC
0x62	0000000**0**	Clear bit for AVI_INFO_RAW and AVI_INFO_ST bits. 0 - No function 1 - Clear AVI_INFO_RAW and AVI_INFO_ST	
ISRC2_PCKT_MB2			R/W
0x63	**0**0000000	INT2 interrupt mask for ISRC2 Packet detection interrupt. When set the ISRC2 Packet detection interrupt will trigger the INT2 interrupt and ISRC2_INFO_ST will indicate the interrupt status. 0 - Disables ISRC2 Infoframe detection interrupt for INT2 1 - Enables ISRC2 Infoframe detection interrupt for INT2	
ISRC1_PCKT_MB2			R/W
0x63	0**0**000000	INT2 interrupt mask for ISRC1 Packet detection interrupt. When set the ISRC1 Packet detection interrupt will trigger the INT2 interrupt and ISRC1_INFO_ST will indicate the interrupt status. 0 - Disables ISRC1 Infoframe detection interrupt for INT2 1 - Enables ISRC1 Infoframe detection interrupt for INT2	
ACP_PCKT_MB2			R/W
0x63	00**0**00000	INT2 interrupt mask for Audio Content Protection Packet detection interrupt. When set the Audio Content Protection Infoframe detection interrupt will trigger the INT2 interrupt and ACP_INFO_ST will indicate the interrupt status. 0 - Disables Audio Content Protection Infoframe detection interrupt for INT2 1 - Enables Audio Content Protection Infoframe detection interrupt for INT2	
VS_INFO_MB2			R/W
0x63	000**0**0000	INT2 interrupt mask for Vendor Specific Infoframe detection interrupt. When set the Vendor Specific Infoframe detection interrupt will trigger the INT2 interrupt and VS_INFO_ST will indicate the interrupt status. 0 - Disables Vendor Specific Infoframe detection interrupt for INT2 1 - Enables Vendor Specific Infoframe detection interrupt for INT2	
MS_INFO_MB2			R/W
0x63	0000**0**000	INT2 interrupt mask for MPEG source Infoframe detection interrupt. When set the MPEG Source Infoframe detection interrupt will trigger the INT2 interrupt and MS_INFO_ST will indicate the interrupt status. 0 - Disables MPEG source Info frame detection interrupt for INT2 1 - Enables MPEG source Info frame detection interrupt for INT2	
SPD_INFO_MB2			R/W
0x63	00000**0**00	INT2 interrupt mask for SPD Infoframe detection interrupt. When set the SPD Infoframe detection interrupt will trigger the INT2 interrupt and SPD_INFO_ST will indicate the interrupt status. 0 - Disables SPD Info frame detection interrupt for INT2 1 - Enables SPD Info frame detection interrupt for INT2	
AUDIO_INFO_MB2			R/W
0x63	000000**0**0	INT2 interrupt mask for Audio Infoframe detection interrupt. When set the Audio Infoframe detection interrupt will trigger the INT2 interrupt and AVI_INFO_ST will indicate the interrupt status. 0 - Disables AUDIO Info frame detection interrupt for INT2 1 - Enables AUDIO Info frame detection interrupt for INT2	

Reg	Bits	Description	
AVI_INFO_MB2			R/W
0x63	0000000<u>0</u>	INT2 interrupt mask for AVI Infoframe detection interrupt. When set an AVI Infoframe detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT2. 0 - Disables AVI Info frame detection interrupt for INT2 1 - Enables AVI Info frame detection interrupt for INT2	
ISRC2_PCKT_MB1			R/W
0x64	<u>0</u>0000000	INT1 interrupt mask for ISRC2 Infoframe detection interrupt. When set the ISRC2 Infoframe detection interrupt will trigger the INT1 interrupt and ISRC2_INFO_ST will indicate the interrupt status. 0 - Disables ISRC2 Packet detection interrupt for INT1 1 - Enables ISRC2 Packet detection interrupt for INT1	
ISRC1_PCKT_MB1			R/W
0x64	0<u>0</u>000000	INT1 interrupt mask for ISRC1 Infoframe detection interrupt. When set the ISRC1 Infoframe detection interrupt will trigger the INT1 interrupt and ISRC1_INFO_ST will indicate the interrupt status. 0 - Disables ISRC1 Infoframe detection interrupt for INT1 1 - Enables ISRC1 Infoframe detection interrupt for INT1	
ACP_PCKT_MB1			R/W
0x64	00<u>0</u>00000	INT1 interrupt mask for Audio Content Protection Packet detection interrupt. When set the Audio Content Protection Packet detection interrupt will trigger the INT1 interrupt and ACP_INFO_ST will indicate the interrupt status. 0 - Disables Audio Content Protection Infoframe detection interrupt for INT1 1 - Enables Audio Content Protection Infoframe detection interrupt for INT1	
VS_INFO_MB1			R/W
0x64	000<u>0</u>0000	INT1 interrupt mask for Vendor Specific Infoframe detection interrupt. When set the Vendor Specific Infoframe detection interrupt will trigger the INT1 interrupt and VS_INFO_ST will indicate the interrupt status. 0 - Disables Vendor Specific Infoframe detection interrupt for INT1 1 - Enables Vendor Specific Infoframe detection interrupt for INT1	
MS_INFO_MB1			R/W
0x64	0000<u>0</u>000	INT1 interrupt mask for MPEG source Infoframe detection interrupt. When set the MPEG source Infoframe detection interrupt will trigger the INT1 interrupt and MS_INFO_ST will indicate the interrupt status. 0 - Disables MPEG source Infoframe detection interrupt for INT1 1 - Enables MPEG source Infoframe detection interrupt for INT1	
SPD_INFO_MB1			R/W
0x64	00000<u>0</u>00	INT1 interrupt mask for SPD Infoframe detection interrupt. When set the SPD Infoframe detection interrupt will trigger the INT1 interrupt and SPD_INFO_ST will indicate the interrupt status. 0 - Disables SPD Info frame detection interrupt for INT1 1 - Enables SPD Info frame detection interrupt for INT1	
AUDIO_INFO_MB1			R/W
0x64	000000<u>0</u>0	INT1 interrupt mask for Audio Infoframe detection interrupt. When set the Audio Infoframe detection interrupt will trigger the INT1 interrupt and AVI_INFO_ST will indicate the interrupt status. 0 - Disables AUDIO Info frame detection interrupt for INT1 1 - Enables AUDIO Info frame detection interrupt for INT1	
AVI_INFO_MB1			R/W
0x64	0000000<u>0</u>	INT1 interrupt mask for AVI Infoframe detection interrupt. When set an AVI Infoframe detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT1. 0 - Disables AVI Info frame detection interrupt for INT1 1 - Enables AVI Info frame detection interrupt for INT1	
CS_DATA_VALID_RAW			R
0x65	<u>0</u>0000000	Raw status signal of Channel Status Data Valid signal. 0 - Channel status data is not valid 1 - Channel status data is valid	
INTERNAL_MUTE_RAW			R
0x65	0<u>0</u>000000	Raw status signal of Internal Mute signal. 0 - Audio is not muted 1 - Audio is muted	
AV_MUTE_RAW			R
0x65	00<u>0</u>00000	Raw status signal of AV Mute detection signal. 0 - No AV mute raw received since last HDMI reset condition 1 - AV mute received	

Reg	Bits	Description	
AUDIO_CH_MD_RAW			R
0x65	0000**0**0000	Raw status signal indicating the layout value of the audio packets that were last received 0 - The last audio packets received have a layout value of 1. (e.g. Layout-1 corresponds to 2-channel audio when Audio Sample packets are received). 1 - The last audio packets received have a layout value of 0 (e.g. Layout-0 corresponds to 8-channel audio when Audio Sample packets are received).	
HDMI_MODE_RAW			R
0x65	00000**0**000	Raw status signal of HDMI Mode signal. 0 - DVI is being received 1 - HDMI is being received	
GEN_CTL_PCKT_RAW			R
0x65	000000**0**00	Raw status signal of General Control Packet detection signal. 0 - No general control packets received since the last HDMI reset condition 1 - General control packets received	
AUDIO_C_PCKT_RAW			R
0x65	0000000**0**0	Raw status signal of Audio Clock Regeneration Packet detection signal. 0 - No audio clock regeneration packets received since the last HDMI reset condition 1 - Audio clock regeneration packets received	
GAMUT_MDATA_RAW			R
0x65	00000000**0**	Raw status signal of Gamut Metadata Packet detection signal. 0 - No Gamut Metadata packet has been received in the last video frame or since the last HDMI packet detection reset. 1 - A Gamut Metadata packet has been received in the last video frame. This bit will reset to zero after an HDMI packet detection reset or upon writing to GAMUT_PACKET_ID.	
CS_DATA_VALID_ST			R
0x66	**0**0000000	Latched status of Channel Status Data Valid interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CS_DATA_VALID_CLR. This bit is only valid if enabled via the corresponding the INT1 or INT2 interrupt mask bit 0 - CS_DATA_VALID_RAW has not changed. An interrupt has not been generated. 1 - CS_DATA_VALID_RAW has changed. An interrupt has been generated.	
INTERNAL_MUTE_ST			R
0x66	0**0**000000	Latched status of Internal Mute interrupt signal. Once set this bit will remain high until the interrupt has been cleared via INTERNAL_MUTE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - INTERNAL_MUTE_RAW has not changed. An interrupt has not been generated. 1 - INTERNAL_MUTE_RAW has changed. An interrupt has been generated.	
AV_MUTE_ST			R
0x66	00**0**00000	Latched status of AV Mute detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AV_MUTE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - AV_MUTE_RAW has not changed. An interrupt has not been generated. 1 - AV_MUTE_RAW has changed. An interrupt has been generated.	
AUDIO_CH_MD_ST			R
0x66	0000**0**0000	Latched status of Audio Channel mode interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_CH_MD_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - AUDIO_CH_MD_RAW has not changed. An interrupt has not been generated. 1 - AUDIO_MODE_CHNG_RAW has changed. An interrupt has been generated.	
HDMI_MODE_ST			R
0x66	00000**0**000	Latched status of HDMI Mode interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_MODE_CLR. This bit is only valid if enabled via the corresponding the INT1 or INT2 interrupt mask bit 0 - HDMI_MODE_RAW has not changed. An interrupt has not been generated. 1 - HDMI_MODE_RAW has changed. An interrupt has been generated.	
GEN_CTL_PCKT_ST			R
0x66	000000**0**00	Latched status of General Control Packet interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GEN_CTL_PCKT_CLR. This bit is only valid if enabled via the corresponding the INT1 or INT2 interrupt mask bit. 0 - GEN_CTL_PCKT_RAW has not changed. Interrupt has not been generated from this register. 1 - GEN_CTL_PCKT_RAW has changed. Interrupt has been generated from this register.	

Reg	Bits	Description	
AUDIO_C_PCKT_ST			R
0x66	0000000**0**	Latched status of Audio Clock Regeneration Packet interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_PCKT_CLR. This bit is only valid if enabled via the corresponding the INT1 or INT2 interrupt mask bit 0 - AUDIO_C_PCKT_RAW has not changed. Interrupt has not been generated from this register 1 - AUDIO_C_PCKT_RAW has changed. Interrupt has been generated from this register.	
GAMUT_MDATA_ST			R
0x66	0000000**0**	Latched status of Gamut Metadata Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via the corresponding the INT1 or INT2 interrupt mask bit 0 - GAMUT_MDATA_RAW has not changed. Interrupt has not been generated from this register 1 - GAMUT_MDATA_RAW has changed. Interrupt has been generated from this register.	
CS_DATA_VALID_CLR			SC
0x67	**0**0000000	Clear bit for Channel Status Data Valid interrupt signal. 0 - Does not clear 1 - Clears CS_DATA_VALID_ST	
INTERNAL_MUTE_CLR			SC
0x67	0**0**000000	Clear bit for Internal Mute interrupt signal. 0 - Does not clear INTERNAL_MUTE_ST 1 - Clears INTERNAL_MUTE_ST	
AV_MUTE_CLR			SC
0x67	00**0**00000	Clear bit for AV Mute Detected interrupt signal. 0 - Does not clear AV_MUTE_ST 1 - Clears AV_MUTE_ST	
AUDIO_CH_MD_CLR			SC
0x67	000**0**0000	Clear bit for Audio Channel mode interrupt signal. 0 - Does not clear AUDIO_CH_MD_ST 1 - Clears AUDIO_CH_MD_ST	
HDMI_MODE_CLR			SC
0x67	0000**0**000	Clear bit for HDMI Mode interrupt signal. 0 - Does not clear HDMI_MODE_ST 1 - Clears HDMI_MODE_ST	
GEN_CTL_PCKT_CLR			SC
0x67	00000**0**00	Clear bit for General Control Packet detection interrupt signal. 0 - Does not clear GEN_CTL_PCKT_ST 1 - Clears GEN_CTL_PCKT_ST	
AUDIO_C_PCKT_CLR			SC
0x67	000000**0**0	Clear bit for Audio Clock Regeneration Packet detection interrupt signal. 0 - Does not clear AUDIO_C_PCKT_ST 1 - Clears AUDIO_C_PCKT_ST	
GAMUT_MDATA_CLR			SC
0x67	0000000**0**	Clear bit for Gamut Metadata Packet detection interrupt signal. 0 - Does not clear GAMUT_MDATA_ST 1 - Clears GAMUT_MDATA_ST	
CS_DATA_VALID_MB2			R/W
0x68	**0**0000000	INT2 interrupt mask for Channel Status Data Valid interrupt. When set the Channel Status Data Valid interrupt will trigger the INT2 interrupt and CS_DATA_VALID_ST will indicate the interrupt status. 0 - Disables Channel Status Data Valid interrupt for INT2 1 - Enables Channel Status Data Valid interrupt for INT2	
INTERNAL_MUTE_MB2			R/W
0x68	0**0**000000	INT2 interrupt mask for Internal Mute interrupt. When set the Internal Mute interrupt will trigger the INT2 interrupt and INTERNAL_MUTE_ST will indicate the interrupt status. 0 - Disables Internal Mute interrupt for INT2 1 - Enables Internal Mute interrupt for INT2	
AV_MUTE_MB2			R/W
0x68	00**0**00000	INT2 interrupt mask for AV Mute detected interrupt. When set the AV Mute detected interrupt will trigger the INT2 interrupt and AV_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT2 1 - Enables AV Mute detected interrupt for INT2	

Reg	Bits	Description
AUDIO_CH_MD_MB2		R/W
0x68	0000**0**0000	INT2 interrupt mask for Audio Channel mode interrupt. When set the Audio Channel mode interrupt will trigger the INT2 interrupt and AUDIO_CH_MD_ST will indicate the interrupt status. 0 - Disables Audio Channel Mode interrupt for INT2 1 - Enables Audio Channel Mode interrupt for INT2
HDMI_MODE_MB2		R/W
0x68	0000**0**000	INT2 interrupt mask for HDMI Mode interrupt. When set the HDMI Mode interrupt will trigger the INT2 interrupt and HDMI_MODE_ST will indicate the interrupt status. 0 - Disables HDMI Mode interrupt for INT2 1 - Enables HDMI Mode interrupt for INT2
GEN_CTL_PCKT_MB2		R/W
0x68	00000**0**00	INT2 interrupt mask for General Control Packet detection interrupt. When set the General Control Packet detection interrupt will trigger the INT2 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables General Control Packet detection interrupt for INT2 1 - Enables General Control Packet detection interrupt for INT2
AUDIO_C_PCKT_MB2		R/W
0x68	000000**0**0	INT2 interrupt mask for Audio Clock Regeneration Packet detection interrupt. When set the Audio Clock Regeneration Packet detection interrupt will trigger the INT2 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables Audio Clock Regeneration Packet detection interrupt for INT2 1 - Enables Audio Clock Regeneration Packet detection interrupt for INT2
GAMUT_MDATA_MB2		R/W
0x68	0000000**0**	INT2 interrupt mask for Gamut Metadata Packet detection interrupt. When set the Gamut Metadata Packet detection interrupt will trigger the INT2 interrupt and GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables Gamut Metadata Packet detection interrupt for INT2 1 - Enables Gamut Metadata Packet detection interrupt for INT2
CS_DATA_VALID_MB1		R/W
0x69	**0**0000000	INT1 interrupt mask for Channel Status Data Valid interrupt. When set the Channel Status Data Valid interrupt will trigger the INT1 interrupt and CS_DATA_VALID_ST will indicate the interrupt status. 0 - Disables Channel Status Data Valid interrupt for INT1 1 - Enables Channel Status Data Valid interrupt for INT1
INTERNAL_MUTE_MB1		R/W
0x69	0**0**000000	INT1 interrupt mask for Internal Mute interrupt. When set the Internal Mute interrupt will trigger the INT1 interrupt and INTERNAL_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT1 1 - Enables AV Mute detected interrupt for INT1
AV_MUTE_MB1		R/W
0x69	00**0**00000	INT1 interrupt mask for AV Mute detected interrupt. When set the AV Mute detected interrupt will trigger the INT1 interrupt and AV_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT1 1 - Enables AV Mute detected interrupt for INT1
AUDIO_CH_MD_MB1		R/W
0x69	0000**0**0000	INT1 interrupt mask for Audio Channel mode interrupt. When set the Audio Channel mode interrupt will trigger the INT1 interrupt and AUDIO_CH_MD_ST will indicate the interrupt status. 0 - Disables Audio Channel Mode interrupt for INT1 1 - Enables Audio Channel Mode interrupt for INT1
HDMI_MODE_MB1		R/W
0x69	0000**0**000	INT1 interrupt mask for HDMI Mode detection interrupt. When set the HDMI Mode interrupt will trigger the INT1 interrupt and HDMI_MODE_ST will indicate the interrupt status. 0 - Disables HDMI Mode interrupt for INT1 1 - Enables HDMI Mode interrupt for INT1
GEN_CTL_PCKT_MB1		R/W
0x69	00000**0**00	INT1 interrupt mask for General Control Packet detection interrupt. When set the General Control Packet detection interrupt will trigger the INT1 interrupt and GEN_CTL_PCKT_ST will indicate the interrupt status. 0 - Disables General Control Packet detection interrupt for INT1 1 - Enables General Control Packet detection interrupt for INT1
AUDIO_C_PCKT_MB1		R/W
0x69	000000**0**0	INT1 interrupt mask for Audio Clock Regeneration Packet detection interrupt. When set the Audio Clock Regeneration Packet detection interrupt will trigger the INT1 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables Audio Clock Regeneration Packet detection interrupt for INT1 1 - Enables Audio Clock Regeneration Packet detection interrupt for INT1

Reg	Bits	Description	
GAMUT_MDATA_MB1			R/W
0x69	0000000<u>0</u>	INT1 interrupt mask for Gamut Metadata Packet detection interrupt. When set the Gamut Metadata Packet detection interrupt will trigger the INT1 interrupt and GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables Gamut Metadata Packet detection interrupt for INT1 1 - Enables Gamut Metadata Packet detection interrupt for INT1	
TMDSPLL_LCK_A_RAW			R
0x6A	00<u>0</u>00000	A readback to indicate the raw status of the Port A TMDS PLL lock signal. 0 - TMDS PLL on Port A is not locked. 1 - TMDS PLL on Port A is locked to the incoming clock.	
TMDSPLL_LCK_B_RAW			R
0x6A	000<u>0</u>0000	A readback to indicate the raw status of the port B TMDS PLL lock signal. 0 - TMDS PLL on Port B is not locked. 1 - TMDS PLL on Port B is locked to the incoming clock.	
TMDS_CLK_A_RAW			R
0x6A	000000<u>0</u>0	Raw status of Port A TMDS Clock detection signal. 0 - No TMDS clock detected on Port A 1 - TMDS clock detected on Port A.	
TMDS_CLK_B_RAW			R
0x6A	0000000<u>0</u>	Raw status of Port B TMDS Clock detection signal. 0 - No TMDS clock detected on Port B 1 - TMDS clock detected on Port B.	
TMDSPLL_LCK_A_ST			R
0x6B	00<u>0</u>00000	Latched status of Port A TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDSPLL_LCK_A_RAW has not changed. An interrupt has not been generated 1 - TMDSPLL_LCK_A_RAW has changed. An interrupt has been generated.	
TMDSPLL_LCK_B_ST			R
0x6B	000<u>0</u>0000	Latched status of Port B TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDSPLL_LCK_B_RAW has not changed. An interrupt has not been generated. 1 - TMDSPLL_LCK_B_RAW has changed. An interrupt has been generated.	
TMDS_CLK_A_ST			R
0x6B	000000<u>0</u>0	Latched status of Port A TMDS Clock Detection interrupt signal .Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDS_CLK_A_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_A_RAW has changed. An interrupt has been generated.	
TMDS_CLK_B_ST			R
0x6B	0000000<u>0</u>	Latched status of Port B TMDS Clock Detection interrupt signal .Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - TMDS_CLK_B_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_B_RAW has changed. An interrupt has been generated.	
TMDSPLL_LCK_A_CLR			SC
0x6C	00<u>0</u>00000	Clear bit for Port A TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_A_ST. 1 - Clears TMDSPLL_LCK_A_ST.	
TMDSPLL_LCK_B_CLR			SC
0x6C	000<u>0</u>0000	Clear bit for Port B TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_B_ST. 1 - Clears TMD.SPLL_LCK_B_ST.	
TMDS_CLK_A_CLR			SC
0x6C	000000<u>0</u>0	Clear bit for Port A TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_A_ST. 1 - Clears TMDS_CLK_A_ST.	
TMDS_CLK_B_CLR			SC
0x6C	0000000<u>0</u>	Clear bit for Port B TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_B_ST. 1 - Clears TMDS_CLK_B_ST.	

Reg	Bits	Description
TMDSPLL_LCK_A_MB2		R/W
0x6D	00<u>0</u>00000	INT2 interrupt mask for Port A TMDS PLL Lock interrupt. When set the Port A TMDS PLL Lock interrupt will trigger the INT2 interrupt and TMDSPLL_LCK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDSPLL Lock interrupt for INT2. 1 - Enables Port A TMDSPLL Lock interrupt for INT2.
TMDSPLL_LCK_B_MB2		R/W
0x6D	000<u>0</u>0000	INT2 interrupt mask for Port B TMDS PLL Lock interrupt. When set the Port B TMDS PLL Lock interrupt will trigger the INT2 interrupt and TMDSPLL_LCK_B_ST will indicate the interrupt status. 0 - Disables Port B TMDSPLL Lock interrupt for INT2. 1 - Enables Port B TMDSPLL Lock interrupt for INT2.
TMDS_CLK_A_MB2		R/W
0x6D	0000000<u>0</u>	INT2 interrupt mask for Port A TMDS Clock detection interrupt. When set the Port A TMDS Clock detection interrupt will trigger the INT2 interrupt and TMDS_CLK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDS Clock Detection interrupt for INT2 1 - Enables Port A TMDS Clock Detection interrupt for INT2.
TMDS_CLK_B_MB2		R/W
0x6D	0000000<u>0</u>	INT2 interrupt mask for Port B TMDS Clock detection interrupt. When set the Port B TMDS Clock detection interrupt will trigger the INT2 interrupt and TMDS_CLK_B_ST will indicate the interrupt status. 0 - Disables Port B TMDS Clock Detection interrupt for INT2 1 - Enables Port B TMDS Clock Detection interrupt for INT2.
TMDSPLL_LCK_A_MB1		R/W
0x6E	00<u>0</u>00000	INT1 interrupt mask for Port A TMDS PLL Lock interrupt. When set the Port A TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDSPLL Lock interrupt for INT1 1 - Enables Port A TMDSPLL Lock interrupt for INT1.
TMDSPLL_LCK_B_MB1		R/W
0x6E	000<u>0</u>0000	INT1 interrupt mask for Port B TMDS PLL Lock interrupt. When set the Port B TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_B_ST will indicate the interrupt status. 0 - Disables Port B TMDSPLL Lock interrupt for INT1. 1 - Enables Port B TMDSPLL Lock interrupt for INT1.
TMDS_CLK_A_MB1		R/W
0x6E	0000000<u>0</u>	INT1 interrupt mask for Port A TMDS Clock detection interrupt. When set the Port A TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDS Clock Detection interrupt for INT1 1 - Enables Port A TMDS Clock Detection interrupt for INT1.
TMDS_CLK_B_MB1		R/W
0x6E	0000000<u>0</u>	INT1 interrupt mask for Port B TMDS Clock detection interrupt. When set the Port B TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_B_ST will indicate the interrupt status. 0 - Disables Port B TMDS Clock Detection interrupt for INT1 1 - Enables Port B TMDS Clock Detection interrupt for INT1.
HDMI_ENCRPT_A_RAW		R
0x6F	00<u>0</u>00000	Raw status of Port A Encryption detection signal. 0 - Current frame in Port A is not encrypted. 1 - Current frame in Port A is encrypted.
HDMI_ENCRPT_B_RAW		R
0x6F	000<u>0</u>0000	Raw status of Port B Encryption detection signal. 0 - Current frame in Port B is not encrypted. 1 - Current frame in Port B is encrypted.
CABLE_DET_A_RAW		R
0x6F	0000000<u>0</u>	Raw status of Port A +5 V cable detection signal. 0 - No cable detected on Port A 1 - Cable detected on Port A
CABLE_DET_B_RAW		R
0x6F	0000000<u>0</u>	Raw status of Port B +5 V cable detection signal. 0 - No cable detected on Port B 1 - Cable detected on Port B

Reg	Bits	Description	
HDMI_ENCRPT_A_ST			R
0x70	00<u>0</u>00000	Latched status for Port A Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - HDMI_ENCRPT_A_RAW has not changed. An interrupt has not been generated 1 - HDMI_ENCRPT_A_RAW has changed. An interrupt has been generated.	
HDMI_ENCRPT_B_ST			R
0x70	000<u>0</u>0000	Latched status for Port B Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - HDMI_ENCRPT_B_RAW has not changed. An interrupt has not been generated 1 - HDMI_ENCRPT_B_RAW has changed. An interrupt has been generated.	
CABLE_DET_A_ST			R
0x70	0000000<u>0</u>	Latched status for Port A +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - CABLE_DET_A_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_A_RAW has changed. Interrupt has been generated from this register.	
CABLE_DET_B_ST			R
0x70	00000000	Latched status for Port B +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - CABLE_DET_B_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_B_RAW has changed. Interrupt has been generated from this register.	
HDMI_ENCRPT_A_CLR			SC
0x71	00<u>0</u>00000	Clear bit for Port A Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_A_ST. 1 - Clears HDMI_ENCRPT_A_ST.	
HDMI_ENCRPT_B_CLR			SC
0x71	000<u>0</u>0000	Clear bit for Port B Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_B_ST. 1 - Clears HDMI_ENCRPT_B_ST.	
CABLE_DET_A_CLR			SC
0x71	0000000<u>0</u>	Clear bit for Port A +5V cable detection interrupt signal. 0 - Does not clear CABLE_DET_A_ST 1 - Clears CABLE_DET_A_ST	
CABLE_DET_B_CLR			SC
0x71	00000000	Clear bit for Port B +5V cable detection interrupt signal. 0 - Does not clear CABLE_DET_B_ST 1 - Clears CABLE_DET_B_ST	
HDMI_ENCRPT_A_MB2			R/W
0x72	00<u>0</u>00000	INT2 interrupt mask for Port A Encryption detection interrupt. When set the Port A Encryption detection interrupt will trigger the INT2 interrupt and HDMI_ENCRPT_A_ST will indicate the interrupt status. 0 - Disables Port A HDMI Encryption detection interrupt for INT2. 1 - Enables Port A HDMI Encryption detection interrupt for INT2.	
HDMI_ENCRPT_B_MB2			R/W
0x72	000<u>0</u>0000	INT2 interrupt mask for Port B Encryption detection interrupt. When set the Port B Encryption detection interrupt will trigger the INT2 interrupt and HDMI_ENCRPT_B_ST will indicate the interrupt status. 0 - Disables Port B HDMI Encryption detection interrupt for INT2. 1 - Enables Port B HDMI Encryption detection interrupt for INT2.	
CABLE_DET_A_MB2			R/W
0x72	0000000<u>0</u>	INT2 interrupt mask for Port A +5V cable detection interrupt. When set the Port A +5V cable detection interrupt will trigger the INT2 interrupt and CABLE_DET_A_ST will indicate the interrupt status. 0 - Disables Port A +5V Cable Detection interrupt for INT2. 1 - Enables Port A +5V Cable Detection interrupt for INT2.	
CABLE_DET_B_MB2			R/W
0x72	00000000	INT2 interrupt mask for Port B +5V cable detection interrupt. When set the Port B +5V cable detection interrupt will trigger the INT2 interrupt and CABLE_DET_B_ST will indicate the interrupt status. 0 - Disables Port B +5V Cable Detection interrupt for INT2. 1 - Enables Port B +5V Cable Detection interrupt for INT2.	

Reg	Bits	Description	
HDMI_ENCRPT_A_MB1			R/W
0x73	00<u>0</u>00000	INT1 interrupt mask for Port A Encryption detection interrupt. When set the Port A Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_A_ST will indicate the interrupt status. 0 - Disables Port A HDMI Encryption detection interrupt for INT1. 1 - Enables Port A HDMI Encryption detection interrupt for INT1.	
HDMI_ENCRPT_B_MB1			R/W
0x73	000<u>0</u>0000	INT1 interrupt mask for Port B Encryption detection interrupt. When set the Port B Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_B_ST will indicate the interrupt status. 0 - Disables Port B HDMI Encryption detection interrupt for INT1. 1 - Enables Port B HDMI Encryption detection interrupt for INT1.	
CABLE_DET_A_MB1			R/W
0x73	0000000<u>0</u>	INT1 interrupt mask for Port A +5V cable detection interrupt. When set the Port A +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_A_ST will indicate the interrupt status. 0 - Disables Port A +5V Cable Detection interrupt for INT1. 1 - Enables Port A +5V Cable Detection interrupt for INT1.	
CABLE_DET_B_MB1			R/W
0x73	0000000<u>0</u>	INT1 interrupt mask for Port B +5V cable detection interrupt. When set the Port B +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_B_ST will indicate the interrupt status. 0 - Disables Port B +5V Cable Detection interrupt for INT1. 1 - Enables Port B +5V Cable Detection interrupt for INT1.	
VIDEO_3D_RAW			R
0x74	00000<u>0</u>00	Raw status of the Video 3D signal. This flag is set when the following requirements are met; a VS Infoframe is received with byte PB1, PB2 and PB3 set to 0x000C03 and the HDMI_VIDEO_FORMAT field in the VS Infoframe is set to 010b. This flag is cleared when a VS Infoframe with the appropriate requirements for 3D or when a VS Infoframe has not been received within 3 VSyncs. 0 - Video 3D not detected 1 - Video 3D detected	
V_LOCKED_RAW			R
0x74	000000<u>0</u>0	Raw status of the Vertical Sync Filter Locked signal. 0 - Vertical sync filter has not locked and vertical sync parameters are not valid 1 - Vertical sync filter has locked and vertical sync parameters are valid	
DE_REGEN_LCK_RAW			R
0x74	0000000<u>0</u>	Raw status of the DE regeneration lock signal. 0 - DE regeneration block has not been locked 1 - DE regeneration block has been locked to the incoming DE signal	
VIDEO_3D_ST			R
0x75	00000<u>0</u>00	Latched status for the Video 3D interupt. Once set this bit will remain high until the interrupt has been cleared via VIDEO_3D_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - VIDEO_3D_RAW has not changed. An interrupt has not been generated. 1 - VIDEO_3D_RAW has changed. An interrupt has been generated.	
V_LOCKED_ST			R
0x75	000000<u>0</u>0	Latched status for the Vertical Sync Filter Locked interrupt. Once set this bit will remain high until the interrupt has been cleared via V_LOCKED_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - V_LOCKED_RAW has not changed. An interrupt has not been generated. 1 - V_LOCKED_RAW has changed. An interrupt has been generated.	
DE_REGEN_LCK_ST			R
0x75	0000000<u>0</u>	Latched status for DE Regeneration Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via DE_REGEN_LCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - DE_REGEN_LCK_RAW has not changed. An interrupt has not been generated. 1 - DE_REGEN_LCK_RAW has changed. An interrupt has been generated.	
VIDEO_3D_CLR			SC
0x76	00000<u>0</u>00	Clear bit for Video 3D Interrupt 0 - Does not clear VIDEO_3D_ST 1 - Clears VIDEO_3D_ST	
V_LOCKED_CLR			SC
0x76	000000<u>0</u>0	Clear bit for Vertical Sync Filter Locked Interrupt 0 - Does not clear V_LOCKED_ST 1 - Clears V_LOCKED_ST	

Reg	Bits	Description
DE_REGEN_LCK_CLR		SC
0x76	0000000<u>0</u>	Clear bit for DE Regeneration Lock interrupt signal. 0 - Does not clear DE_REGEN_LCK_ST 1 - Clears DE_REGEN_LCK_ST
VIDEO_3D_MB2		R/W
0x77	00000<u>0</u>00	INT2 interrupt mask for Video 3D interrupt. When set the Video 3D interrupt will trigger the INT2 interrupt and VIDEO_3D_ST will indicate the interrupt status. 0 - Disables Video 3D interrupt on INT2 1 - Enables Video 3D interrupt on INT2
V_LOCKED_MB2		R/W
0x77	000000<u>0</u>0	INT2 interrupt mask for Vertical Sync Filter Locked interrupt. When set the Vertical Sync Filter Locked interrupt will trigger the INT2 interrupt and V_LOCKED_ST will indicate the interrupt status. 0 - Disables Vertical Sync Filter Lock interrupt on INT2 1 - Enables Vertical Sync Filter Lock interrupt on INT2
DE_REGEN_LCK_MB2		R/W
0x77	0000000<u>0</u>	INT2 interrupt mask for DE Regeneration Lock interrupt. When set the DE Regeneration Lock interrupt will trigger the INT2 interrupt and DE_REGEN_LCK_ST will indicate the interrupt status. 0 - Disables DE Regeneration Lock interrupt on INT2 1 - Enables DE Regeneration Lock interrupt on INT2
VIDEO_3D_MB1		R/W
0x78	00000<u>0</u>00	INT1 interrupt mask for Video 3D interrupt. When set the Video 3D interrupt will trigger the INT1 interrupt and VIDEO_3D_ST will indicate the interrupt status. 0 - Disables Video 3D interrupt on INT1 1 - Enables Video 3D interrupt on INT1
V_LOCKED_MB1		R/W
0x78	000000<u>0</u>0	INT1 interrupt mask for Vertical Sync Filter Locked interrupt. When set the Vertical Sync Filter Locked interrupt will trigger the INT1 interrupt and V_LOCKED_ST will indicate the interrupt status. 0 - Disables Vertical Sync Filter Lock interrupt on INT1 1 - Enables Vertical Sync Filter Lock interrupt on INT1
DE_REGEN_LCK_MB1		R/W
0x78	0000000<u>0</u>	INT1 interrupt mask for DE Regeneration Lock interrupt. When set the DE Regeneration Lock interrupt will trigger the INT1 interrupt and DE_REGEN_LCK_ST will indicate the interrupt status. 0 - Disables DE Regeneration Lock interrupt on INT1 1 - Enables DE Regeneration Lock interrupt on INT1
NEW_ISRC2_PCKT_RAW		R
0x79	<u>0</u>0000000	Status of the New ISRC2 interrupt signal. When set to 1 it indicates a that an ISRC2 packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ISRC2_PCKT_CLR. 0 - No new ISRC2 packet received 1 - ISRC2 packet with new content received
NEW_ISRC1_PCKT_RAW		R
0x79	0<u>0</u>000000	Status of the New ISRC1 interrupt signal. When set to 1 it indicates a that an ISRC1 packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ISRC1_PCKT_CLR. 0 - No new ISRC1 packet received 1 - ISRC1 packet with new content received
NEW_ACP_PCKT_RAW		R
0x79	00<u>0</u>00000	Status of the New ACP Packet interrupt signal. When set to 1 it indicates a that an ACP packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ACP_PCKT_CLR. 0 - No new ACP packet received 1 - ACP packet with new content received
NEW_VS_INFO_RAW		R
0x79	000<u>0</u>0000	Status of the New Vendor Specific Infoframe interrupt signal. When set to 1 it indicates a that an Vendor Specific Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_VS_INFO_CLR. 0 - No new VS packet received 1 - VS packet with new content received
NEW_MS_INFO_RAW		R
0x79	0000<u>0</u>000	Status of the New MPEG Source Infoframe interrupt signal. When set to 1 it indicates a that an MPEG Source Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_MS_INFO_CLR. 0 - No new MPEG source InfoFrame received 1 - MPEG source InfoFrame with new content received

Reg	Bits	Description	
NEW_SPD_INFO_RAW			R
0x79	00000000	Status of the New Source Product Descriptor Packet interrupt signal. When set to 1 it indicates a that an Source Product Descriptor packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_SPD_INFO_CLR. 0 - No new SPD InfoFrame received 1 - SPD InfoFrame with new content received	
NEW_AUDIO_INFO_RAW			R
0x79	00000000	Status of the New Audio Infoframe interrupt signal. When set to 1 it indicates a that an Audio Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_AUDIO_INFO_CLR. 0 - No new audio InfoFrame received 1 - Audio InfoFrame with new content received	
NEW_AVI_INFO_RAW			R
0x79	00000000	Status of the New AVI Infoframe interrupt signal. When set to 1 it indicates that an AVI Infoframe has been received with new contents. Once set this bit will remain high until the interrupt has been cleared via NEW_AVI_INFO_CLR. 0 - No new AVI InfoFrame received 1 - AVI InfoFrame with new content received	
NEW_ISRC2_PCKT_ST			R
0x7A	00000000	Latched status for the New ISRC2 Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ISRC2_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new ISRC2 packet received. An interrupt has not been generated. 1 - ISRC2 packet with new content received. An interrupt has been generated.	
NEW_ISRC1_PCKT_ST			R
0x7A	00000000	Latched status for the New ISRC1 Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ISRC1_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new ISRC1 packet received. An interrupt has not been generated. 1 - ISRC1 packet with new content received. An interrupt has been generated.	
NEW_ACP_PCKT_ST			R
0x7A	00000000	Latched status for the New ACP Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ACP_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new ACP packet received. An interrupt has not been generated. 1 - ACP packet with new content received. An interrupt has been generated.	
NEW_VS_INFO_ST			R
0x7A	00000000	Latched status for the New Vendor Specific Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_VS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new VS packet received. An interrupt has not been generated. 1 - VS packet with new content received. An interrupt has been generated.	
NEW_MS_INFO_ST			R
0x7A	00000000	Latched status for the New MPEG Source Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_MS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new MPEG Source InfoFrame received. Interrupt has not been generated. 1 - MPEG Source InfoFrame with new content received. Interrupt has been generated.	
NEW_SPD_INFO_ST			R
0x7A	00000000	Latched status for the New Source Product Descriptor Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_SPD_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new SPD InfoFrame received. Interrupt has not been generated. 1 - SPD InfoFrame with new content received. Interrupt has been generated.	
NEW_AUDIO_INFO_ST			R
0x7A	00000000	Latched status for the New Audio Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_AUDIO_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new Audio InfoFrame received. Interrupt has not been generated. 1 - Audio InfoFrame with new content received. Interrupt has been generated.	
NEW_AVI_INFO_ST			R
0x7A	00000000	Latched status for the NEW_AVI_INFO_RAW. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set this bit will remain high until the interrupt has been cleared via NEW_AVI_INFO_CLR. 0 - NEW_AVI_INFO_RAW has not changed state 1 - NEW_AVI_INFO_RAW has changed state	

Reg	Bits	Description	
NEW_ISRC2_PCKT_CLR			SC
0x7B	00000000	Clear bit for NEW_ISRC2_PCKT_RAW and NEW_ISRC2_PCKT_ST bits. 0 - No function 1 - Clear NEW_ISRC2_PCKT_RAW and NEW_ISRC2_PCKT_ST	
NEW_ISRC1_PCKT_CLR			SC
0x7B	00000000	Clear bit for NEW_ISRC1_PCKT_RAW and NEW_ISCR1_PCKT_ST bits. 0 - No function 1 - Clear NEW_ISRC1_PCKT_RAW and NEW_ISRC1_PCKT_ST	
NEW_ACP_PCKT_CLR			SC
0x7B	00000000	Clear bit for NEW_ACP_PCKT_RAW and NEW_ACP_PCKT_ST bits. 0 - No function 1 - Clear NEW_ACP_PCKT_RAW and NEW_ACP_PCKT_ST	
NEW_VS_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_VS_INFO_RAW and NEW_VS_INFO_ST bits. 0 - No function 1 - Clear NEW_VS_INFO_RAW and NEW_VS_INFO_ST	
NEW_MS_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_MS_INFO_RAW and NEW_MS_INFO_ST bits. 0 - No function 1 - Clear NEW_MS_INFO_RAW and NEW_MS_INFO_ST	
NEW_SPD_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_SPD_INFO_RAW and NEW_SPD_INFO_ST bits. 0 - No function 1 - Clear NEW_SPD_INFO_RAW and NEW_SPD_INFO_ST	
NEW_AUDIO_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_AUDIO_INFO_RAW and NEW_AUDIO_INFO_ST bits. 0 - No function 1 - Clear NEW_AUDIO_INFO_RAW and NEW_AUDIO_INFO_ST	
NEW_AVI_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST bits. 0 - No function 1 - Clear NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST	
NEW_ISRC2_PCKT_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New ISRC2 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT2 interrupt and NEW_ISRC2_ST will indicate the interrupt status. 0 - Disables New ISRC2 Packet interrupt for INT2 1 - Enables New ISRC2 Packet interrupt for INT2	
NEW_ISRC1_PCKT_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New ISRC1 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT2 interrupt and NEW_ISRC1_ST will indicate the interrupt status. 0 - Disables New ISRC1 Packet interrupt for INT2 1 - Enables New ISRC1 Packet interrupt for INT2	
NEW_ACP_PCKT_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New ACP Packet interrupt. When set the New ACP interrupt will trigger the INT2 interrupt and NEW_ACP_ST will indicate the interrupt status. 0 - Disables New ACP Packet interrupt for INT2 1 - Enables New ACP Packet interrupt for INT2	
NEW_VS_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New Vendor Specific Infoframe interrupt. When set the New Vendor Specific Infoframe interrupt will trigger the INT2 interrupt and NEW_VS_INFO_ST will indicate the interrupt status. 0 - Disables New VS Infoframe interrupt for INT2 1 - Enables New VS Infoframe interrupt for INT2	
NEW_MS_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New MPEG Source Infoframe interrupt. When set the New MPEG Source Infoframe interrupt will trigger the INT2 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New MS Infoframe interrupt for INT2 1 - Enables New MS Infoframe interrupt for INT2	

Reg	Bits	Description
NEW_SPD_INFO_MB2		R/W
0x7C	00000**0**00	INT2 interrupt mask for New Source Product Descriptor Infoframe interrupt. When set the New Source Product Descriptor Infoframe interrupt will trigger the INT2 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New SPD Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
NEW_AUDIO_INFO_MB2		R/W
0x7C	000000**0**0	INT2 interrupt mask for New Audio Infoframe interrupt. When set the New Audio Infoframe interrupt will trigger the INT2 interrupt and NEW_AUDIO_INFO_ST will indicate the interrupt status. 0 - Disables New Audio Infoframe interrupt for INT2 1 - Enables New Audio Infoframe interrupt for INT2
NEW_AVI_INFO_MB2		R/W
0x7C	0000000**0**	INT2 interrupt mask for New AVI Infoframe detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT2. 0 - Disables New SPD Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
NEW_ISRC2_PCKT_MB1		R/W
0x7D	**0**0000000	INT1 interrupt mask for New ISRC2 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT1 interrupt and NEW_ISRC2_ST will indicate the interrupt status. 0 - Disables New ISRC2 Packet interrupt for INT1 1 - Enables New ISRC2 Packet interrupt for INT1
NEW_ISRC1_PCKT_MB1		R/W
0x7D	0**0**000000	INT1 interrupt mask for New ISRC1 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT1 interrupt and NEW_ISRC1_ST will indicate the interrupt status. 0 - Disables New ISRC1 Packet interrupt for INT1 1 - Enables New ISRC1 Packet interrupt for INT1
NEW_ACP_PCKT_MB1		R/W
0x7D	00**0**00000	INT1 interrupt mask for New ACP Packet interrupt. When set the New ACP interrupt will trigger the INT1 interrupt and NEW_ACP_ST will indicate the interrupt status. 0 - Disables New ACP Packet interrupt for INT1 1 - Enables New ACP Packet interrupt for INT1
NEW_VS_INFO_MB1		R/W
0x7D	000**0**0000	INT1 interrupt mask for New Vendor Specific Infoframe interrupt. When set the New Vendor Specific Infoframe interrupt will trigger the INT1 interrupt and NEW_VS_INFO_ST will indicate the interrupt status. 0 - Disables New VS Infoframe interrupt for INT1 1 - Enables New VS Infoframe interrupt for INT1
NEW_MS_INFO_MB1		R/W
0x7D	0000**0**000	INT1 interrupt mask for New MPEG Source Infoframe interrupt. When set the New MPEG Source Infoframe interrupt will trigger the INT1 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New MS Infoframe interrupt for INT1 1 - Enables New MS Infoframe interrupt for INT1
NEW_SPD_INFO_MB1		R/W
0x7D	00000**0**00	INT1 interrupt mask for New Source Product Descriptor Infoframe interrupt. When set the New Source Product Descriptor Infoframe interrupt will trigger the INT1 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New SPD Infoframe interrupt for INT1 1 - Enables New SPD Infoframe interrupt for INT1
NEW_AUDIO_INFO_MB1		R/W
0x7D	000000**0**0	INT1 interrupt mask for New Audio Infoframe interrupt. When set the New Audio Infoframe interrupt will trigger the INT1 interrupt and NEW_AUDIO_INFO_ST will indicate the interrupt status. 0 - Disables New Audio Infoframe interrupt for INT1 1 - Enables New Audio Infoframe interrupt for INT1
NEW_AVI_INFO_MB1		R/W
0x7D	0000000**0**	INT1 interrupt mask for New AVI Infoframe detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT1. 0 - Disable new AVI Infoframe interrupt for INT1 1 - Enable new AVI Infoframe interrupt for INT1
FIFO_NEAR_OVFL_RAW		R
0x7E	**0**0000000	Status of Audio FIFO Near Overflow interrupt signal. When set to 1 it indicates the Audio FIFO is near overflow as the number FIFO registers containing stereo data is greater or equal to value set in AUDIO_FIFO_ALMOST_FULL_THRESHOLD. Once set, this bit will remain high until it is cleared via FIFO_NEAR_OVFL_CLR. 0 - Audio FIFO has not reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0] 1 - Audio FIFO has reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0]

Reg	Bits	Description	
FIFO_UNDERFLO_RAW			R
0x7E	0[0]000000	Status of Audio FIFO Underflow interrupt signal. When set to 1 it indicates the Audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit will remain high until it is cleared via AUDIO_FIFO_UNDERFLO_CLR. 0 - Audio FIFO has not underflowed 1 - Audio FIFO has underflowed	
FIFO_OVERFLO_RAW			R
0x7E	00[0]00000	Status of Audio FIFO Overflow interrupt signal. When set to 1 it indicates Audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit will remain high until it is cleared via AUDIO_FIFO_OVERFLO_CLR. 0 - Audio FIFO has not overflowed 1 - Audio FIFO has overflowed	
CTS_PASS_THRSH_RAW			R
0x7E	000[0]0000	Status of the ACR CTS value exceed threshold interrupt signal. When set to 1 it indicates the CTS Value of the ACR packets has exceeded the threshold set by CTS_CHANGE_THRESHOLD. Once set, this bit will remain high until it is cleared via CTS_PASS_THRSH_CLR. 0 - Audio clock regeneration CTS value has not passed the threshold 1 - Audio clock regeneration CTS value has changed more than threshold	
CHANGE_N_RAW			R
0x7E	0000[0]000	Status of the ACR N Value changed interrupt signal. When set to 1 it indicates the N Value of the ACR packets has changed. Once set, this bit will remain high until it is cleared via CHANGE_N_CLR. 0 - Audio clock regeneration N value has not changed 1 - Audio clock regeneration N value has changed	
PACKET_ERROR_RAW			R
0x7E	00000[0]00	Status of the Packet Error interrupt signal. When set to 1 it indicates a that an any packet has been received with an uncorrectable EEC error in either the header or body. Once set, this bit will remain high until it is cleared via PACKET_ERROR_CLR. 0 - No uncorrectable error detected in packet header 1 - Uncorrectable error detected in an unknown packet (error in packet header)	
AUDIO_PCKT_ERR_RAW			R
0x7E	000000[0]0	Status of the Audio Packet Error interrupt signal. When set to 1 it indicates a that an Audio packet has been received with an uncorrectable error. Once set, this bit will remain high until it is cleared via AUDIO_PCKT_ERR_CLR. 0 - No uncorrectable error detected in audio packets 1 - Uncorrectable error detected in an audio packet	
NEW_GAMUT_MDATA_RAW			R
0x7E	0000000[0]	Status of the New Gamut Metadata Packet interrupt signal. When set to 1 it indicates a that a Gamut Metadata packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_GAMUT_MDATA_PCKT_CLR. 0 - No new Gamut metadata packet received or no change has taken place 1 - New Gamut metadata packet received that triggered this interrupt	
FIFO_NEAR_OVFL_ST			R
0x7F	[0]0000000	Latched status for the Audio FIFO Near Overflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_OVFL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not reached high threshold 1 - Audio FIFO has reached high threshold	
FIFO_UNDERFLO_ST			R
0x7F	0[0]000000	Latched status for the Audio FIFO Underflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_UNDERFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not underflowed 1 - Audio FIFO has underflowed	
FIFO_OVERFLO_ST			R
0x7F	00[0]00000	Latched status for the Audio FIFO Overflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_OVERFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not overflowed 1 - Audio FIFO has overflowed	
CTS_PASS_THRSH_ST			R
0x7F	000[0]0000	Latched status for the ACR CTS Value Exceed Threshold interrupt. Once set this bit will remain high until the interrupt has been cleared via CTS_PASS_THRSH_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio clock regeneration CTS value has not passed the threshold 1 - Audio clock regeneration CTS value has changed more than threshold	

Reg	Bits	Description	
CHANGE_N_ST			R
0x7F	0000**0**000	Latched status for the ACR N Value Changed interrupt. Once set this bit will remain high until the interrupt has been cleared via CHANGE_N_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio clock regeneration N value has not changed 1 - Audio clock regeneration N value has changed	
PACKET_ERROR_ST			R
0x7F	00000**0**00	Latched status for the Packet Error interrupt. Once set this bit will remain high until the interrupt has been cleared via PACKET_ERROR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No uncorrectable error detected in packet header. An interrupt has not been generated. 1 - Uncorrectable error detected in an unknown packet (in packet header). An interrupt has been generated.	
AUDIO_PCKT_ERR_ST			R
0x7F	000000**0**0	Latched status for the Audio Packet Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_PCKT_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No uncorrectable error detected in audio packets. An interrupt has not been generated. 1 - Uncorrectable error detected in an audio packet. An interrupt has been generated.	
NEW_GAMUT_MDATA_ST			R
0x7F	0000000**0**	Latched status for the New Gamut Metadata Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No new Gamut metadata packet received or no change has taken place. An interrupt has not been generated. 1 - New Gamut metadata packet received. An interrupt has been generated.	
FIFO_NEAR_OVFL_CLR			SC
0x80	**0**0000000	Clear bit for the Audio FIFO Near Overflow interrupt. 0 - Does not clear 1 - Clears FIFO_NEAR_OVERL_ST	
FIFO_UNDERFLO_CLR			SC
0x80	0**0**000000	Clear bit for the Audio FIFO Underflow interrupt. 0 - Does not clear FIFO_UNDERFLO_ST 1 - Clears FIFO_UNDERFLO_ST	
FIFO_OVERFLO_CLR			SC
0x80	00**0**00000	Clear bit for the Audio FIFO Overflow interrupt. 0 - Does not clear FIFO_OVERFLO_ST 1 - Clears FIFO_OVERFLO_ST	
CTS_PASS_THRSH_CLR			SC
0x80	000**0**0000	Clear bit for ACR CTS Value Exceed Threshold interrupt. 0 - Does not clear 1 - Clears CTS_PASS_THRSH_ST	
CHANGE_N_CLR			SC
0x80	0000**0**000	Clear bit for ACR N Value Changed interrupt. 0 - Does not clear CHANGE_N_ST 1 - Clears CHANGE_N_ST	
PACKET_ERROR_CLR			SC
0x80	00000**0**00	Clear bit for Packet Error interrupt. 0 - Does not clear PACKET_ERROR_ST 1 - Clears PACKET_ERROR_ST	
AUDIO_PCKT_ERR_CLR			SC
0x80	000000**0**0	Clear bit for Audio Packet Error interrupt. 0 - Does not clear AUDIO_PCKT_ERR_ST 1 - Clears AUDIO_PCKT_ERR_ST	
NEW_GAMUT_MDATA_CLR			SC
0x80	0000000**0**	Clear bit for New Gamut Metadata Packet interrupt. 0 - Does not clear NEW_GAMUT_MDATA_ST 1 - Clears NEW_GAMUT_MDATA_ST	
FIFO_NEAR_OVFL_MB2			R/W
0x81	**0**0000000	INT2 interrupt mask for Audio FIFO Near Overflow interrupt. When set the Audio FIFO Near Overflow interrupt will trigger the INT2 interrupt and FIFO_NEAR_OVFL_ST will indicate the interrupt status. 0 - Disable Audio FIFO Near Overflow interrupt on INT2 1 - Enable Audio FIFO Near Overflow interrupt on INT2	

Reg	Bits	Description
FIFO_UNDERFLO_MB2		R/W
0x81	0<u>0</u>000000	INT2 interrupt mask for Audio FIFO Underflow interrupt. When set the Audio FIFO Underflow interrupt will trigger the INT2 interrupt and FIFO_UNDERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Underflow interrupt on INT2 1 - Enable Audio FIFO Underflow interrupt on INT2
FIFO_OVERFLO_MB2		R/W
0x81	00<u>0</u>00000	INT2 interrupt mask for Audio FIFO Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT2 interrupt and FIFO_OVERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT2 1 - Enable Audio FIFO Overflow interrupt on INT2
CTS_PASS_THRSH_MB2		R/W
0x81	000<u>0</u>0000	INT2 interrupt mask for ACR CTS Value Exceed Threshold interrupt. When set the ACR CTS Value Exceed Threshold interrupt will trigger the INT2 interrupt and CTS_PASS_THRSH_ST will indicate the interrupt status. 0 - Disable ACR CTS Value Exceeded Threshold interrupt on INT2 1 - Enable ACR CTS Value Exceeded Threshold interrupt on INT2
CHANGE_N_MB2		R/W
0x81	0000<u>0</u>000	INT2 interrupt mask for ACR N Value changed interrupt. When set the ACR N Value changed interrupt will trigger the INT2 interrupt and CHANGE_N_ST will indicate the interrupt status. 0 - Disables ACR N Value Changed interrupt for INT2 1 - Enables ACR N Value Changed interrupt for INT2
PACKET_ERROR_MB2		R/W
0x81	00000<u>0</u>00	INT2 interrupt mask for Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT2 interrupt and PACKET_ERROR_ST will indicate the interrupt status. 0 - Disables Packet Error interrupt for INT2 1 - Enables Packet Error interrupt for INT2
AUDIO_PCKT_ERR_MB2		R/W
0x81	000000<u>0</u>0	INT2 interrupt mask for Audio Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT2 interrupt and AUDIO_PCKT_ERR_ST will indicate the interrupt status. 0 - Disables Audio Packet Error interrupt for INT2 1 - Enables Audio Packet Error interrupt for INT2
NEW_GAMUT_MDATA_MB2		R/W
0x81	0000000<u>0</u>	INT2 interrupt mask for New Gamut Metadata packet interrupt. When set the New Gamut Metadata packet interrupt will trigger the INT2 interrupt and NEW_GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables New Gamut metadata Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
FIFO_NEAR_OVFL_MB1		R/W
0x82	<u>0</u>0000000	INT1 interrupt mask for Audio FIFO Near Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT1 interrupt and FIFO_NEAR_OVFL_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
FIFO_UNDERFLO_MB1		R/W
0x82	0<u>0</u>000000	INT1 interrupt mask for Audio FIFO Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT1 interrupt and FIFO_OVERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
FIFO_OVERFLO_MB1		R/W
0x82	00<u>0</u>00000	INT1 interrupt mask for Audio FIFO Overflow interrupt. When set the Audio FIFO Overflow interrupt will trigger the INT1 interrupt and FIFO_OVERFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
CTS_PASS_THRSH_MB1		R/W
0x82	000<u>0</u>0000	INT1 interrupt mask for ACR CTS Value Exceed Threshold interrupt. When set the ACR CTS Value Exceed Threshold interrupt will trigger the INT1 interrupt and CTS_PASS_THRSH_ST will indicate the interrupt status. 0 - Disable ACR CTS Value Exceeded Threshold interrupt on INT1 1 - Enable ACR CTS Value Exceeded Threshold interrupt on INT1
CHANGE_N_MB1		R/W
0x82	0000<u>0</u>000	INT1 interrupt mask for ACR N Value changed interrupt. When set the ACR N Value changed interrupt will trigger the INT1 interrupt and CHANGE_N_ST will indicate the interrupt status. 0 - Disables ACR N Value Changed interrupt for INT1 1 - Enables ACR N Value Changed interrupt for INT1

Reg	Bits	Description
PACKET_ERROR_MB1		R/W
0x82	00000**0**00	INT1 interrupt mask for Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT1 interrupt and PACKET_ERROR_ST will indicate the interrupt status. 0 - Disables Packet Error interrupt for INT1 1 - Enables Packet Error interrupt for INT1
AUDIO_PCKT_ERR_MB1		R/W
0x82	0000000**0**	INT1 interrupt mask for Audio Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT1 interrupt and AUDIO_PCKT_ERR_ST will indicate the interrupt status. 0 - Disables Audio Packet Error interrupt for INT1 1 - Enables Audio Packet Error interrupt for INT1
NEW_GAMUT_MDATA_MB1		R/W
0x82	0000000**0**	INT1 interrupt mask for New Gamut Metadata packet interrupt. When set the New Gamut Metadata packet interrupt will trigger the INT1 interrupt and NEW_GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables New Gamut METADATA Infoframe interrupt for INT1 1 - Enables New SPD Infoframe interrupt for INT1
DEEP_COLOR_CHNG_RAW		R
0x83	**0**0000000	Status of Deep Color Mode Changed Interrupt signal. When set to 1 it indicates a change in the deep color mode has been detected. Once set, this bit will remain high until it is cleared via DEEP_COLOR_CHNG_CLR. 0 - Deep color mode has not changed 1 - Change in deep color triggered this interrupt
VCLK_CHNG_RAW		R
0x83	0**0**000000	Status of Video Clock Changed Interrupt signal. When set to 1 it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit will remain high until it is cleared via VCLK_CHNG_CLR. 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock triggered this interrupt
AUDIO_MODE_CHNG_RAW		R
0x83	00**0**00000	Status of Audio Mode Change Interrupt signal. When set to 1 it indicates that the type of audio packet received has changed. The following are considered Audio modes, No Audio Packets, Audio Sample Packet, DSD packet or HBR Packet. Once set, this bit will remain high until it is cleared via AUDIO_MODE_CHNG_CLR. 0 - Audio mode has not changed. 1 - Audio mode has changed.
PARITY_ERROR_RAW		R
0x83	000**0**0000	Status of Parity Error Interrupt signal. When set to 1 it indicates an audio sample packet has been received with parity error. Once set, this bit will remain high until it is cleared via PARITY_ERROR_CLR. 0 - No parity error detected in audio packets 1 - Parity error has been detected in an audio packet
NEW_SAMP_RT_RAW		R
0x83	0000**0**000	Status of new sampling rate interrupt signal. When set to 1 it indicates that audio sampling frequency field in channel status data has changed. Once set, this bit will remain high until it is cleared via NEW_SAMP_RT _CLR. 0 - Sampling rate bits of the channel status data on audio channel 0 have not changed 1 - Sampling rate bits of the channel status data on audio channel 0 have changed
AUDIO_FLT_LINE_RAW		R
0x83	00000**0**00	Status of Audio Flat Line interrupt signal. When set to 1 it indicates audio sample packet has been received with the Flat line bit set to 1. Once set, this bit will remain high until it is cleared via AUDIO_FLT_LINE_CLR. 0 - Audio sample packet with flat line bit set has not been received 1 - Audio sample packet with flat line bit set has been received
NEW_TMDS_FRQ_RAW		R
0x83	0000000**0**	Status of New TMDS Frequency interrupt signal. When set to 1 it indicates the TMDS Frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0]. Once set, this bit will remain high until it is cleared via NEW_TMDS_FREQ_CLR. 0 - TMDS frequency has not changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map 1 - TMDS frequency has changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map
FIFO_NEAR_UFLO_RAW		R
0x83	0000000**0**	Status of Audio FIFO Near Underflow interrupt signal. When set to 1 it indicates the Audio FIFO is near underflow as the number of FIFO registers containing stereo data is less or equal to value set in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD. Once set, this bit will remain high until it is cleared via FIFO_NEAR_UFLO_CLR. 0 - Audio FIFO has not reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0] 1 - Audio FIFO has reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0]

Reg	Bits	Description	
DEEP_COLOR_CHNG_ST			R
0x84	0000000	Latched status of Deep Color Mode Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via DEEP_COLOR_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Deep color mode has not changed 1 - Change in deep color has been detected	
VCLK_CHNG_ST			R
0x84	000000	Latched status of Video Clock Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via VCLK_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock	
AUDIO_MODE_CHNG_ST			R
0x84	00000	Latched status of Audio Mode Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_MODE_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio mode has not changed 1 - Audio mode has changed. The following are considered Audio modes, No Audio, PCM, DSD or HBR	
PARITY_ERROR_ST			R
0x84	0000	Latched status of Parity Error Interrupt. Once set this bit will remain high until the interrupt has been cleared via PARITY_ERROR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No parity error detected in audio packets 1 - Parity error detected in an audio packet	
NEW_SAMP_RT_ST			R
0x84	0000	Latched status of New Sampling Rate Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_SAMP_RT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Sampling rate bits of the channel status data on audio channel 0 have not changed 1 - Sampling rate bits of the channel status data on audio channel 0 have changed.	
AUDIO_FLT_LINE_ST			R
0x84	000000	Latched status of New TMDS Frequency Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio sample packet with flat line bit set has not been received 1 - Audio sample packet with flat line bit set has been received	
NEW_TMDS_FRQ_ST			R
0x84	0000000	Latched status of New TMDS Frequency Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - TMDS frequency has not changed by more than tolerance 1 - TMDS frequency has changed by more than tolerance	
FIFO_NEAR_UFLO_ST			R
0x84	00000000	Latched status for the Audio FIFO Near Underflow interrupt. Once set this bit will remain high until the interrupt has been cleared via FIFO_UFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Audio FIFO has not reached low threshold 1 - Audio FIFO has reached low threshold	
DEEP_COLOR_CHNG_CLR			SC
0x85	0000000	Clear bit for the Deep Color Mode Change Interrupt. 0 - Does not clear DEEP_COLOR_CHNG_ST 1 - Clears DEEP_COLOR_CHNG_ST	
VCLK_CHNG_CLR			SC
0x85	000000	Clear bit for the Video Clock Change Interrupt. 0 - Does not clear VCLK_CHNG_ST 1 - Clears VCLK_CHNG_ST	
AUDIO_MODE_CHNG_CLR			SC
0x85	00000	Clear bit for the Audio Mode Change Interrupt. 0 - Does not clear AUDIO_MODE_CHNG_ST 1 - Clears AUDIO_MODE_CHNG_ST	
PARITY_ERROR_CLR			SC
0x85	0000	Clear bit for the Parity Error Interrupt. 0 - Does not clear 1 - Clears PARRITY_ERROR_ST	

Reg	Bits	Description	
NEW_SAMP_RT_CLR			SC
0x85	0000**0**000	Clear bit for the New Sample Rate Interrupt. 0 - Does not clear NEW_SAMP_RT_ST 1 - Clears NEW_SAMP_RT_ST	
AUDIO_FLT_LINE_CLR			SC
0x85	00000**0**00	Clear bit for the Audio Flat line Interrupt. 0 - Does not clear 1 - Clears AUDIO_FLT_LINE_ST	
NEW_TMDS_FRQ_CLR			SC
0x85	000000**0**0	Clear bit for the New TMDS Frequency Interrupt. 0 - Does not clear NEW_TMDS_FRQ_ST 1 - Clears NEW_TMDS_FRQ_ST	
FIFO_NEAR_UFLO_CLR			SC
0x85	0000000**0**	Clear bit for the Audio FIFO Near Underflow interrupt. 0 - Does not clear 1 - Clears FIFO_NEAR_UFLO_ST	
DEEP_COLOR_CHNG_MB2			R/W
0x86	**0**0000000	INT2 interrupt mask for Deep Color Mode Changed interrupt. When set the Deep Color Mode Changed interrupt will trigger the INT2 interrupt and DEEP_COLOR_CHNG_ST will indicate the interrupt status. 0 - Disable Deep Color Mode Changed interrupt on INT2 1 - Enable Deep Color Mode Changed interrupt on INT2	
VCLK_CHNG_MB2			R/W
0x86	0**0**000000	INT2 interrupt mask for Video Clock Changed interrupt. When set the Video Clock Changed interrupt will trigger the INT2 interrupt and VCLK_CHNG_ST will indicate the interrupt status. 0 - Disable Video Clock Changed interrupt on INT2 1 - Enable Video Clock Changed interrupt on INT2	
AUDIO_MODE_CHNG_MB2			R/W
0x86	00**0**00000	INT2 interrupt mask for Audio Mode Change interrupt. When set the Audio Mode Change interrupt will trigger the INT2 interrupt and AUDIO_MODE_CHNG_ST will indicate the interrupt status. 0 - Disable Audio Mode Changed interrupt on INT2 1 - Enable Audio Mode Changed interrupt on INT2	
PARITY_ERROR_MB2			R/W
0x86	000**0**0000	INT2 interrupt mask for Parity Error interrupt. When set the Parity Error interrupt will trigger the INT2 interrupt and PARITY_ERROR_ST will indicate the interrupt status. 0 - Disable Parity Error interrupt on INT2 1 - Enable Parity Error interrupt on INT2	
NEW_SAMP_RT_MB2			R/W
0x86	0000**0**000	INT2 interrupt mask for New Sample Rate interrupt. When set the New Sample interrupt will trigger the INT2 interrupt and NEW_SAMP_RT_ST will indicate the interrupt status. 0 - Disable New Sample Rate interrupt on INT2 1 - Enable New Sample Rate interrupt on INT2	
AUDIO_FLT_LINE_MB2			R/W
0x86	00000**0**00	INT2 interrupt mask for Audio Flat line interrupt. When set the Audio Flat line interrupt will trigger the INT2 interrupt and AUDIO_FLT_LINE_ST will indicate the interrupt status. 0 - Disable Audio Flat Line interrupt on INT2 1 - Enable Audio Flat Line interrupt on INT2	
NEW_TMDS_FRQ_MB2			R/W
0x86	000000**0**0	INT2 interrupt mask for New TMDS Frequency interrupt. When set the New TMDS Frequency interrupt will trigger the INT2 interrupt and NEW_TMDS_ST will indicate the interrupt status. 0 - Disable New TMDS Frequency interrupt on INT2 1 - Enable New TMDS Frequency interrupt on INT2	
FIFO_NEAR_UFLO_MB2			R/W
0x86	0000000**0**	INT2 interrupt mask for Audio FIFO Near Underflow interrupt. When set the Audio FIFO Near Underflow interrupt will trigger the INT2 interrupt and FIFO_NEAR_UFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Near Underflow interrupt on INT2 1 - Enable Audio FIFO Near Underflow interrupt on INT2	

Reg	Bits	Description
DEEP_COLOR_CHNG_MB1		R/W
0x87	0000000	INT1 interrupt mask for Deep Color Mode Changed interrupt. When set the Deep Color Mode Changed interrupt will trigger the INT1 interrupt and DEEP_COLOR_CHNG_ST will indicate the interrupt status. 0 - Disable Deep Color Mode Change interrupt on INT1 1 - Enable Deep Color Mode interrupt on INT1
VCLK_CHNG_MB1		R/W
0x87	000000	INT1 interrupt mask for Video Clock Changed interrupt. When set the Video Clock Changed interrupt will trigger the INT1 interrupt and VCLK_CHNG_ST will indicate the interrupt status. 0 - Disable Video Clock Change interrupt on INT1 1 - Enable Video Clock Change interrupt on INT1
AUDIO_MODE_CHNG_MB1		R/W
0x87	00000	INT1 interrupt mask for Audio Mode Changed interrupt. When set the Audio Mode Changed interrupt will trigger the INT1 interrupt and AUDIO_MODE_CHNG_ST will indicate the interrupt status. 0 - Disable Audio Mode Change interrupt on INT1 1 - Enable Audio Mode Change interrupt on INT1
PARITY_ERROR_MB1		R/W
0x87	0000	INT1 interrupt mask for Parity Error interrupt. When set the Parity Error interrupt will trigger the INT1 interrupt and PARITY_ERROR_ST will indicate the interrupt status. 0 - Disable Parity Error interrupt on INT1 1 - Enable Parity Error interrupt on INT1
NEW_SAMP_RT_MB1		R/W
0x87	000	INT1 interrupt mask for New Sample Rate interrupt. When set the New Sample Rate interrupt will trigger the INT1 interrupt and NEW_SAMP_RT_ST will indicate the interrupt status. 0 - Disable New Sample Rate interrupt on INT1 1 - Enable New Sample Rate interrupt on INT1
AUDIO_FLT_LINE_MB1		R/W
0x87	00	INT1 interrupt mask for Audio Flat Line interrupt. When set the Audio Flat Line interrupt will trigger the INT1 interrupt and AUDIO_FLT_LINE_ST will indicate the interrupt status. 0 - Disable Audio Flat Line interrupt on INT1 1 - Enable Audio Flat Line interrupt on INT1
NEW_TMDS_FRQ_MB1		R/W
0x87	0	INT1 interrupt mask for New TMDS Frequency interrupt. When set the New TMDS Frequency interrupt will trigger the INT1 interrupt and NEW_TMDS_FREQ_ST will indicate the interrupt status. 0 - Disable New TMDS Frequency interrupt on INT1 1 - Enable New TMDS Frequency interrupt on INT1
FIFO_NEAR_UFLO_MB1		R/W
0x87	0	INT1 interrupt mask for Audio FIFO Near Underflow interrupt. When set the Audio FIFO Near Underflow interrupt will trigger the INT1 interrupt and FIFO_UFLO_ST will indicate the interrupt status. 0 - Disable Audio FIFO Overflow interrupt on INT1 1 - Enable Audio FIFO Overflow interrupt on INT1
MS_INF_CKS_ERR_RAW		R
0x88	0000000	Status of MPEG Source Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an MPEG Source Infoframe. Once set, this bit will remain high until it is cleared via MS_INF_CKS_ERR_CLR. 0 - No MPEG source infoframe checksum error has occurred 1 - An MPEG source infoframe checksum error has occurred
SPD_INF_CKS_ERR_RAW		R
0x88	000000	Status of SPD Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an SPD Infoframe. Once set, this bit will remain high until it is cleared via ASPD_INF_CKS_ERR_CLR. 0 - No SPD infoframe checksum error has occurred 1 - An SPD infoframe checksum error has occurred
AUD_INF_CKS_ERR_RAW		R
0x88	00000	Status of Audio Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an Audio Infoframe. Once set, this bit will remain high until it is cleared via AUDIO_INF_CKS_ERR_CLR. 0 - No Audio infoframe checksum error has occurred 1 - An Audio infoframe checksum error has occurred
AVI_INF_CKS_ERR_RAW		R
0x88	0000	Status of AVI Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an AVI InfoFrame. Once set, this bit will remain high until it is cleared via AVI_INF_CKS_ERR_CLR. 0 - No AVI infoframe checksum error has occurred 1 - An AVI infoframe checksum error has occurred

Reg	Bits	Description	
AKSV_UPDATE_A_RAW			R
0x88	0000000<u>0</u>	Status of Port A AKSV Update Interrupt signal. When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port A. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_A_CLR. 0 - No AKSV updates on Port A. 1 - Detected a write access to the AKSV register on Port A.	
AKSV_UPDATE_B_RAW			R
0x88	0000000<u>0</u>	Status of Port B AKSV Update Interrupt signal. When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port B. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_B_CLR. 0 - No AKSV updates on Port B. 1 - Detected a write access to the AKSV register on Port A.	
MS_INF_CKS_ERR_ST			R
0x89	<u>0</u>0000000	Latched status of MPEG Source Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No change in MPEG source infoframe checksum error 1 - An MPEG source infoframe checksum error has triggered this interrupt	
SPD_INF_CKS_ERR_ST			R
0x89	0<u>0</u>000000	Latched status of SPD Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via SPD_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No change in SPD infoframe checksum error 1 - An SPD infoframe checksum error has triggered this interrupt	
AUD_INF_CKS_ERR_ST			R
0x89	00<u>0</u>00000	Latched status of Audio Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No change in Audio infoframe checksum error 1 - An Audio infoframe checksum error has triggered this interrupt	
AVI_INF_CKS_ERR_ST			R
0x89	000<u>0</u>0000	Latched status of AVI Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AVI_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No change in AVI infoframe checksum error 1 - An AVI infoframe checksum error has triggered this interrupt	
AKSV_UPDATE_A_ST			R
0x89	0000000<u>0</u>	Latched status of Port A AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AKSV_UPDATE_A_RAW has not changed. An interrupt has not been generated. 1 - TAKSV_UPDATE_A_RAW has changed. An interrupt has been generated.	
AKSV_UPDATE_B_ST			R
0x89	0000000<u>0</u>	Latched status of Port B AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_A_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AKSV_UPDATE_B_RAW has not changed. An interrupt has not been generated. 1 - TAKSV_UPDATE_B_RAW has changed. An interrupt has been generated.	
MS_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u>0000000	Clear bit for the MPEG Source Infoframe Checksum Error Interrupt. 0 - Does not clear MS_INF_CKS_ERR_ST 1 - Clears MS_INF_CKS_ERR_ST	
SPD_INF_CKS_ERR_CLR			SC
0x8A	0<u>0</u>000000	Clear bit for the SPD Infoframe Checksum Error Interrupt. 0 - Does not clear 1 - Clears SPD_INF_CKS_ERR_ST	
AUD_INF_CKS_ERR_CLR			SC
0x8A	00<u>0</u>00000	Clear bit for the Audio Infoframe Checksum Error Interrupt. 0 - Does not clear AUD_INF_CKS_ERR_ST 1 - Clears AUD_INF_CKS_ERR_ST	
AVI_INF_CKS_ERR_CLR			SC
0x8A	000<u>0</u>0000	Clear bit for the AVI Infoframe Checksum Error Interrupt. 0 - Does not clear AVI_INF_CKS_ERR_ST 1 - Clears AVI_INF_CKS_ERR_ST	

Reg	Bits	Description	
AKSV_UPDATE_A_CLR			SC
0x8A	0000000<u>0</u>	Clear bit for the Port A AKSV Update Interrupt. 0 - Does not clear AKSV_UPDATE_A_ST 1 - Clears AKSV_UPDATE_A_ST	
AKSV_UPDATE_B_CLR			SC
0x8A	0000000<u>0</u>	Clear bit for the Port B AKSV Update Interrupt. 0 - Does not clear AKSV_UPDATE_B_ST 1 - Clears AKSV_UPDATE_B_ST	
MS_INF_CKS_ERR_MB2			R/W
0x8B	<u>0</u>0000000	INT2 interrupt mask for MPEG Source Infoframe Checksum Error interrupt. When set the MPEG Source Infoframe Checksum Error interrupt will trigger the INT2 interrupt and MS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable MPEG Source Infoframe Checksum Error interrupt on INT2 1 - Enable MPEG Source Infoframe Checksum Error interrupt on INT2	
SPD_INF_CKS_ERR_MB2			R/W
0x8B	0<u>0</u>000000	INT2 interrupt mask for SPD Infoframe Checksum Error interrupt. When set the SPD Infoframe Checksum Error interrupt will trigger the INT2 interrupt and SPD_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT2 1 - Enable SPD Infoframe Checksum Error interrupt on INT2	
AUD_INF_CKS_ERR_MB2			R/W
0x8B	00<u>0</u>00000	INT2 interrupt mask for Audio Infoframe Checksum Error interrupt. When set the Audio Infoframe Checksum Error interrupt will trigger the INT2 interrupt and AUDIO_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Audio Infoframe Checksum Error interrupt on INT2 1 - Enable Audio Infoframe Checksum Error interrupt on INT2	
AVI_INF_CKS_ERR_MB2			R/W
0x8B	000<u>0</u>0000	INT2 interrupt mask for AVI Infoframe Checksum Error interrupt. When set the AVI Infoframe Checksum Error interrupt will trigger the INT2 interrupt and AVI_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable AVI Infoframe Checksum Error interrupt on INT2 1 - Enable AVI Infoframe Checksum Error interrupt on INT2	
AKSV_UPDATE_A_MB2			R/W
0x8B	0000000<u>0</u>	INT2 interrupt mask for Port A AKSV Update interrupt. When set the Port A AKSV Update interrupt will trigger the INT2 interrupt and AKSV_UPDATE_A_ST will indicate the interrupt status. 0 - Disables Port A AKSV Update interrupt for INT2. 1 - Enables Port A AKSV Update interrupt for INT2.	
AKSV_UPDATE_B_MB2			R/W
0x8B	0000000<u>0</u>	INT1 interrupt mask for Port B AKSV Update interrupt. When set the Port B AKSV Update interrupt will trigger the INT2 interrupt and AKSV_UPDATE_B_ST will indicate the interrupt status. 0 - Disables Port B AKSV Update interrupt for INT2. 1 - Enables Port B AKSV Update interrupt for INT2.	
MS_INF_CKS_ERR_MB1			R/W
0x8C	<u>0</u>0000000	INT1 interrupt mask for MPEG Source Infoframe Checksum Error interrupt. When set the MPEG Source Infoframe Checksum Error interrupt will trigger the INT1 interrupt and MS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT1 1 - Enable SPD Infoframe Checksum Error interrupt on INT1	
SPD_INF_CKS_ERR_MB1			R/W
0x8C	0<u>0</u>000000	INT1 interrupt mask for SPD Infoframe Checksum Error interrupt. When set the SPD Infoframe Checksum Error interrupt will trigger the INT1 interrupt and SPD_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT1 1 - Enable SPD Infoframe Checksum Error interrupt on INT1	
AUD_INF_CKS_ERR_MB1			R/W
0x8C	00<u>0</u>00000	INT1 interrupt mask for Audio Infoframe Checksum Error interrupt. When set the Audio Infoframe Checksum Error interrupt will trigger the INT1 interrupt and AUDIO_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Audio Infoframe Checksum Error interrupt on INT1 1 - Enable Audio Infoframe Checksum Error interrupt on INT1	
AVI_INF_CKS_ERR_MB1			R/W
0x8C	000<u>0</u>0000	INT1 interrupt mask for AVI Infoframe Checksum Error interrupt. When set the AVI Infoframe Checksum Error interrupt will trigger the INT1 interrupt and AVI_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable AVI Infoframe Checksum Error interrupt on INT1 1 - Enable AVI Infoframe Checksum Error interrupt on INT1	

Reg	Bits	Description
AKSV_UPDATE_A_MB1		R/W
0x8C	0000000<u>0</u>	INT1 interrupt mask for Port A AKSV Update interrupt. When set the Port A AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_A_ST will indicate the interrupt status. 0 - Disables Port A AKSV Update interrupt for INT1. 1 - Enables Port A AKSV Update interrupt for INT1.
AKSV_UPDATE_B_MB1		R/W
0x8C	0000000<u>0</u>	INT1 interrupt mask for Port B AKSV Update interrupt. When set the Port B AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_B_ST will indicate the interrupt status. 0 - Disables Port B AKSV Update interrupt for INT1. 1 - Enables Port B AKSV Update interrupt for INT1.
BG_MEAS_DONE_RAW		R
0x8D	000000<u>0</u>0	Status of Background port Measurement completed interrupt signal. When set to 1 it indicates measurements of TMDS frequency and video parameters on the selected background port have been completed. Once set, this bit will remain high until it is cleared via BG_MEAS_DONE_CLR. 0 - Measurements of TMDS frequency and video parameters of background port not finished or not requested. 1 - Measurements of TMDS frequency and video parameters of background port are ready
VS_INF_CKS_ERR_RAW		R
0x8D	0000000<u>0</u>	Status of Vendor Specific Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for a Vendor Specific Infoframe. Once set, this bit will remain high until it is cleared via VS_INF_CKS_ERR_CLR. 0 - No VS infoframe checksum error has occurred 1 - A VS infoframe checksum error has occurred
BG_MEAS_DONE_ST		R
0x8E	000000<u>0</u>0	Latched status of Background Port Measurement completed interrupt. Once set this bit will remain high until the interrupt has been cleared via BG_MEAS_DONE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Measurements of TMDS frequency and video parameters of background port not finished or not requested. 1 - Measurements of TMDS frequency and video parameters of background port are ready
VS_INF_CKS_ERR_ST		R
0x8E	0000000<u>0</u>	Latched status of MPEG Source Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No change in VS infoframe checksum error 1 - A VS infoframe checksum error has triggered this interrupt
BG_MEAS_DONE_CLR		SC
0x8F	000000<u>0</u>0	Clear bit for the Background Port Measurement completed Interrupt. 0 - Does not clear BG_MEAS_DONE_ST 1 - Clears BG_MEAS_DONE_ST
VS_INF_CKS_ERR_CLR		SC
0x8F	0000000<u>0</u>	Clear bit for the Vendor Specific Infoframe Checksum Error Interrupt. 0 - Does not clear 1 - Clears VS_INF_CKS_ERR_ST
BG_MEAS_DONE_MB2		R/W
0x90	000000<u>0</u>0	INT2 interrupt mask for Background port Measurement completed interrupt. When set the Background port Measurement completed interrupt will trigger the INT2 interrupt and BG_MEAS_DONE_ST will indicate the interrupt status. 0 - Disable Background port Measurement Completed interrupt on INT2 1 - Enable Background port Measurement Completed interrupt on INT2
VS_INF_CKS_ERR_MB2		R/W
0x90	0000000<u>0</u>	INT2 interrupt mask for Vendor Specific Infoframe Checksum Error interrupt. When set the Vendor Specific Infoframe Checksum Error interrupt will trigger the INT2 interrupt and VS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Vendor Specific Infoframe Checksum Error interrupt on INT2 1 - Enable Vendor Specific Infoframe Checksum Error interrupt on INT2
BG_MEAS_DONE_MB1		R/W
0x91	000000<u>0</u>0	INT1 interrupt mask for Background port Measurement completed interrupt. When set the Background port Measurement completed interrupt will trigger the INT1 interrupt and BG_MEAS_DONE_ST will indicate the interrupt status. 0 - Disable Background port Measurement Completed interrupt on INT1 1 - Enable Background port Measurement Completed interrupt on INT1

Reg	Bits	Description
VS_INF_CKS_ERR_MB1		R/W
0x91	0000000<u>0</u>	INT1 interrupt mask for Vendor Specific Infoframe Checksum Error interrupt. When set the Vendor Specific Infoframe Checksum Error interrupt will trigger the INT1 interrupt and VS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Vendor Specific Checksum Error interrupt on INT1 1 - Enable Vendor Specific Checksum Error interrupt on INT1
CEC_RX_RDY2_RAW		R
0x92	00<u>0</u>00000	Raw status of CEC Receiver Buffer 2 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. 0 - No change 1 - CEC Rx buffer 2 has received a complete message which is ready be read by the host
CEC_RX_RDY1_RAW		R
0x92	000<u>0</u>0000	Raw status of CEC Receiver Buffer 1 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 1. 0 - No change 1 - CEC Rx buffer 1 has received a complete message which is ready be read by the host
CEC_RX_RDY0_RAW		R
0x92	0000<u>0</u>000	Raw status of CEC Receiver Buffer 0 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 0. 0 - No change 1 - CEC Rx buffer 0 has received a complete message which is ready be read by the host
CEC_TX_RETRY_TIMEOUT_RAW		R
0x92	00000<u>0</u>00	Raw status of CEC Transmitter retry timeout signal. 0 - No change 1 - CEC TX has retried to send the current message by the no. of times specified in the TX_RETRY_REGISTER but it was unsuccessful every time
CEC_TX_ARBITRATION_LOST_RAW		R
0x92	000000<u>0</u>0	Raw status of CEC Transmitter Arbitration lost signal. 0 - No change 1 - CEC TX has lost arbitration to another TX
CEC_TX_READY_RAW		R
0x92	0000000<u>0</u>	Raw status of CEC Transmitter 'message sent' signal. This bit will be go high whenever the TX has successfully sent a message. 0 - No change 1 - CEC TX has successfully sent the last outgoing message
CEC_RX_RDY2_ST		R
0x93	00<u>0</u>00000	Latched status of CEC_RX_RDY2_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into buffer 2 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 2
CEC_RX_RDY1_ST		R
0x93	000<u>0</u>0000	Latched status of CEC_RX_RDY1_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into buffer 1 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 1
CEC_RX_RDY0_ST		R
0x93	0000<u>0</u>000	Latched status of CEC_RX_RDY0_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into buffer 0 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 0
CEC_TX_RETRY_TIMEOUT_ST		R
0x93	00000<u>0</u>00	Latched status of CEC_TX_RETRY_TIMEOUT_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX fails to send the current message within the number of retry attempts specified by CEC_TX_RETRY this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_RETRY_TIMEOUT_CLR. 0 - No change 1 - CEC TX has tried but failed to resend the current message for the number of times specified by CEC_TX_RETRY

Reg	Bits	Description	
CEC_TX_ARBITRATION_LOST_ST			R
0x93	0000000**0**	Latched status of CEC_TX_ARBITRATION_LOST_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX loses arbitration while trying to send a message this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_ARBITRATION_LOST_CLR. 0 - No change 1 - The CEC TX has lost arbitration to another TX	
CEC_TX_READY_ST			R
0x93	0000000**0**	Latched status of CEC_TX_READY_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When the CEC TX successfully sends the current message this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_READY_CLR. 0 - No change 1 - Message transmitted successfully	
CEC_RX_RDY2_CLR			SC
0x94	00**0**00000	Clear bit for CEC Receiver Buffer 2 Ready interrupt. 0 - Does not clear CEC_RX_RDY2_ST 1 - Clears CEC_RX_RDY2_ST	
CEC_RX_RDY1_CLR			SC
0x94	000**0**0000	Clear bit for CEC Receiver Buffer 1 Ready interrupt. 0 - Does not clear CEC_RX_RDY1_ST 1 - Clears CEC_RX_RDY1_ST	
CEC_RX_RDY0_CLR			SC
0x94	0000**0**000	Clear bit for CEC Receiver Buffer 0 Ready interrupt. 0 - Does not clear CEC_RX_RDY0_ST 1 - Clears CEC_RX_RDY0_ST	
CEC_TX_RETRY_TIMEOUT_CLR			SC
0x94	00000**0**00	Clear bit for CEC Transmitter Retry Timeout interrupt. 0 - Does not clear CEC_TX_RETRY_TIMEOUT_ST 1 - Clears CEC_TX_RETRY_TIMEOUT_ST	
CEC_TX_ARBITRATION_LOST_CLR			SC
0x94	000000**0**0	Clear bit for CEC Transmitter Arbitration Lost interrupt. 0 - Does not clear CEC_TX_ARBITRATION_LOST_ST 1 - Clears CEC_TX_ARBITRATION_LOST_ST	
CEC_TX_READY_CLR			SC
0x94	0000000**0**	Clear bit for CEC Transmitter Ready interrupt. 0 - Does not clear CEC_TX_READY_ST 1 - Clears CEC_TX_READY_ST	
CEC_RX_RDY2_MB2			R/W
0x95	00**0**00000	INT2 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT2 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 2 Ready interrupt on INT2 1 - Enables CEC Receiver Buffer 2 Ready interrupt on INT2	
CEC_RX_RDY1_MB2			R/W
0x95	000**0**0000	INT2 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT2 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 1 Ready interrupt on INT2 1 - Enables CEC Receiver Buffer 1 Ready interrupt on INT2	
CEC_RX_RDY0_MB2			R/W
0x95	0000**0**000	INT2 interrupt mask for CEC Receiver Buffer 0 Ready interrupt. When set the CEC Receiver Buffer 0 Ready interrupt will trigger the INT2 interrupt and CEC_RX_RDY0_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 0 Ready interrupt on INT2 1 - Enables CEC Receiver Buffer 0 Ready interrupt on INT2	
CEC_TX_RETRY_TIMEOUT_MB2			R/W
0x95	00000**0**00	INT2 interrupt mask for CEC Transmitter Retry Timeout interrupt. When set the CEC Transmitter Retry Timeout interrupt will trigger the INT2 interrupt and CEC_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Timeout Retry interrupt on INT2 1 - Enables CEC Receiver Transmitter Timeout Retry interrupt on INT2	

Reg	Bits	Description	
CEC_TX_ARBITRATION_LOST_MB2			R/W
0x95	0000000**0**	INT2 interrupt mask for CEC Transmitter Arbitration Lost interrupt. When set the CEC Transmitter Arbitration Lost interrupt will trigger the INT2 interrupt and CEC_TX_ARBIRATION_LOST_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Arbitration Lost interrupt on INT2 1 - Enables CEC Receiver Transmitter Arbitration Lost interrupt on INT2	
CEC_TX_READY_MB2			R/W
0x95	0000000**0**	INT2 interrupt mask for CEC Transmitter Ready interrupt. When set the CEC Transmitter Ready interrupt will trigger the INT2 interrupt and CEC_TX_RDY_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Ready interrupt on INT2 1 - Enables CEC Receiver Transmitter Ready interrupt on INT2	
CEC_RX_RDY2_MB1			R/W
0x96	0**0**000000	INT1 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 2 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 2 Ready interrupt on INT1	
CEC_RX_RDY1_MB1			R/W
0x96	000**0**0000	INT1 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 1 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 1 Ready interrupt on INT1	
CEC_RX_RDY0_MB1			R/W
0x96	0000**0**000	INT1 interrupt mask for CEC Receiver Buffer 0 Ready interrupt. When set the CEC Receiver Buffer 0 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY0_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 0 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 0 Ready interrupt on INT1	
CEC_TX_RETRY_TIMEOUT_MB1			R/W
0x96	00000**0**00	INT1 interrupt mask for CEC Transmitter Retry Timeout interrupt. When set the CEC Transmitter Retry Timeout interrupt will trigger the INT1 interrupt and CEC_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Timeout Retry interrupt on INT1 1 - Enables CEC Receiver Transmitter Timeout Retry interrupt on INT1	
CEC_TX_ARBITRATION_LOST_MB1			R/W
0x96	0000000**0**	INT1 interrupt mask for CEC Transmitter Arbitration Lost interrupt. When set the CEC Transmitter Arbitration Lost interrupt will trigger the INT1 interrupt and CEC_TX_ARBIRATION_LOST_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Arbitration Lost interrupt on INT1 1 - Enables CEC Receiver Transmitter Arbitration Lost interrupt on INT1	
CEC_TX_READY_MB1			R/W
0x96	0000000**0**	INT1 interrupt mask for CEC Transmitter Ready interrupt. When set the CEC Transmitter Ready interrupt will trigger the INT1 interrupt and CEC_TX_RDY_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Ready interrupt on INT1 1 - Enables CEC Receiver Transmitter Ready interrupt on INT1	
CEC_INT_WAKE_OPCODE7_RAW			R
0x97	**0**0000000	Status of CEC_WAKE_OPCODE7 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE7 is specified by the user via the CEC_WAKE_OPCODE7 register. 0 - WAKE_OPCODE7 not received. 1 - WAKE_OPCODE7 received.	
CEC_INT_WAKE_OPCODE6_RAW			R
0x97	0**0**000000	Status of CEC_WAKE_OPCODE6 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE6 is specified by the user via the CEC_WAKE_OPCODE6 register. 0 - WAKE_OPCODE6 not received. 1 - WAKE_OPCODE6 received.	
CEC_INT_WAKE_OPCODE5_RAW			R
0x97	00**0**00000	Status of CEC_WAKE_OPCODE5 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE5 is specified by the user via the CEC_WAKE_OPCODE5 register. 0 - WAKE_OPCODE5 not received. 1 - WAKE_OPCODE5 received.	
CEC_INT_WAKE_OPCODE4_RAW			R
0x97	000**0**0000	Status of CEC_WAKE_OPCODE4 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE4 is specified by the user via the CEC_WAKE_OPCODE4 register. 0 - WAKE_OPCODE4 not received. 1 - WAKE_OPCODE4 received.	

Reg	Bits	Description	
CEC_INT_WAKE_OPCODE3_RAW			R
0x97	0000**0**000	Status of CEC_WAKE_OPCODE3 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE3 is specified by the user via the CEC_WAKE_OPCODE3 register. 0 - WAKE_OPCODE3 not received. 1 - WAKE_OPCODE3 received.	
CEC_INT_WAKE_OPCODE2_RAW			R
0x97	00000**0**00	Status of CEC_WAKE_OPCODE2 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE2 is specified by the user via the CEC_WAKE_OPCODE2 register. 0 - WAKE_OPCODE2 not received. 1 - WAKE_OPCODE2 received.	
CEC_INT_WAKE_OPCODE1_RAW			R
0x97	000000**0**0	Status of CEC_WAKE_OPCODE1 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE1 is specified by the user via the CEC_WAKE_OPCODE1 register. 0 - WAKE_OPCODE1 not received. 1 - WAKE_OPCODE1 received.	
CEC_INT_WAKE_OPCODE0_RAW			R
0x97	0000000**0**	Status of CEC_WAKE_OPCODE0 received signal. The CEC command that corresponds to CEC_WAKE_OPCODE0 is specified by the user via the CEC_WAKE_OPCODE0 register. 0 - WAKE_OPCODE0 not received. 1 - WAKE_OPCODE0 received.	
CEC_INT_WAKE_OPCODE7_ST			R
0x98	**0**0000000	Latched status of CEC_WAKE_OPCODE7_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE7_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE7 not received. 1 - WAKE_OPCODE7 received.	
CEC_INT_WAKE_OPCODE6_ST			R
0x98	0**0**000000	Latched status of CEC_WAKE_OPCODE6_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE6_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE6 not received. 1 - WAKE_OPCODE6 received.	
CEC_INT_WAKE_OPCODE5_ST			R
0x98	00**0**00000	Latched status of CEC_WAKE_OPCODE5_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE5_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE5 not received. 1 - WAKE_OPCODE5 received.	
CEC_INT_WAKE_OPCODE4_ST			R
0x98	000**0**0000	Latched status of CEC_WAKE_OPCODE4_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE4_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE4 not received. 1 - WAKE_OPCODE4 received.	
CEC_INT_WAKE_OPCODE3_ST			R
0x98	0000**0**000	Latched status of CEC_WAKE_OPCODE3_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE3_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE3 not received. 1 - WAKE_OPCODE3 received.	
CEC_INT_WAKE_OPCODE2_ST			R
0x98	00000**0**00	Latched status of CEC_WAKE_OPCODE2_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE2_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE2 not received. 1 - WAKE_OPCODE2 received.	
CEC_INT_WAKE_OPCODE1_ST			R
0x98	000000**0**0	Latched status of CEC_WAKE_OPCODE1_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE1_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE1 not received. 1 - WAKE_OPCODE1 received.	
CEC_INT_WAKE_OPCODE0_ST			R
0x98	0000000**0**	Latched status of CEC_WAKE_OPCODE0_RAW. Once set this bit will remain high until the interrupt has been cleared via CEC_INT_WAKE_OPCODE0_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - WAKE_OPCODE0 not received. 1 - WAKE_OPCODE0 received.	

Reg	Bits	Description	
CEC_INT_WAKE_OPCODE7_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE7_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE7_ST	
CEC_INT_WAKE_OPCODE6_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE6_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE6_ST	
CEC_INT_WAKE_OPCODE5_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE5_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE5_ST	
CEC_INT_WAKE_OPCODE4_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE4_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE4_ST	
CEC_INT_WAKE_OPCODE3_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE3_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE3_ST	
CEC_INT_WAKE_OPCODE2_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE2_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE2_ST	
CEC_INT_WAKE_OPCODE1_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE1_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE1_ST	
CEC_INT_WAKE_OPCODE0_CLR			SC
0x99	0000000	Clear bit for CEC_INT_WAKE_OPCODE0_ST 0 - No function 1 - Clears CEC_INT_WAKE_OPCODE0_ST	
CEC_INT_WAKE_OPCODE7_MB2			R/W
0x9A	0000000	INT2 interrupt mask for CEC_WAKE_OPCODE7_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE7 is received. 0 - Disables CEC_WAKE_OPCODE7 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE7 received interrupt for INT2	
CEC_INT_WAKE_OPCODE6_MB2			R/W
0x9A	0000000	INT2 interrupt mask for CEC_WAKE_OPCODE6_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE6 is received. 0 - Disables CEC_WAKE_OPCODE6 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE6 received interrupt for INT2	
CEC_INT_WAKE_OPCODE5_MB2			R/W
0x9A	0000000	INT2 interrupt mask for CEC_WAKE_OPCODE5_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE5 is received. 0 - Disables CEC_WAKE_OPCODE5 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE5 received interrupt for INT2	
CEC_INT_WAKE_OPCODE4_MB2			R/W
0x9A	0000000	INT2 interrupt mask for CEC_WAKE_OPCODE4_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE4 is received. 0 - Disables CEC_WAKE_OPCODE4 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE4 received interrupt for INT2	
CEC_INT_WAKE_OPCODE3_MB2			R/W
0x9A	0000000	INT2 interrupt mask for CEC_WAKE_OPCODE3_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE3 is received. 0 - Disables CEC_WAKE_OPCODE3 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE3 received interrupt for INT2	

Reg	Bits	Description	
CEC_INT_WAKE_OPCODE2_MB2			R/W
0x9A	00000**0**00	INT2 interrupt mask for CEC_WAKE_OPCODE2_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE2 is received. 0 - Disables CEC_WAKE_OPCODE2 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE2 received interrupt for INT2	
CEC_INT_WAKE_OPCODE1_MB2			R/W
0x9A	000000**0**0	INT2 interrupt mask for CEC_WAKE_OPCODE1_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE1 is received. 0 - Disables CEC_WAKE_OPCODE1 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE1 received interrupt for INT2	
CEC_INT_WAKE_OPCODE0_MB2			R/W
0x9A	0000000**0**	INT2 interrupt mask for CEC_WAKE_OPCODE0_ST. When set an interrupt will be generated on INT2 if CEC_WAKE_OPCODE0 is received. 0 - Disables CEC_WAKE_OPCODE0 received interrupt for INT2 1 - Enables CEC_WAKE_OPCODE0 received interrupt for INT2	
CEC_INT_WAKE_OPCODE7_MB1			R/W
0x9B	**0**0000000	INT1 interrupt mask for CEC_WAKE_OPCODE7_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE7 is received. 0 - Disables CEC_WAKE_OPCODE7 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE7 received interrupt for INT1	
CEC_INT_WAKE_OPCODE6_MB1			R/W
0x9B	0**0**000000	INT1 interrupt mask for CEC_WAKE_OPCODE6_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE6 is received. 0 - Disables CEC_WAKE_OPCODE6 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE6 received interrupt for INT1	
CEC_INT_WAKE_OPCODE5_MB1			R/W
0x9B	00**0**00000	INT1 interrupt mask for CEC_WAKE_OPCODE5_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE5 is received. 0 - Disables CEC_WAKE_OPCODE5 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE5 received interrupt for INT1	
CEC_INT_WAKE_OPCODE4_MB1			R/W
0x9B	000**0**0000	INT1 interrupt mask for CEC_WAKE_OPCODE4_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE4 is received. 0 - Disables CEC_WAKE_OPCODE4 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE4 received interrupt for INT1	
CEC_INT_WAKE_OPCODE3_MB1			R/W
0x9B	0000**0**000	INT1 interrupt mask for CEC_WAKE_OPCODE3_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE3 is received. 0 - Disables CEC_WAKE_OPCODE3 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE3 received interrupt for INT1	
CEC_INT_WAKE_OPCODE2_MB1			R/W
0x9B	00000**0**00	INT1 interrupt mask for CEC_WAKE_OPCODE2_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE2 is received. 0 - Disables CEC_WAKE_OPCODE2 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE2 received interrupt for INT1	
CEC_INT_WAKE_OPCODE1_MB1			R/W
0x9B	000000**0**0	INT1 interrupt mask for CEC_WAKE_OPCODE1_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE1 is received. 0 - Disables CEC_WAKE_OPCODE1 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE1 received interrupt for INT1	
CEC_INT_WAKE_OPCODE0_MB1			R/W
0x9B	0000000**0**	INT1 interrupt mask for CEC_WAKE_OPCODE0_ST. When set an interrupt will be generated on INT1 if CEC_WAKE_OPCODE0 is received. 0 - Disables CEC_WAKE_OPCODE0 received interrupt for INT1 1 - Enables CEC_WAKE_OPCODE0 received interrupt for INT1	
SDP_STD_CHANGED_RAW			R
0x9C	0000**0**000	Raw status of SDP Standard changed signal. 1 - SDP auto detect result has changed	

Reg	Bits	Description	
SDP_BURST_LOCKED_RAW			R
0x9C	000000<u>0</u>0	Raw Status of SDP Burst lock signal 1 - SDP is color locked	
SDP_VIDEO_DETECTED_RAW			R
0x9C	0000000<u>0</u>	Raw status of Video detected signal. 1 - Video detected at SDP input	
SDP_STD_CHANGED_ST			R
0x9D	0000<u>0</u>000	Latched status for SDP Standard Changed interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SDP_STD_CHANGED_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change. An interrupt has not been generated from this register. 1 - SDP_STD_CHANGED_RAW has changed and generated an interrupt.	
SDP_BURST_LOCKED_ST			R
0x9D	000000<u>0</u>0	Latched status for SDP Burst Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SDP_BURST_LOCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change. An interrupt has not been generated from this register. 1 - SDP_BURST_LOCKED_RAW has changed and generated an interrupt.	
SDP_VIDEO_DETECTED_ST			R
0x9D	0000000<u>0</u>	Latched status for SDP Video Detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SDP_VIDEO_DETECTED_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change. An interrupt has not been generated from this register. 1 - SDP_VIDEO_DETECTED_RAW has changed and generated an interrupt.	
SDP_STD_CHANGED_CLR			SC
0x9E	0000<u>0</u>000	Clear bit for SDP Standard Detection Change interrupt. 0 - Does not clear SDP_STD_CHANGED_ST 1 - Clears SDP_STD_CHANGED_ST	
SDP_BURST_LOCKED_CLR			SC
0x9E	000000<u>0</u>0	Clear bit for SDP Burst Lock interrupt. 0 - Does not clear SDP_BURST_LOCKED_ST 1 - Clears SDP_BURST_LOCKED_ST	
SDP_VIDEO_DETECTED_CLR			SC
0x9E	0000000<u>0</u>	Clear bit for SDP Video detected Interrupt. 0 - Does not clear SDP_VIDEO_DETECTED_S 1 - Clears SDP_VIDEO_DETECTED_ST	
SDP_STD_CHANGED_MB2			R/W
0x9F	0000<u>0</u>000	INT2 interrupt mask for SDP Standard Detection Change interrupt. When set the SDP Standard Detection Change interrupt will trigger the INT2 interrupt and SDP_STD_CHANGED_ST will indicate the interrupt status. 0 - Disables SDP Standard Detection Change interrupt on INT2 1 - Enables SDP Standard Detection Change interrupt on INT2	
SDP_BURST_LOCKED_MB2			R/W
0x9F	000000<u>0</u>0	INT2 interrupt mask for SDP Burst Lock interrupt. When set the SDP Burst Lock interrupt will trigger the INT2 interrupt and SDP_BURST_LOCK_ST will indicate the interrupt status. 0 - Disables SDP Burst Lock interrupt on INT2 1 - Enables SDP Burst Lock interrupt on INT2	
SDP_VIDEO_DETECTED_MB2			R/W
0x9F	0000000<u>0</u>	INT2 interrupt mask for SDP Video Detected interrupt. When set the SDP Burst Lock interrupt will trigger the INT2 interrupt and SDP_BURST_LOCK_ST will indicate the interrupt status. 0 - Disables SDP Video Detected interrupt on INT2 1 - Enables SDP Video Detected interrupt on INT2	
SDP_STD_CHANGED_MB1			R/W
0xA0	0000<u>0</u>000	INT1 interrupt mask for SDP Standard Detection Change interrupt. When set the SDP Standard Detection Change interrupt will trigger the INT1 interrupt and SDP_STD_CHANGED_ST will indicate the interrupt status. 0 - Disables SDP Standard Detection Change interrupt on INT1 1 - Enables SDP Standard Detection Change interrupt on INT1	
SDP_FIFO_CRISIS_MB1			R/W
0xA0	000000<u>0</u>0	INT1 interrupt mask for SDP FIFO Crisis interrupt. When set the SDP FIFO Crisis interrupt will trigger the INT1 interrupt and SDP_FIFO_CRISIS_ST will indicate the interrupt status. 0 - Disables SDP FIFO Crisis interrupt on INT1 1 - Enables SDP FIFO Crisis interrupt on INT1	

Reg	Bits	Description	
SDP_BURST_LOCKED_MB1			R/W
0xA0	0000000<u>0</u>	INT1 interrupt mask for SDP Burst Lock interrupt. When set the SDP Burst Lock interrupt will trigger the INT1 interrupt and SDP_BURST_LOCK_ST will indicate the interrupt status. 0 - Disables SDP Burst Lock interrupt on INT1 1 - Enables SDP Burst Lock interrupt on INT1	
SDP_VIDEO_DETECTED_MB1			R/W
0xA0	0000000<u>0</u>	INT1 interrupt mask for SDP Video Detected interrupt. When set the SDP Burst Lock interrupt will trigger the INT1 interrupt and SDP_BURST_LOCK_ST will indicate the interrupt status. 0 - Disables SDP Video Detected interrupt on INT1 1 - Enables SDP Video Detected interrupt on INT1	
PIN_CHECKER_EN			R/W
0xD6	0000000<u>0</u>	Pseudo boundary scan scheme is implemented on pixel pins P[29:0]. When enabled by setting PIN_CHECKER_EN high, the 8-bit word in PIN_CHECKER_OP is mapped to the pixel pins. 0 - Disabled by default 1 - The 8-bit word in PIN_CHECKER_VAL is mapped to the pins outlined in the description	
PIN_CHECKER_VAL[7:0]			R/W
0xD7	<u>00000000</u>	A control to set the used for the pin checker feature. PIN_CHECKER_VAL is output on the following pins when PIN_CHECKER_EN is set: PIN_CHECKER_VAL output on P[7:0] PIN_CHECKER_VAL output on P[15:8] PIN_CHECKER_VAL output on P[23:16] PIN_CHECKER_VAL output on P[31:24] PIN_CHECKER_VAL output on P[35:32] PIN_CHECKER_VAL[7] output on SYNC_OUT PIN_CHECKER_VAL[6] output on FIELD/DE PIN_CHECKER_VAL[5] output on VS PIN_CHECKER_VAL[4] output on HS	
MAN_OP_CLK_SEL_EN			R/W
0xDD	<u>0</u>0000000	A control to select between automatic and manual output clock selection. 0 - Automatic output clock selection based on OP_FORMAT_SEL 1 - Manual output clock selection as defined by MAN_OP_CLK_SEL[2:0].	
MAN_OP_CLK_SEL[2:0]			R/W
0xDD	0<u>000</u>0000	A control to select the manual output clock. MAN_OP_CLK_SEL_EN must be set to 1 for this control to be valid. 000 - 1x Data clk (CP_CLK) 001 - 2x data clk (2x CP_CLK) 010 - 0.5 Data clk (half CP_CLK) 011 - 90 deg phase shifted 1xData clk (ddr_clk) 100 - Reserved. Do not use. 101 - Reserved. Do not use. 110 - Reserved. Do not use. 111 - Reserved. Do not use.	
DS_WITHOUT_FILTER			R/W
0xE0	<u>0</u>0000000	Disables the chroma filters on channel B and C while keeping the downsampler functional 0 - Filters and downsamples 1 - Downsamples only (no filtering)	
DPP_LUMA_HBW_SEL			R/W
0xE7	00<u>0</u>00000	A control to select the DPP Luma filter bandwidth for stage 2 filters. 0 - Select Low bandwidth (0.44Fs) Higher stopband attenuation 1 - Select High bandwidth (0.47 Fs) Lower stop-band attenuation	
DPP_CHROMA_LOW_EN			R/W
0xE7	000<u>0</u>0000	A control to select DPP Chroma filter bandwidth for stage 2 filters. 0 - High bandwidth, sharp transition filter for channels B/C 1 - Soft filter with minimized ringing for channels B/C	
RD_INFO[15:0]			R
0xEA 0xEB	<u>00000000</u> <u>00000000</u>	Silicon Revision ID. 0x2001 - ADV7844 ES2 Silicon All other values - Invalid for ADV7844	
SDP_SLAVE_ADDR[6:0]			R/W
0xF1	<u>0000000</u>0	Programmable I2C slave address for SDP. This register must be programmed with a valid I2C slave address before the SDP I2C map will be accessible.	
SDP_IO_SLAVE_ADDR[6:0]			R/W
0xF2	<u>0000000</u>0	Programmable I2C slave address for SDP_IO. This register must be programmed with a valid I2C slave address before the SDP IO I2C map will be accessible.	
AVLINK_SLAVE_ADDR[6:0]			R/W
0xF3	<u>0000000</u>0	Programmable I2C slave address for AV.Link map. This register must be programmed with a valid I2C slave address before theAV.Link I2C map will be accessible.	

Reg	Bits	Description	
CEC_SLAVE_ADDR[6:0]			R/W
0xF4	0000000	Programmable I2C slave address for CEC map. This register must be programmed with a valid I2C slave address before the CEC I2C map will be accessible.	
INFOFRAME_SLAVE_ADDR[6:0]			R/W
0xF5	0000000	Programmable I2C slave address for Infoframe map. This register must be programmed with a valid I2C slave address before the Infoframe I2C map will be accessible.	
AFE_SLAVE_ADDR[6:0]			R/W
0xF8	0000000	Programmable I2C slave address for AFE map. This register must be programmed with a valid I2C slave address before the AFE I2C map will be accessible.	
KSV_SLAVE_ADDR[6:0]			R/W
0xF9	0000000	Programmable I2C slave address for Repeater map. This register must be programmed with a valid I2C slave address before the Repeater I2C map will be accessible.	
EDID_SLAVE_ADDR[6:0]			R/W
0xFA	0000000	Programmable I2C slave address for EDID map. This register must be programmed with a valid I2C slave address before the EDID I2C map will be accessible.	
HDMI_SLAVE_ADDR[6:0]			R/W
0xFB	0000000	Programmable I2C slave address for HDMI map. This register must be programmed with a valid I2C slave address before the HDMI I2C map will be accessible.	
CP_SLAVE_ADDR[6:0]			R/W
0xFD	0000000	Programmable I2C slave address for CP map. This register must be programmed with a valid I2C slave address before the CP I2C map will be accessible.	
VDP_SLAVE_ADDR[6:0]			R/W
0xFE	0000000	Programmable I2C slave address for VDP map. This register must be programmed with a valid I2C slave address before the VDP I2C map will be accessible.	
MAIN_RESET			SC
0xFF	0	This control is used to reset the I2C registers to their default values. 0 - No function 1 - Applies main I2C reset	
VDP_RESET			SC
0xFF	0	This control is used to reset the VDP FIFO and controller. 0 - No function 1 - Apply VDP reset	
SDP_RESET			SC
0xFF	0	This control is used to reset the SDP. 0 - No function 1 - Applies SDP reset	
SDP_MEM_RESET			SC
0xFF	0	Memory interface reset 0 - No function 1 - Apply SDP Memory reset	

2.2 CP MAP

Reg	Bits	Description	
RB_CSC_SCALE[1:0]			R
0x0B	00000000	Readback of CSC scale applied to CSC coefficients xx - Readback value	
RB_A4[12:0]			R
0x0B 0x0C	00000000 00000000	Readback of CSC coefficient A4 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_A3[12:0]			R
0x0D 0x0E	00000000 00000000	Readback of CSC coefficient A3 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_A2[12:0]			R
0x0E 0x0F 0x10	00000000 00000000 00000000	Readback of CSC coefficient A2 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_A1[12:0]			R
0x10 0x11	00000000 00000000	Readback of CSC coefficient A1 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_B4[12:0]			R
0x12 0x13	00000000 00000000	Readback of CSC coefficient B4 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_B3[12:0]			R
0x14 0x15	00000000 00000000	Readback of CSC coeff B3 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_B2[12:0]			R
0x15 0x16 0x17	00000000 00000000 00000000	Readback of CSC coeff B2 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_B1[12:0]			R
0x17 0x18	00000000 00000000	Readback of CSC coeff B1 modified by video adjustment block xxxxxxxxxxxxx - Readback value	
RB_C4[12:0]			R
0x19 0x1A	00000000 00000000	Readback of CSC coefficient C4 modified by video adjustment block xxxxxxxxxxxxx - Readback value	
RB_C3[12:0]			R
0x1B 0x1C	00000000 00000000	Readback of CSC coefficient C3 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_C2[12:0]			R
0x1C 0x1D 0x1E	00000000 00000000 00000000	Readback of CSC coefficient C2 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
RB_C1[12:0]			R
0x1E 0x1F	00000000 00000000	Readback of CSC coeff C1 modified by video adjustment block. xxxxxxxxxxxxx - Readback value	
CP_START_HS[12:0]			R/W
0x22 0x23	00000000 00000000	A control to set the position of the start of the HSync output signal in the CP core in Autographic mode only. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x0000 - Default value	

Reg	Bits	Description	
CP_END_HS[12:0]			R/W
0x24 0x25	00000<u>00000</u> <u>00000000</u>	A control to set the position of the end of the HSync output signal in the CP core in Autographic mode only. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x0000 - Default value	
CP_START_SAV[12:0]			R/W
0x26 0x27	00000<u>00000</u> <u>00000000</u>	Manual value for Start of Active Video (SAV) position. Sets the total number of pixels between the start of non active video and the start of active video. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x0000 - Default value	
CP_START_EAV[12:0]			R/W
0x28 0x29	00000<u>00000</u> <u>00000000</u>	Manual value for End of Active Video (EAV) position. Sets the total number of pixels between the end of non active video and the end of active video. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x0000 - Default value	
CP_START_VBI_R[11:0]			R/W
0x2A 0x2B	<u>00000000</u> <u>0000</u>0000	A control to manually set value for start position of VBI region. That is the extra blank region preceeding the odd right (R) field in the 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation this parameter is automatically calculated from the input. 0x000 - Default value	
CP_END_VBI_R[11:0]			R/W
0x2B 0x2C	0000<u>0000</u> <u>00000000</u>	A control to manually set the value for end of VBI position. That is the extra blank region preceding the odd R field in 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation this parameter is automatically calculated from the input. 0x000 - Default value	
CP_START_VBI_EVEN_R[11:0]			R/W
0x2D 0x2E	<u>00000000</u> <u>0000</u>0000	A control to manually set the value for start position of the VBI region. That is the extra blank region preceding the even R field in 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation this parameter is automatically calculated from the input. 0x000 - Default value	
CP_END_VBI_EVEN_R[11:0]			R/W
0x2E 0x2F	0000<u>0000</u> <u>00000000</u>	A control to manually set the value for end position of the VBI. That is the extra blank region preceding the even R field in 3D TV field alternative packing format through HDMI. It is not required to set this value. In normal operation this parameter is automatically calculated from the input. 0x000 - Default value	
DE_V_START_R[3:0]			R/W
0x30	<u>0000</u>0000	A control to adjust the start position of the extra VBI region between L and R fields during an odd field in in 3D TV video field alternative packing format supported by HDMI. This register stores a signed value represented in a 2's complement format. The unit of adjustment is one line. 1000 … 1111 - (-8 lines … -1 line) 0000 - Default value (0 lines) 0001 … 0111 - (1 line … 7 lines)	
DE_V_END_R[3:0]			R/W
0x30	0000<u>0000</u>	A control to adjust the end position of the extra VBI region between L and R fields during the odd field in the 3D TV field alternative packing format supported by HDMI. This register stores a signed value represented in a 2's complement format. The unit of adjustment is one line. 1000 … 1111 - (-8 lines … -1 line) 0000 - Default value (0 lines) 0001 … 0111 - (1 line … 7 lines)	
DE_V_START_EVEN_R[3:0]			R/W
0x31	<u>0000</u>0000	A control to adjust the start position extra VBI region between L and R fields during even field in the 3D TV field alternative packing format supported by HDMI. This register stores a signed value represented in a 2's complement format. The unit of adjustment is one line. 1000 … 1111 - (-8 lines … -1 line) 0000 - Default value (0 lines) 0001 … 0111 - (1 line … 7 lines)	

Reg	Bits	Description	
DE_V_END_EVEN_R[3:0]			R/W
0x31	00000000	A control to adjust the end position of the extra VBI region between L and R fields during even field in the 3D TV field alternative packing format supported by HDMI. This register stores a signed value represented in a 2's complement format. The unit of adjustment is one line. 1000 … 1111 - (-8 lines … -1 line) 0000 - Default value (0 lines) 0001 … 0111 - (1 line … 7 lines)	
BR_NOISE_SHAPING_EN			R/W
0x36	00000000	Enables a noise shaped truncation of the data from 12 bits to 10 bits or 8 bits (as specified by CP_PREC[1:0]) 0 - Disables noise shaped bit reduction. Simple rounding is used for bit reduction 1 - Enables noise shaped bit width reduction.	
BR_NOISE_SHAPING_MODE			R/W
0x36	00000000	A control to select the bit reduction noise shaping mode. This bit is effective if BR_NOISE_SHAPING_EN is set 1. This feature should only be used in HDMI modes. 0 - Noise Shaping Mode 0 1 - Noise Shaping Mode 1	
BR_NOISE_SHAPING_GAIN[1:0]			R/W
0x36	00000000	A control set the gain applied to the noise shaping bit in mode 1. 00 - Gain of 1 01 - Gain of 2 10 - Gain of 4 11 - Gain of 8	
TEN_TO_EIGHT_CONV			R/W
0x36	00000000	A control to indicate if the precision of the data to be rounded and truncated to 8-bit has 10 bit precision. This control is for HDMI use only. 0 - If the input data has got 12 bit precision - then the output data will have 12-, 10- or 8-bits per channel. If the input data has got 10 bit precision - then the output data will have 10-bits per channel. If the input data has got 8 bit precision - then the output data will have 8-bits per channel. 1 - If The input data has got 10 bit precision, the output data will be 8 bits per channel.	
CP_CONTRAST[7:0]			R/W
0x3A	10000000	A control to set the contrast. This field is an unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value which is either 0 or 1. The seven LSBs represents the fractional part of the contrast value. The fractional part has the range [0 to 0.99]. This control is functional if VID_ADJ_EN is set to 1.	
CP_SATURATION[7:0]			R/W
0x3B	10000000	A control to set the saturation. This field is an unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value which is either 0 or 1. The seven LSBs represent the fractional part of the saturation value. The fractional part has a [0 to 0.99] range. This control is functional if VID_ADJ_EN is set to 1.	
CP_BRIGHTNESS[7:0]			R/W
0x3C	00000000	A control to set the brightness. This field is a signed value. The effective brightness value applied to the Luma is obtained by multiplying the programmed value CP_BRIGHTNESS with a gain of 4. The brightness applied to the Luma has a range of [-512 to 508]. This control is functional if VID_ADJ_EN is set to 1. 00000000 - The offset applied to the Luma is 0 . 01111111 - The offset applied to the Luma is 508d. This value corresponds to the brightness setting. 11111111 - The offset applied to the Luma is -512d. This value corresponds to the darkest setting.	
CP_HUE[7:0]			R/W
0x3D	00000000	A control to set the hue. This register a represent an unsigned value which provides hue adjustment. The effective hue applied to the Chroma is [(CP_HUE[7:0] * 180)/256 - 90]. The range of the effective hue applied to the Chroma is [-90° to 90°]. This control is functional if VID_ADJ_EN is set to 1. 00000000 - A hue of -90° is applied to the Chroma 00001111 - A hue of 0° is applied to the Chroma 11111111 - A hue of 90° is applied to the Chroma	
VID_ADJ_EN			R/W
0x3E	00000100	Video Adjustment Enable. This control selects whether or not the color controls feature is enabled. The color controls feature is configured via the parameters CP_CONTRAST[7:0], CP_SATURATION[7:0], CP_BRIGHTNESS[7:0] and CP_HUE[7:0]. The CP CSC must also be enabled for the color controls to be effective. 0 - Disable color controls. 1 - Enable color controls.	

Reg	Bits	Description
CP_UV_ALIGN_SEL[1:0]		R/W
0x3E	0000<u>00</u>100	A control to adjust the timing of the chroma stream. This control adjust the timing of the Cr and Cb interlaved stream output by the CP core for 4:2:2 output modes. 00 - The chroma stream is synchroneous with the start of the active video 01 - The chroma stream is synchroneous with the leading edge of the Hsync 10 - The chroma stream is synchroneous with the leading edge of the DE 11 - The chroma stream is synchronised with the start of the active video
CP_UV_DVAL_INV		R/W
0x3E	0000<u>0</u>100	A control to swap the order of the Cr and Cb in the chroma stream for 4:2:2 output modes. 0 - Do not swap the order of the Cr and Cb samples 1 - Swap the order of the Cr and Cb samples
CP_MODE_GAIN_ADJ_EN		R/W
0x3E	00000<u>1</u>00	A control to enable pregain 0 - The pregain block is bypassed 1 - The pregain block is enabled
ALT_SAT_UV_MAN		R/W
0x3E	000001<u>0</u>0	U and V Saturation Range Control 0 - The range of the saturator on the Cr and the Cb channels are determined by OP_656_RANGE and ALT_DATA_SAT. 1 - The range of the saturator on the Cr and the Cb channels are determined by ALT_SAT_UV if either OP_656_RANGE or ALT_DATA_SAT is set to 0.
ALT_SAT_UV		R/W
0x3E	0000010<u>0</u>	Cr and Cb Saturation Range. Refer to ALT_SAT_UV_MAN for additional detail. 0 - The range of the saturators on channels Cr and Cb is 15-to-235. 1 - The range of the saturators on channels Cr and Cb is 16-to-240.
CP_MODE_GAIN_ADJ[7:0]		R/W
0x40	<u>01011100</u>	Pregain adjustment to compensate for the gain of the Analog Front End. This register stores a value in a 1.7 binary format. 0xxxxxxx - Gain of (0 + (xxxxxxx / 128)) 01011100 - Default pregain (pregain of 0.718) 1xxxxxxx - Gain of (1 + (xxxxxxx / 128))
CH2_POL_MAN_EN		R/W
0x41	<u>0</u>0000010	A control to override the polarity detection by sync channel 2 SSPD 0 - Use result from sync channel 2 SSPD autodetection 1 - Use CH2_POL_VS and CH2_POL_HS
CH2_POL_VS		R/W
0x41	0<u>0</u>000010	A control to override for polarity of VSync by sync channel 2 SSPD. CH2_POL_MAN_EN must be set high for this control to be active. 0 - VSync input to sync channel 2 carries negative polarity signal. 1 - VSync input to sync channel 2 carries positive polarity signal.
CH2_POL_HSCS		R/W
0x41	00<u>0</u>00010	A control to override the polarity of HSync by to sync channel 2 SSPD. CH2_POL_MAN_EN must be set high for this control to be effective. 0 - HSync input to sync channel 2 carries negative polarity signal (HSync or CSync). 1 - HSync input to sync channel 2 carries positive polarity signal (HSync or CSync).
CH2_SYNC_SRC[1:0]		R/W
0x41	000<u>00</u>010	A control to select to synchronization signals processed by sync channel 2 SSPD 00 - Auto detect mode for synchronization source. Use results of auto detection for synchronization signal routing. Result can be read back via CH2_CUR_SYNC[1:0] bits. 01 - Manual setting: separate HSync and VSync to the sync channel 2 SSPD 10 - Manual setting: CSync on HSync input to the sync channel 2 11 - Manual setting: embedded synchronization signal input to the sync channel 2
CH2_TRIG_SSPD		R/W
0x41	00000<u>0</u>10	Trigger synchronization source and polarity detector for sync channel 2 SSPD. A 0 to 1 transition in this bit restarts the auto-sync detection algorithm. This is not a self-clearing bit and must be set to 0 to prepare for next trigger. 0 - Default value - transition 0 to 1 restarts auto-sync detection algorithm 1 - Transition 0 to 1 restarts auto-sync detection algorithm
CH2_SSPD_CONT		R/W
0x41	000000<u>1</u>0	A control to set the synchronization source polarity detection mode for sync channel 2 SSPD. 0 - sync channel 2 SSPD works in one-shot mode (triggered by a 0 to 1 transition on the CH2_TRIG_SSPD bit) 1 - sync channel 2 SSPD works in continuous mode

Reg	Bits	Description
CH2_SSPD_PP_EN		R/W
0x41	0000001<u>0</u>	A control to enable sync channel 2 SSPD post processing 0 - Disable post processing of the synchronization signals input to sync channel 2 SSPD 1 - Check for activity on embedded synchronization signal input to sync channel 2 SSPD when it detects activity on HSync/CSync and VSync. Activity on the embedded signal input to sync channel 2 SSPD is reported by CH2_RS_ACTIVE. The post processing of the synchronization signal input to sync channel 2 SSPD works only if the timing on the embedded synchronization signal and the timing on the HSync/CSync and VSync signals are the same.
CH2_TRIG_STDI		R/W
0x42	00111<u>0</u>11	Triggers standard identification of sync channel 2 STDI. A 0 to 1 transition on this bit triggers the STDI measurements. This is not self-clearing and must be set to 0 to prepare for the next STDI measurements. 0 - Default value - transition 0 to 1 restarts auto-sync detection algorithm 1 - Transition 0 to 1 restarts auto-sync detection algorithm
CH2_STDI_CONT		R/W
0x42	00111<u>1</u>11	A control to select the sync channel 2 STDI mode of operation 0 - sync channel 2 STDI block operates in single-shot mode. 0 to 1 transition on CH2_TRIG_STDI triggers a measurement of the sync channel 2 STDI block. 1 - sync channel 2 STDI runs in continuous mode
CH2_FL_FR_THRESHOLD[2:0]		R/W
0x43	11<u>010</u>100	Threshold for difference between input video field length and internally stored standard to enter and exit freerun. This control is for the sync channel 2 STDI. 000 - Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines. 001 - Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines. 010 - Minimum difference to switch into free run is 10 lines. Maximum difference to switch out of free run is 7 lines. 011 - Minimum difference to switch into free run is 4 lines. Maximum difference to switch out of free run is 3 lines. 100 - Minimum difference to switch into free run is 51 lines. Maximum difference to switch out of free run is 46 lines. 101 - Minimum difference to switch into free run is 69 lines. Maximum difference to switch out of free run is 63 lines. 110 - Minimum difference to switch into free run is 134 lines. Maximum difference to switch out of free run is 127 lines. 111 - Minimum difference to switch into free run is 263 lines. Maximum difference to switch out of free run is 255 lines.
CH2_F_RUN_THR[2:0]		R/W
0x43	11010<u>100</u>	Free run threshold select for sync channel 2. Determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and compared to an internally stored parameter. The magnitude of the difference decides whether or not sync channel 2 will enter free run mode. 000 - Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1. 001 - Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200. 010 - Minimum difference to switch into free run is 128. Maximum difference to switch out of free run is 112. 011 - Minimum difference to switch into free run is 64. Maximum difference to switch out of free run is 48. 100 - Minimum difference to switch into free run is 32. Maximum difference to switch out of free run is 24. 101 - Minimum difference to switch into free run is 16. Maximum difference to switch out of free run is 12. 110 - Minimum difference to switch into free run is 8. Maximum difference to switch out of free run is 6. 111 - Minimum difference to switch into free run is 4. Maximum difference to switch out of free run is 3.
CH2_FR_FIELD_LENGTH[10:0]		R/W
0x46 0x47	<u>00000000</u> <u>000</u>00000	Ideal number of lines per field used by the CP core for the free run decision for sync channel 2. If set to 0 the ideal number of lines per field is dictated by CP_LCOUNT_MAX[11:0]. 0x000 - Default value
CH2_FR_LL[10:0]		R/W
0x47 0x48	00000<u>000</u> <u>00000000</u>	Free run line length in number of crystal clock cycles in one line of video for sync channel 2 STDI. This register should only be programmed for video standards that are not supported by PRIM_MODE[3:0] and VID_STD[5:0]. 0x000 - Actually used internal free run line length is decoded from PRIM_MODE[3:0] and VID_STD[5:0]. All other values - Number of crystal clocks in the ideal line length. Used to enter or exit free run mode.
CH2_STDI_DVALID		R
0x49	<u>0</u>0000000	This bit is set when the measurements performed by sync channel 2 STDI are completed. High level signals validity for CH2_BL, CH2_LCF, CH2_LCVS, CH2_FCL, and CH2_STDI_INTLCD parameters. To prevent false readouts, especially during signal acquisition, CH2_SDTI_DVALID only goes high after four fields with same length are recorded. As a result, STDI measurements can take up to five fields to finish. 0 - Sync channel 2 STDI measurement are not valid 1 - Sync channel 2 STDI measurement are valid

Reg	Bits	Description	
CH2_STDI_INTLCD			R
0x49	0<u>0</u>000000	Interlaced vs. progressive mode detected by sync channel 2 STDI. The readback from this register is valid if CH2_STDI_DVALID is high. 0 - Indicates a video signal on sync channel 2 with non interlaced timing. 1 - Indicates a signal on sync channel 2 with interlaced timing.	
CH2_BL[13:0]			R
0x49 0x4A	00<u>000000</u> <u>00000000</u>	A readback for the sync channel 2 Block Length. Number of crystal clock cycles in a block of eight lines of incoming video. This readback is valid if CH2_STDI_DVALID is high. xxxxxxxxxxxxxx - Readback value	
CH2_LCVS[4:0]			R
0x4B	<u>00000</u>000	A readback for the sync channel 2 Line Count in a VSync. Number of lines in a VSync period measured on sync channel 2. The readback from this field is valid if CH2_STDI_DVALID is high. xxxxx - Readback value	
CH2_LCF[10:0]			R
0x4B 0x4C	00000<u>000</u> <u>00000000</u>	A readback for the sync channel 2 Line Count in a Field Number of lines between two VSyncs measured on sync channel 2. The readback from this field is valid if CH2_STDI_DVALID is high. xxxxxxxxxx - Readback value	
CH2_FCL[12:0]			R
0x4D 0x4E	000<u>00000</u> <u>00000000</u>	A readback for the sync channel 2 Field Count Length Number of crystal clock cycles between successive VSyncs measured by sync channel 2 STDI or in 1/256th of a field. The readback from this field is valid if CH2_STDI_DVALID is high. xxxxxxxxxxxx - Readback value	
CH2_SSPD_DVALID			R
0x4F	<u>0</u>0000000	CH2_SSPD_DVALID is set to 1 when the read backs from the SSPD section of the synchronization Sync channel 2 are valid. This bit is set to 1 after 2^22 crystal clock periods following a reset of the CP section. This bit is set to 0 when the DUT is reset. 0 - Sync channel 2 SSPD results not valid for readback 1 - Sync channel 2 SSPD results valid (detection finished)	
CH2_VS_ACT			R
0x4F	0<u>0</u>000000	A Readback indicating the activity the VSync input to sync channel 2 SSPD. 0 - No activity detected on the VSync input to sync channel 2 SSPD 1 - The VSync input to sync channel 2 SSPD carries an active signal	
CH2_CUR_POL_VS			R
0x4F	00<u>0</u>00000	A Readback indicating the polarity of the VSync input to sync channel 2 SSPD 0 - The VSync input to sync channel 2 SSPD has negative polarity signal 1 - The VSync input to sync channel 2 SSPD has positive polarity signal	
CH2_HS_ACT			R
0x4F	000<u>0</u>0000	A Readback indicating activity on the HSync CSync input to sync channel 2 SSPD 0 - No activity detected on the HSync/CSync input to sync channel 2 SSPD 1 - HSync/CSync input to sync channel 2 SSPD carries an active signal	
CH2_CUR_POL_HS			R
0x4F	0000<u>0</u>000	A Readback indicating the polarity of the HSync/CSync input to sync channel 2 SSPD 0 - The HSync CSync input to sync channel 2 SSPD has negative polarity 1 - The HSync CSync input to sync channel 2 SSPD has positive polarity	
CH2_RS_ACTIVE			R
0x4F	00000<u>0</u>00	A readback indicating activity in embedded synchronization signal input to sync channel 2 SSPD. CH2_SSPD_PP_EN must be set to 1 and CH1_SSPD_DVALID must return 1 for this readback to be valid. This is readback is only valid when there is a HSync and VSync signal present. It is not valid to use this bit when only embedded signal is present. The purpose of this bit is to indicate that the user can switch to embedded sync if using HSync and VSync inputs. 0 - Activity detected on the embedded signal input to sync channel 2 SSPD 1 - No activity detected on the embedded signal input to sync channel 2 SSPD	
CH2_CUR_SYNC_SRC[1:0]			R
0x4F	000000<u>00</u>	Readback of current synchronization source detected by sync channel 2 SSPD. 00 - Not used 01 - Activity detected on HSync and VSync input to sync channel 2 SSPD 10 - CSync detected in the HSync input to sync channel 2 SSPD 11 - Activity detected on embedded synchronization input to sync channel 2 SSPD	

Reg	Bits	Description	
CSC_SCALE[1:0]			R/W
0x52	01000000	A control to set the CSC coefficient scalar. 00 - CSC scalar set to 1 01 - CSC scalar set to 2 10 - Reserved. Do not use 11 - Reserved. Do not use	
A4[12:0]			R/W
0x52 0x53	01000000 00000000	CSC Coefficient A4. Contains 13-bit A4 coefficient for the A channel. 0x0000 - Default value	
A3[12:0]			R/W
0x54 0x55	00000000 00000000	CSC Coefficient A3. Contains 13-bit A3 coefficient for the A channel. 0x0000 - Default value	
A2[12:0]			R/W
0x55 0x56 0x57	00000000 00000000 00001000	CSC Coefficient A2. Contains 13-bit A2 coefficient for the A channel. 0x0000 - Default value	
A1[12:0]			R/W
0x57 0x58	00001000 00000000	CSC Coefficient A1. Contains 13-bit A1 coefficient for the A channel. 0x0800 - Default value	
B4[12:0]			R/W
0x59 0x5A	00000000 00000000	CSC Coefficient B4. Contains 13-bitB4 coefficient for the B channel. 0x0000 - Default value	
B3[12:0]			R/W
0x5B 0x5C	00000000 00000001	CSC Coefficient B3. Contains 13-bit B3 coefficient for the B channel. 0x0000 - Default value	
B2[12:0]			R/W
0x5C 0x5D 0x5E	00000001 00000000 00000000	CSC Coefficient B2. Contains 13-bit B2 coefficient for the B channel. 0x0800 - Default value	
B1[12:0]			R/W
0x5E 0x5F	00000000 00000000	CSC Coefficient B1. Contains 13-bit B1 coefficient for the B channel. 0x0000 - Default value	
C4[12:0]			R/W
0x60 0x61	00000000 00000000	CSC Coefficient C4. Contains 13-bit C4 coefficient for the C channel. 0x0000 - Default value	
C3[12:0]			R/W
0x62 0x63	00100000 00000000	CSC Coefficient C3. Contains 13-bit C3 coefficient for the C channel. 0x0800 - Default value	
C2[12:0]			R/W
0x63 0x64 0x65	00000000 00000000 00000000	CSC Coefficient C2. Contains 13-bit C2 coefficient for the C channel. 0x0000 - Default value	
C1[12:0]			R/W
0x65 0x66	00000000 00000000	CSC Coefficient C1. Contains 13-bit C1 coefficient for the C channel. 0x0000 - Default value	
EMB_SYNC_ON_ALL			R/W
0x67	00000000	A control to alter the gain computed by the AGC based on the presence of an embedded synchronization on channels A, B and C. Used only in case of RGB input and RGB output with Color-Controls enabled 0 - Embedded synchronization is present only on the Luma channel (i.e. channel A) 1 - All three input channels have and embedded synchronization	

Reg	Bits	Description	
CSC_COEFF_SEL[3:0]			R/W
0x68	1111 0000	A control to select the mode the CP CSC operates in. 0000 - CP CSC configuration in manual mode 1111 - CP CSC configured in automatic mode xxxx - Reserved	
CP_CHROMA_LOW_EN			R/W
0x68	1111 0 000	Filter Response Control for the 444 to 422 Chroma decimation filter 0 - High bandwidth, sharp transition filter for channels B/C 1 - Soft filter with minimized ringing for channels B/C	
MAN_CP_CSC_EN			R/W
0x69	0000 0 100	A control to manually enable the CP CSC. By default the CP CSC will be automatically enabled in the case that either a color-space conversion or video-adjustments (Hue, Saturation, Contrast, Brightness) is determined to be required due to other I2C settings. If MAN_CP_CSC_EN is set to one the CP CSC is forced into the enabled state. 0 - CP CSC will be automatically enabled if required. For example if either a color-space conversion or video-adjustments (Hue, Saturation, Contrast, Brightness) is determined to be required due to other I2C settings. 1 - Manual override to force CP-CSC to be enabled	
EIA_861_COMPLIANCE			R/W
0x69	0000 0 1 00	A control to implement compliance to the CEA 861 standard for 525p inputs. This bit effects the start of the VBI for the 525p standard only. 0 - The VBI region starts on line 1. 1 - The VBI region starts on line 523. The start of the VBI region is compliant with the 861 specification.	
CLMP_A_MAN			R/W
0x6C	0 0010000	Manual clamping enable for channel A. 0 - Use the digital fine clamp value determined by the on-chip clamp loop 1 - Ignore internal digital fine clamp loop result. Use CLMP_A[11:0]	
CLMP_BC_MAN			R/W
0x6C	0 0 010000	Manual clamping enable for channel B and C. 0 - Use the digital fine clamp value determined by the on-chip clamp loop. 1 - Ignore internal digital fine clamp loop result. use CLMP_B[11:0] for channel B and CLMP_C[11:0] for channel C.	
CLMP_FREEZE			R/W
0x6C	00 0 10000	Stops the digital fine clamp loops for channels A, B and C from updating. 0 - Clamp value updated on every active video line. 1 - Clamp loops are stopped and not updated.	
CLMP_A[11:0]			R/W
0x6C 0x6D	0001 0000 00000000	Manual clamp value for channel A. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_A_MAN is set to 1. To change the CLMP_A[11:0], the register addresses 0x6C and 0x6D must be updated with the desired clamp value written to in this order and with no other I2C access in between. 0x000 - minimum range, - ... 0xFFF - maximum range	
CLMP_B[11:0]			R/W
0x6E 0x6F	00000000 0000 0000	Manual clamp value for channel B. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_BC_MAN is set to 1. To change the CLMP_B[11:0], the register addresses 0x6E and 0x6F must be updated with the desired clamp value written to in this order and with no other I2C access in between. 0x000 - minimum range, - ... 0xFFF - maximum range	
CLMP_C[11:0]			R/W
0x6F 0x70	0000 0000 00000000	Manual clamp value for channel C. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_BC_MAN is set to 1. To change the CLMP_C[11:0], the register addresses 0x6F and 0x70 must be updated with the desired clamp value written to in this order and with no other I2C access in between. 0x000 - minimum range, - ... 0xFFF - maximum range	

Reg	Bits	Description	
AGC_TAR[9:0]			R/W
0x71 0x72	00000000 00000000	Manual AGC Target Value Enable. The register is used to set the target value for horizontal synchronization depth after gain has been applied. The field represents an unsigned value. Manual AGC Target Value. See also description of AGC_TAR_MAN, AGC_FREEZE, AGC_TIM. 0x000 - minimum range, - … 0x3FF - maximum range	
AGC_TAR_MAN			R/W
0x71	00000000	Manual Target Level Enable. 0 - The AGC operates based on a 300 mV or 286 mV horizontal synchronization depth. Use HS_NORM to select between the two. 1 - AGC operates based on AGC_TAR[9:0].	
AGC_FREEZE			R/W
0x71	00000000	AGC Freeze Enable. 0 - The AGC loop is operational 1 - The AGC loop is frozen and not updated further. the last gain value becomes static.	
HS_NORM			R/W
0x71	00000000	Nominal Hsync Depth Selection. 0 - The AGC target scales the video as per 300 mV horizontal synchronization depth 1 - The AGC target scales the video as per 286 mV horizontal synchronization depth	
AGC_TIM[2:0]			R/W
0x71	00000000	AGC Time Constant Selection. 000 - 100 lines 001 - 1 frame 010 - 0.5 sec 011 - 1 sec 100 - 2 sec 101 - 3 sec 110 - 5 sec 111 - 7 sec	
GAIN_MAN			R/W
0x73	00010000	Enables the gain factor to be set by the AGC or manually. 0 - AGC controls the gain for all three channels, 1 - Manual gains are used for all three channels	
AGC_MODE_MAN			R/W
0x73	00010000	A control to set how the gains for all 3 channels is configured 0 - The gain is dependant on the type of input and OP_656_RANGE 1 - Gain operation controlled by GAIN_MAN	
A_GAIN[9:0]			R/W
0x73 0x74	00010000 00000100	A control to set the manual gain value for channel A. This register is an unsigned value in a 2.8 binary format. To change A_GAIN[9:0], the register at addresses 0x73 and 0x74 must be written to in this order with no I2C access in between. 0x000 - Gain of 0 0x100 - Unity Gain 0x3FF - Gain of 3.99	
B_GAIN[9:0]			R/W
0x74 0x75	00000100 00000001	A control to set the manual gain value for channel B. This register stores an unsigned value in a 2.8 binary format. To change A_GAIN[9:0], the register at addresses 0x74 and 0x75 must be written to in this order with no I2C access in between. 0x000 - Gain of 0 0x100 - Unity Gain 0x3FF - Gain of 3.99	
C_GAIN[9:0]			R/W
0x75 0x76	00000001 00000000	A control to set the manual gain value for channel C. This register stores an unsigned value in a 2.8 binary format. To change C_GAIN[9:0], the registers at addresses 0x75 and 0x76 must be written to in sequence with no I2C access in between. 0x000 - Gain of 0 0x100 - Unity Gain 0x3FF - Gain of 3.99	

Reg	Bits	Description	
CP_PREC[1:0]			R/W
0x77	11111111	A control to set the precision of the data output by the CP core for channels A, B and C. 00 - Rounds and truncates data in channels A, B and C to 10-bit precision 01 - Rounds and truncates data in channels A, B and C to 12-bit precision 10 - Rounds and truncates data in channels A, B and C to 8 bit precision 11 - Rounds and truncates data in channels A, B, and C to the precision set in OP_FORMAT_SEL[6:0]	
A_OFFSET[9:0]			R/W
0x77 0x78	11111111 11111111	A control to set the manual offset for channel A. This field stores an unsigned value. To change A_OFFSET[9:0], the register addresses 0x77 and 0x78 must be written to in this order with no I2C access in between. 0x3FF - Auto Offset to Ch A , Any other value - Ch A offset	
B_OFFSET[9:0]			R/W
0x78 0x79	11111111 11111111	A control to set the manual offset for channel B. This field stores an unsigned value. To change B_OFFSET[9:0], the register addresses 0x78 and 0x79 must be written to in this order with no I2C access in between. 0x3FF - Auto Offset to Ch B , Any other value - Ch B offset.	
C_OFFSET[9:0]			R/W
0x79 0x7A	11111111 11111111	A control to set the manual offset for channel C. This field stores an unsigned value. To change C_OFFSET[9:0], the register addresses 0x79 and 0x7A must be written to in this order with no I2C access in between. 0x3FF - Auto Offset to Ch C Any other value - Ch C offset.	
AV_INV_F			R/W
0x7B	00000101	A control to invert the F bit in the AV codes. 0 - Inserts the F bit with default polarity, 1 - Inverts the F bit before inserting it into the AV code	
AV_INV_V			R/W
0x7B	00000101	A control to invert V bit in AV codes. 0 - Do not invert V bit polarity before inserting it into the AV code, 1 - Invert V bit polarity before inserting it into the AV code	
AV_POS_SEL			R/W
0x7B	00000101	A control to select AV codes position 0 - SAV code at HS falling edge and EAV code at HS rising edge. 1 - Uses predetermined (default) positions for AV codes.	
DE_WITH_AVCODE			R/W
0x7B	00000101	A control to insert AV codes in relation to the DE output signal 0 - AV codes locked to default values. DE position can be moved independently of AV codes. 1 - Inserted AV codes moves in relation to DE position change.	
START_HS[9:0]			R/W
0x7C 0x7E	11000000 00000000	A control to shift the position of the leading edge of the HSync output by the CP core. This register stores a signed value in a 2's complement format. START_HS[9:0] is the number of pixel clocks by which the leading edge of the HSync is shifted (e.g. 0x3FF corresponds to a shift of 1 pixel clock away form the active video, 0x005 corresponds to a shift of 5 pixel clocks toward the active video). 0x000 - Default value. 0x000 to 0x1FF - The leading edge of the HSync is shifted toward the active video. 0x200 to 0x3FF - The leading edge of the HSync is shifted away from the active video.	
END_HS[9:0]			R/W
0x7C 0x7D	11000000 00000000	A control to shift the position of the trailing edge of the HSync output by the CP core. This register stores a signed value in a 2's complement format. HS_END[9:0] is the number of pixel clock by which the leading edge of the HSync is shifted (e.g. 0x3FF corresponds to a shift of 1 pixel clock away form the active video, 0x005 corresponds to a shift of 5 pixel clocks toward the active video). 0x000 - Default value. 0x000 to 0x1FF - The trailing edge of the HSync is shifted toward the active video. 0x200 to 0x3FF - The trailing edge of the HSync is shifted away from the active video.	
START_VS[3:0]			R/W
0x7F	00000000	A control to shift the position of the leading edge of the VSync output by the CP core. This register stores a signed value in a 2's complement format. START_VS[3:0] is the number of lines by which the leading edge of the VSync is shifted (e.g. 0x0F corresponds to a shift by 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The leading edge of the VSync is shifted toward the active video. 0x8 to 0xF - The leading edge of the VSync is shifted away from the active video.	

Reg	Bits	Description
END_VS[3:0]		R/W
0x7F	00000000	A control to shift the position of the trailing edge of the VSync output by the CP core. This register stores a signed value in a 2's complement format. SEND_VS[3:0] is the number of lines by which the trailing edge of the VSync is shifted (e.g. 0x0F corresponds to a shift of 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The trailing edge of the VSync is shifted toward the active video. 0x8 to 0xF - The trailing edge of the VSync is shifted away from the active video.
START_FE[3:0]		R/W
0x80	00000000	A control to shift the position of the start of even field edge of the FIELD signal output by the CP core This register stores a signed value in a 2's complement format. START_FE[3:0] the number of lines by which the start of the even fields edge of the FIELD signal is shifted (e.g. 0x0D corresponds to a shift of 3 lines toward the active video, 0x05 corresponds to a shift of 5 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The edge of the FIELD signal corresponding to the start of the even field is shifted toward the active video. 0x8 to 0xF - The trailing of the FIELD signal corresponding to the start of the even field is shifted away from the active video.
START_FO[3:0]		R/W
0x80	00000000	A control to shift the position of the start of odd field edge of the FIELD signal output by the CP core This register stores a signed value in a 2's complement format. START_FO[3:0] the number of lines by which the start of the odd fields edge of the FIELD signal is shifted (e.g. 0x0D corresponds to a shift of 3 lines toward the active video, 0x05 corresponds to a shift of 5 line away from the active video). 0x0 - Default value. 0x0 to 0x7 - The edge of the FIELD signal corresponding to the start of the odd field is shifted toward the active video. 0x8 to 0xF - The trailing of the FIELD signal corresponding to the start of the odd field is shifted away from the active video.
MEAS_WL[1:0]		R/W
0x81	11000000	A control to set the width of the window length used for noise calibration measurements. The unit for this parameter is a pixel clock cycle. Refer to Noise[7:0] and CALIB[10:0]. 00 - Window length is 128 LLC clock cycles, 01 - Window length is 64 LLC clock cycles, 10 - Window length is 32 LLC clock cycles, 11 - Window length is 16 LLC clock cycles,
GR_AV_BL_EN		R/W
0x81	11000000	A control to enable the insertion of data blanking and AV codes for auto-graphics mode. 0 - Data blanking and AV code insertion for auto graphics mode disabled. 1 - Data blanking and AV code insertion for auto graphics mode enabled.
MEAS_WS[11:0]		R/W
0x81 0x82	11000000 00000100	A control to set the start value of the measurement window use for noise and calibration. The unit for this parameter is a pixel clock cycle. Refer to NOISE[7:0] and CALIB[10:0]. A value of 0 positions the start of the window at the trailing edge of the incoming HSync. 0x000 - Start value (in LLC clock cycles) of measurement window. Value of 0 positions window at trailing edge of incoming HSync 0x004 - Default value
ISD_THR[7:0]		R/W
0x83	00000000	A control used to set the threshold used for the ISD measurement. ISD_THR[7:0] stores a 12-bit unsigned value. 0x00 - The threshold is calculated automatically and set to (level of HSync tip) + 0.5 * (HSync depth). >0x01 - The threshold is set to (ISD_THR[7:0] * 8)

Reg	Bits	Description	
CP_GAIN_FILT[3:0]			R/W
0x84	0000**1100**	A control to set the coefficient A of the IIF filter to filter the gain applied to the video signal when the gain is manually set. The value set in this register is effective only when manual gain is enabled. The filter is designed as and IIR filter with a transfer function of the form Y[N]=(1-A)*y[N-1]+A*X[N] 0000 - No filtering, i.e. coefficient A = 1 0001 - Coefficient A = 1/128 lines 0010 - Coefficient A = 1/256 lines 0011 - Coefficient A = 1/512 lines 0100 - Coefficient A = 1/1024 lines 0101 - Coefficient A = 1/2048 lines 0110 - Coefficient A = 1/4096 lines 0111 - Coefficient A = 1/8192 lines 1000 - Coefficient A = 1/16 384 lines 1001 - Coefficient A = 1/32 768 lines 1010 - Coefficient A = 1/65 536 lines 1011 - Coefficient A = 1/131 072 lines All other values - Reserved. Do not use.	
CH1_SSPD_PP_EN			R/W
0x84	0000110**0**	A control to enable sync channel 1 SSPD post processing 0 - Disable post processing of the synchronization signals input to sync channel 1 SSPD 1 - Check for activity on embedded synchronization signal input to sync channel 1 SSPD when it detects activity on HSync CSync and VSync. Activity on the embedded signal input to sync channel 1 SSPD is reported by CH1_RS_ACTIVE. The post processing of the synchronization signal input to sync channel 1 SSPD works only if the timing on the embedded synchronization signal and the timing on the HSync/CSync and VSync signals are the same.	
IFSD_AVG			R/W
0x84	00001100	A control to set the averaging mode used to compute IFSD[8:0] 0 - ISD[8:0] is averaged over 128 lines of video to generate IFSD[8:0] 1 - ISD[8:0] is averaged over 256 lines of video to generate IFSD[8:0]	
CH1_POL_MAN_EN			R/W
0x85	0000011	A control to override for polarity detection by sync channel 1 SSPD. CH1_POL_MAN_EN must be set high for this bit to become active. 0 - Use result from sync channel 1 SSPD polarity auto detection 1 - Manual override: use CH1_POL_VS and CH1_POL_HS	
CH1_POL_VS			R/W
0x85	00000011	A control to override for polarity of VSync by sync channel 1 SSPD. 0 - VSync input to sync channel 1 carries negative polarity signal. 1 - VSync input to sync channel 1 carries positive polarity signal.	
CH1_POL_HSCS			R/W
0x85	00000011	A control to override the polarity of HSync by to sync channel 1 SSPD. CH1_POL_MAN_EN must be set high for this bit to become active. 0 - HSync input to sync channel 1 carries negative polarity signal (HSync or CSync). 1 - HSync input to sync channel 1 carries positive polarity signal (HSync or CSync).	
CH1_SYNC_SRC[1:0]			R/W
0x85	000**00**011	A control to select to synchronization signals processed by sync channel 1 SSPD 00 - Auto detect mode for synchronization source. Use results of auto detection for synchronization signal routing. Result can be read back via CH1_CUR_SYNC[1:0] bits. 01 - Manual setting: separate HSync and VSync to sync channel 1 SSPD 10 - Manual setting: CSync on HSync input to sync channel 1 11 - Manual setting: embedded synchronization signal input to sync channel 1	
CH1_TRIG_SSPD			R/W
0x85	00000**0**11	Trigger synchronization source and polarity detector for sync channel 1 SSPD. A 0 to 1 transition in this bit restarts the auto-sync detection algorithm. This is not a self-clearing bit and must be set to 0 to prepare for next trigger. 0 - Default value - transition 0 to 1 restarts auto-sync detection algorithm 1 - Transition 0 to 1 restarts auto-sync detection algorithm	
CH1_SSPD_CONT			R/W
0x85	0000001**1**	A control to set the synchronization source polarity detection mode for sync channel 1 SSPD. 0 - sync channel 1 SSPD works in one-shot mode (triggered by a 0 to 1 transition on the CH1_TRIG_SSPD bit) 1 - sync channel 1 SSPD works in continuous mode	

Reg	Bits	Description	
DS_OUT			R/W
0x85	0000001<u>1</u>	Digital synchronization output enable. 1 - Output synchronous VSync 0 - Asynchronous VSync	
CH1_TRIG_STDI			R/W
0x86	00001<u>0</u>11	Trigger synchronization source and polarity detector for sync channel 1 STDI. A 0 to 1 transition in this bit restarts the auto-sync detection algorithm. This is not a self-clearing bit and must be set to 0 to prepare for next trigger. 0 - Default value - transition 0 to 1 restarts auto-sync detection algorithm 1 - Transition 0 to 1 restarts auto-sync detection algorithm	
CH1_STDI_CONT			R/W
0x86	0000101<u>1</u>	A control to set the synchronization source polarity detection mode for sync channel 1 SSPD. 0 - sync channel 1 SSPD works in one-shot mode (triggered by a 0 to 1 transition on the CH1_TRIG_SSPD bit) 1 - sync channel 1 SSPD works in continuous mode	
DE_V_START_EVEN[3:0]			R/W
0x88	<u>0000</u>0000	A control to adjust the start position of the VBI region in even field. This register stores a signed value represented in a 2's complement format. The unit of adjustment is one pixel clock. 1000 … 1111 - (-8 lines … -1 line) 0000 - Default value (0 lines) 0001 … 0111 - (1 line … 7 lines)	
DE_V_END_EVEN[3:0]			R/W
0x88	0000<u>0000</u>	A control to adjust the end position of the VBI region in even field. This register stores a signed value represented in a 2's complement format. The unit of adjustment is one pixel clock. 1000 … 1111 - (-8 lines … -1 line) 0000 - Default value (0 lines) 0001 … 0111 - (1 line … 7 lines)	
START_VS_EVEN[3:0]			R/W
0x89	<u>0000</u>0000	A control to shift the position of the leading edge of the VSync output by the CP core. This register stores a signed value in a 2's complement format. START_VS_EVEN[3:0] is the number of lines by which the leading edge of the Vsync is shifted (e.g. 0x0F corresponds to a shift by 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 to 0x7 - The leading edge of the even VSync is shifted toward the active video. 0x8 to 0xF - The leading edge of the even VSync is shifted away from the active video.	
END_VS_EVEN[3:0]			R/W
0x89	0000<u>0000</u>	A control to shift the position of the trailing edge of the VSync output by the CP core. This register stores a signed value in a 2's complement format. END_VS_EVEN[3:0] is the number of lines by which the trailing edge of the Vsync is shifted (e.g. 0x0F corresponds to a shift of 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video). 0x0 to 0x7 - The trailing edge of the even VSync is shifted toward the active video. 0x8 to 0xF - The trailing edge of the even VSync is shifted away from the active video.	
IGNR_CLMP_VS_MAR_END[4:0]			R/W
0x8A	<u>00100</u>000	A control to set the end of the window during which the clamp is ignored. This register stores the unsigned number of pixel clocks between the end position of the window relative to the trailing edge of the VSync. This control should only be used VID_STD[5:0] is set for auto-graphics mode. 0x04 - Default value	
IGNR_CLMP_VS_MAR_START[4:0]			R/W
0x8A 0x8B	0010000<u>0</u> <u>0100</u>0000	A control to set the start of the window during which the clamp is ignored. This register stores the unsigned number of pixel clocks between the start position of the window relative to the leading edge of the VSync. This control should only be used VID_STD[5:0] is set for auto-graphics mode. 0x04 - Default value	
DE_H_START[9:0]			R/W
0x8B 0x8D	0100<u>00</u>00 <u>00000000</u>	A control to vary the leading edge position of the DE signal output by the CP core. This register stores a signed value in a 2's complement format. The unit of DE_H_START[9:0] is one pixel clock. 0x200 - -512 pixels of shift 0x3FF - -1 pixel of shift 0x000 - Default value (no shift) 0x001 - +1 pixel of shift 0x1FF - +511 pixels	

Reg	Bits	Description
DE_H_END[9:0]		R/W
0x8B 0x8C	01000000 00000000	A control to vary the trailing edge position of the DE signal output by the CP core. This register stores a signed value in a 2's complement format. The unit of DE_H_END[9:0] is one pixel clock. 0x200 - -512 pixels of shift 0x3FF - -1 pixel of shift 0x000 - Default value (no shift) 0x001 - +1 pixel of shift 0x1FF - +511 pixels
DE_V_START[3:0]		R/W
0x8E	00000000	A control to vary the start position of the VBI region. This register stores a signed value represented in a 2's complement format. The unit of DE_V_START[9:0] is one line. 1000 - -8 lines of shift 1111 - -1 line of shift 0000 - Default 0001 - +1 line of shift 0111 - +7 lines of shift
DE_V_END[3:0]		R/W
0x8E	00000000	A control to vary the position of the end of the VBI region. This register stores a signed value represented in a 2's complement format. The unit of DE_V_START[9:0] is one line. 1000 - -8 lines of shift 1111 - -1 line of shift 0000 - Default 0001 - +1 line of shift 0111 - +7 lines of shift
CH1_FR_LL[10:0]		R/W
0x8F 0x90	01000000 00000000	Free run line length in number of crystal clock cycles in one line of video for sync channel 1 STDI. This register should only be programmed video standards that are not supported by PRIM_MODE[3:0] and VID_STD[5:0]. 0x000 - Internal free run line length is decoded from PRIM_MODE[3:0] and VID_STD[5:0]. All other values - Number of crystal clocks in the ideal line length. Used to enter or exit free run mode.
INTERLACED		R/W
0x91	01000000	Sets the interlaced/progressive mode of the incoming video processed in CP mode. 0 - The CP core expects video mode is progressive 1 - the CP core expects video mode is interlaced
CP_START_VS[5:0]		R/W
0x9A 0x9B	00000000 00000000	A control to set the position of the start of the VSync output signal in the CP core in Autographic mode only. In the case of an interlaced signal this register adjusts the odd VS signal. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 000000 - Default value
CP_END_VS[5:0]		R/W
0x9B	00000000	A control to set the position of the end of the VSync output signal in the CP core in Autographic mode only. In the case of an interlaced signal this register adjusts the odd VS signal. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 000000 - Default value
CP_START_VS_EVEN[10:0]		R/W
0x9C 0x9D	00000000 00000000	A control to set the position of the start of the even VSync output signal in the CP core in Autographic mode only. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x000 - Default value
CP_END_VS_EVEN[10:0]		R/W
0x9D 0x9E	00000000 00000000	A control to set the position of the end of the even VSync output signal in the CP core in Autographic mode only. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x000 - Default value
CP_START_F_ODD[10:0]		R/W
0x9F 0xA0	00000000 00000000	A control to set the position of the end of the odd field output signal in the CP core in Autographic mode only. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x000 - Default value

Reg	Bits	Description	
CP_START_F_EVEN[10:0]			R/W
0xA0 0xA1	00000000 00000000	A control to set the position of the end of the even field output signal in the CP core in Autographic mode only. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. The value is unsigned. 0x000 - Default value	
CP_START_VBI[11:0]			R/W
0xA5 0xA6	00000000 00000000	Manual value for start of VBI region position (of odd fields in case of interlaced output). This is an unsigned value. It sets the total number of lines at the start of a frame of non-interlaced standard video. It sets the total number of lines at the start of the odd frame of interlaced standard video. Programming of this parameter is optional and should only be performed when the part is set in auto-graphics mode. 0x000 - Default value	
CP_END_VBI[11:0]			R/W
0xA6 0xA7	00000000 00000000	Manual value for end of VBI region position (of odd fields in case of interlaced output). This is an unsigned value. It sets the total number of lines at the end of a frame of non-interlaced standard video. It sets the total number of lines at the end of the odd frame of interlaced standard video. Programming of this parameter is optional and should only be performed when the part is set in auto-graphics mode. 0x000 - Default value	
CP_START_VBI_EVEN[11:0]			R/W
0xA8 0xA9	00000000 00000000	Manual value for start of VBI in even fields. This is an unsigned value. Total number of lines at the start of the even frame of interlaced standard. Programming of this parameter is optional and should only be performed when the part is set in auto-graphics mode. 0x000 - Default value	
CP_END_VBI_EVEN[11:0]			R/W
0xA9 0xAA	00000000 00000000	Manual value for end of VBI region position for even fields. This is an unsigned value. Total number of lines at the end of the even frame of interlaced standard. Programming of this parameter is optional and should only be performed when the part is set in auto graphics mode. 0x000 - Default value	
CP_LCOUNT_MAX[11:0]			R/W
0xAB 0xAC	00000000 00000000	Manual value for total number of lines in a frame expected by the CP core. CP_LCOUNT_MAX[11:0] is an unsigned value. This register is used for manual configuration of the free run feature. The value programmed in this register is used for sync channel 1. The value programmed in this register is used also for sync channel 2 if CH2_FR_FIELD_LENGTH[10:0] set to 0x000. 0x000 - Ideal number of lines per frame is decoded from PRIM_MODE[3:0] and VID_STD[5:0] for sync channel 1. All other values - Use the programmed value as ideal number of lines per frame in free run decision for sync channel 1.	
CH1_STDI_DVALID			R
0xB1	00000000	This bit is set when the measurements performed by sync channel 1 STDI are completed. High level signals validity for CH1_BL, CH1_LCF, CH1_LCVS, CH1_FCL, and CH1_STDI_INTLCD parameters. To prevent false readouts, especially during signal acquisition, CH1_SDTI_DVALID only goes high after four fields with same length are recorded. As a result, STDI measurements can take up to five fields to finish. 0 - Sync channel 1 STDI measurement are not valid 1 - Sync channel 1 STDI measurement are valid	
CH1_STDI_INTLCD			R
0xB1	00000000	Interlaced vs. progressive mode detected by sync channel 1 STDI. The readback from this register is valid if CH1_STDI_DVALID is high. 0 - Indicates a video signal on sync channel 1 with non interlaced timing. 1 - Indicates a signal on sync channel 1 with interlaced timing.	
CH1_BL[13:0]			R
0xB1 0xB2	00000000 00000000	A readback for the Block Length for sync channel 1. Number of crystal clock cycles in a block of eight lines of incoming video. This readback is valid if CH1_STDI_DVALID is high. xxxxxxxxxxxxxx - Readback value	
CH1_LCVS[4:0]			R
0xB3	00000000	A readback for the sync channel 1 Line Count in a VSync. Number of lines in a VSync period measured on sync channel 1. The readback from this field is valid if CH1_STDI_DVALID is high. xxxxx - Readback value	
CH1_LCF[10:0]			R
0xB3 0xB4	00000000 00000000	A readback for the sync channel 1 Line Count in a Field Number of lines between two VSyncs measured on sync channel 1. The readback from this field is valid if CH1_STDI_DVALID is high. xxxxxxxxxxx - Readback value	

Reg	Bits	Description	
CH1_SSPD_DVALID			R
0xB5	0xxxxxxx	CH1_SSPD_DVALID is set to 1 when the read backs from the SSPD section of the synchronization sync channel 1 are valid. This bit is set to 1 after 2^22 crystal clock periods following a reset of the CP section. This bit is set to 0 when the DUT is reset. 0 - Sync channel 1 SSPD results not valid for readback 1 - Sync channel 1 SSPD results valid	
CH1_VS_ACT			R
0xB5	x0xxxxxx	Readback indicating the activity the VSync input to sync channel 1 SSPD 0 - No activity detected on the VSync input to sync channel 1 SSPD 1 - The VSync input to sync channel 1 SSPD carries an active signal	
CH1_CUR_POL_VS			R
0xB5	xx0xxxxx	Readback indicating polarity on the HSync/CSync input to sync channel 1 SSPD 0 - The VSync input to sync channel 1 SSPD has negative polarity signal 1 - The VSync input to sync channel 1 SSPD has positive polarity signal	
CH1_HS_ACT			R
0xB5	xxx0xxxx	Readback indicating activity on the HSync/CSync input to sync channel 1 SSPD 0 - No activity detected on the HSync CSync input to sync channel 1 SSPD 1 - HSync CSync input to sync channel 1 SSPD carries an active signal	
CH1_CUR_POL_HS			R
0xB5	xxxx0xxx	Readback indicating the polarity of the HSync/CSync input to sync channel 1 SSPD 0 - The HSync CSync input to sync channel 1 SSPD has negative polarity 1 - The HSync CSync input to sync channel 1 SSPD has positive polarity	
CH1_RS_ACTIVE			R
0xB5	xxxxx0xx	A readback indicating activity in embedded synchronization signal input to sync channel 1 SSPD. CH1_SSPD_PP_EN must be set to 1 and CH1_SSPD_DVALID must return 1 for this readback to be valid. This is readback is only valid when there is a HSync and VSync signal present. It is not valid to use this bit when only embedded signal is present. The purpose of this bit is to indicate that the user can switch to embedded sync if using HSync and VSync inputs. 0 - Activity detected on the embedded signal input to sync channel 1 SSPD 1 - No activity detected on the embedded signal input to sync channel 1 SSPD	
CH1_CUR_SYNC_SRC[1:0]			R
0xB5	xxxxxx00	Readback of current synchronization source detected by sync channel 1 SSPD. 00 - Not used 01 - Activity detected on HSync and VSync input to sync channel 1 SSPD 10 - CSync detected in the HSync input to sync channel 1 SSPD 11 - Activity detected on embedded synchronization input to sync channel 1 SSPD	
CH1_FCL[12:0]			R
0xB8 0xB9	xxx00000 00000000	A readback for the sync channel 1 Field Count Length Number of crystal clock cycles between successive VSyncs measured by sync channel 1 STDI or in 1/256th of a field. The readback from this field is valid if CH1_STDI_DVALID is high. xxxxxxxxxxxxx - Readback value	
HDMI_FRUN_MODE			R/W
0xBA	xxxxxxx0	A control to configure the free run feature in HDMI mode. 0 - HDMI free run mode 0. The part free runs when the TMDS clock is not detected on the selected HDMI port 1 - HDMI free run mode 1. The CP core free runs when the TMDS clock is not detected on the selected HDMI port or it the video resolution of HDMI stream processed by the part does not match the video resolution programmed in PRIM_MODE[3:0] and VID_STD[5:0].	
HDMI_FRUN_EN			R/W
0xBA	xxxxxxx1	A control to enable free run in HDMI mode. 0 - Disable the free run feature in HDMI mode 1 - Enable the free run feature in HDMI mode	
DPP_BYPASS_EN			R/W
0xBD	xxx1xxxx	Manual control to enable DPP block. 1 - DPP Bypassed 0 - DPP Enabled	
DLY_A			R/W
0xBE	0xxxxxxx	A control to delay the data on channel A by one pixel clock cycle. 1 - Delay the data of channel A by 1 pixel clock cycle 0 - Do not delay the data of channel A	

Reg	Bits	Description	
DLY_B			R/W
0xBE	0**0**000000	A control to delay the data on channel B by one pixel clock cycle. 1 - Delay the data of channel B by 1 pixel clock cycle 0 - Do not delay the data of channel B	
DLY_C			R/W
0xBE	000**0**0000	A control to delay the data on channel C by one pixel clock cycle. 1 - Delay the data of channel C by 1 pixel clock cycle 0 - Do not delay the data of channel C	
HCOUNT_ALIGN_ADJ[4:0]			R/W
0xBE 0xBF	000000**00** **000**10010	Manual adjustment for internally generated hcount offset . This register allows an adjustment of 15 pixels to the left or to the right. The MSB sets the direction (left or right) and the 4 LSBs set the number of pixels to move. This is an unsigned control. 00000 - Default value	
CP_DEF_COL_MAN_VAL			R/W
0xBF	00010**0**10	A control to enable manual selection of the color used when the CP core free runs. 0 - Uses default color blue 1 - Outputs default colors as given in CP_DEF_COL_CHA, CP_DEF_COL_B and CP_DEF_COL_C	
CP_DEF_COL_AUTO			R/W
0xBF	000100**1**0	A control to enable the insertion of default color when the CP free runs. 0 - Disable automatic insertion of default color 1 - Output default colors when the CP free runs	
CP_FORCE_FREERUN			R/W
0xBF	0001001**0**	A control to force the CP to free run. 0 - Do not force the CP core free run. 1 - Force the CP core to free run.	
DEF_COL_CHA[7:0]			R/W
0xC0	**00000000**	A control the set the default color for channel A. To be used if CP_DEF_COL_MAN_VAL is 1. 0x00 - Default value	
DEF_COL_CHB[7:0]			R/W
0xC1	**00000000**	A control to set the default color for channel B. To be used if CP_DEF_COL_MAN_VAL is 1 0x00 - Default value	
DEF_COL_CHC[7:0]			R/W
0xC2	**00000000**	A control to set the default color for channel C. To be used if CP_DEF_COL_MAN_VAL is 1 0x00 - Default value	
CLAMP_AVG_FCTR[1:0]			R/W
0xC5	**10**010001	A control to set the coefficient A of the IIR filter used for auto clamp mode. The function transfer is Y[N]=(1-A)*Y[N-1]+A*X[N] 00 - No filtering, A=1 01 - The clamp is averaged over 8 lines. A=1/8 10 - The clamp is averaged over 16 lines. A=1/16 11 - The clamp is averaged over 32 lines. A=1/32	
CP_ANVC_POS_START[12:0]			R/W
0xC6 0xC9 0xCA	**00000000** **0**0101100 **0000**0000	Start of window for Analog Voltage Clamp Measurement (New Clamping Scheme). Unsigned 0x0000 - Default value	
CP_ANVC_POS_DURATION[7:0]			R/W
0xC7	**00000000**	Duration of the window for Analog Voltage Clamp Measurement (New Clamping Scheme). Unsigned 0x0000 - Default value	
CP_DFC_POS_START[12:0]			R/W
0xC8 0xC9 0xCA	**00000000** 0**0**101100 0000**0000**	Start of window for Digital Fine Clamp Measurement (New Clamping Scheme). Unsigned 0x0000 - Default value	
SWAP_SPLIT_AV			R/W
0xC9	00101**1**00	A control to swap the Luma and Chroma AV codes in DDR modes 0 - Swap the Luma and Chroma AV codes in DDR mode 1 - Do not swap the Luma and Chroma AV codes in DDR mode	

Reg	Bits	Description
DIS_AUTO_PARAM_BUFF		R/W
0xC9	0010110<u>0</u>	A control to disable the buffering of the timing parameters used for free run in HDMI mode. 0 - Buffer the last measured parameters in HDMI mode used to determine video resolution the part free runs into. 1 - Disable the buffering of measured parameters in HDMI mode. Free run standard determined by PRIM_MODE[3:0], VID_STD[5:0] and V_FREQ[2:0]
AUTO_SL_FILTER_FREEZE_EN		R/W
0xCB	01<u>1</u>00000	This bit determines if the internally generated parameter for the position of the HSync trailing edge is updated during the VBI region. This control is only intended for auto-graphics mode. It is recommended to leave AUTO_SL_FILTER_FREEZE_EN to default. Unless AUTO_SL_FILTER_FREEZE_EN is left to default, the part may generate an incorrect HSync trailing edge position parameter if the input synchronization is embedded and has serration pulses 0 - Do not freeze the trailing edge position of the HSync during the VBI region. 1 - Freeze the trailing edge position of the HSync during the VBI region.
HDMI_CP_LOCK_THRESHOLD[1:0]		R/W
0xCB	01100<u>00</u>	Locking time of filter used for buffering of timing parameters in HDMI mode. 00 - Slowest locking time 01 - Medium locking time 10 - Fastest locking time 11 - Fixed step size of 0.5 pixel
PW_WIN_MAN		R/W
0xDA	000000<u>0</u>	A control to configure the peak white window 0 - Use active window generated for the peak white measurement 1 - Use manual peak white window specified
PW_SHOW_WIN		R/W
0xDA	0000000<u>0</u>	A control to show the peak white window 0 - Do not show the peak white window 1 - Show peak white window
PW_VB[7:0]		R/W
0xDB	<u>00011001</u>	Value for beginning of Peak White window in a field. This register stores an unsigned value. 0x19 - Default value
PW_VL[7:0]		R/W
0xDC	<u>01100100</u>	Value for end of Peak White window in a field. This register stores an unsigned value. 0x64 - Default value
PW_HB[11:0]		R/W
0xDD 0xDE	<u>00010010</u> <u>1100</u>0101	Value for beginning of Peak White window in a line. This register stores an unsigned value. 0x12C - Default value
PW_HL[11:0]		R/W
0xDE 0xDF	1100<u>0101</u> <u>01111000</u>	Value for end of Peak White window in a line. This register stores an unsigned value. 0x578 - Default value
HDMI_CP_AUTOPARM_LOCKED		R
0xE0	0<u>0</u>000000	A readback to report the lock status of the parameter buffering in HDMI mode 0 - The parameter buffering block has not lock to the synchronization signal from the HDMI core. 1 - The parameter buffering block has lock to the synchronization signal from the HDMI core.
HDMI_AUTOPARM_STS[1:0]		R
0xE0	00<u>00</u>0000	CP status for HDMI mode 00 - The CP is free running with according to timing parameters programmed in PRIM_MODE and VID_STD 01 - The timing buffer filter has locked to the HDMI input 10 - The CP is free running according to the HDMI buffered parameters 11 - Reserved
CP_AGC_GAIN[9:0]		R
0xE0 0xE1	000000<u>00</u> <u>00000000</u>	A readback value of the gain used gain on the data of channel A. The value stored in this register has is in a 1.9 binary format and composed of one integer and nine fractional bits. xxxxxxxxxx - Readback value of the gain
NOISE[7:0]		R
0xE2	<u>00000000</u>	A readback for the noise value measured on the Luma channel (i.e. channel A). This register provides an unsigned value representing the difference between the maximum and minimum value measured during the window configured by MEAS_WS[11:0] and MEAS_WL[1:0]. xxxxxxxx - Readback value

Reg	Bits	Description	
CALIB[10:0]			R
0xE3 0xE6	000000000 00000000	A readback for the calibration value measured on the Luma channel (i.e. channel A). This register provides a signed value representing the average level over the extent of the window configured by MEAS_WS and MEAS_WL. xxxxxxxxxx - Readback value	
IFSD[8:0]			R
0xE3 0xE5	000000000 00000000	A readback for the average value of the ISD measurement over 128 or 256 lines. The number of lines used to computes IFSD[8:0] is set in IFSD_AVG. xxxxxxxxx - Readback value	
ISD[8:0]			R
0xE3 0xE4	000000000 00000000	A readback for representing the area of the of HSync that falls below the slicing threshold set by ISD_THR[7:0]. A high values indicates robust locking. xxxxxxxxx - Readback value	
HSD_CHC[9:0]			R
0xE7 0xEA	000000000 00000000	A readback for the measured value of the HSync depth on channel C before the gain multiplier. The value is presented in 1.9 binary format. xxxxxxxxxx - Readback for measured value of the HSync depth on channel C	
HSD_CHB[9:0]			R
0xE7 0xE9	000000000 00000000	A readback for the measured value of the HSync depth on channel B before the gain multiplier. The value is presented in 1.9 binary format. xxxxxxxxxx - Readback for measured value of the HSync depth on channel B	
HSD_CHA[9:0]			R
0xE7 0xE8	000000000 00000000	A readback for the measured value of the HSync depth on channel A before the gain multiplier. The value is presented in 1.9 binary format. xxxxxxxxxx - Readback for measured value of the HSync depth on channel A	
HSD_FB[11:0]			R
0xEB 0xEC	000000000 00000000	A readback for the measured value of HSync depth on channel A, after gain multiplier, for external feedback loop. The value is presented in twos complement form. This means that only a standard adder is needed to subtract the actual HSync depth (as per HSD_FB) from a nominal value, as the HSD_FB value is already in negative format. xxxxxxxxxxxx - Readback value	
PKV_CHA[9:0]			R
0xED 0xEE	000000000 00000000	Maximum signal level measured during the active video on channel A. xxxxxxxxxx - Readback value	
PKV_CHB[9:0]			R
0xED 0xEF	000000000 00000000	Maximum signal level measured during the active video on channel B. xxxxxxxxxx - Readback value	
PKV_CHC[9:0]			R
0xED 0xF0	000000000 00000000	Maximum signal level measured during the active video on channel C. xxxxxxxxxx - Readback value	
CH1_FL_FR_THRESHOLD[2:0]			R/W
0xF3	110101000	Threshold for difference between input video field length and internally stored standard to enter and exit freerun. 000 - Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines. 001 - Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines. 010 - Minimum difference to switch into free run is 10 lines. Maximum difference to switch out of free run is 7 lines. 011 - Minimum difference to switch into free run is 4 lines. Maximum difference to switch out of free run is 3 lines. 100 - Minimum difference to switch into free run is 51 lines. Maximum difference to switch out of free run is 46 lines. 101 - Minimum difference to switch into free run is 69 lines. Maximum difference to switch out of free run is 63 lines. 110 - Minimum difference to switch into free run is 134 lines. Maximum difference to switch out of free run is 127 lines. 111 - Minimum difference to switch into free run is 263 lines. Maximum difference to switch out of free run is 255 lines.	

Reg	Bits	Description	
CH1_F_RUN_THR[2:0]			R/W
0xF3	11010100	Free run threshold select for sync channel 1. Determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and compared to an internally stored parameter. The magnitude of the difference decides whether or not sync channel 1 will enter free run mode. 000 - Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1. 001 - Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200. 010 - Minimum difference to switch into free run is 128. Maximum difference to switch out of free run is 112. 011 - Minimum difference to switch into free run is 64. Maximum difference to switch out of free run is 48. 100 - Minimum difference to switch into free run is 32. Maximum difference to switch out of free run is 24. 101 - Minimum difference to switch into free run is 16. Maximum difference to switch out of free run is 12. 110 - Minimum difference to switch into free run is 8. Maximum difference to switch out of free run is 6. 111 - Minimum difference to switch into free run is 4. Maximum difference to switch out of free run is 3.	
CSC_COEFF_SEL_RB[3:0]			R
0xF4	00000000	Readback of the CP CSC conversion when configured in automatic mode 0000 - CSC is bypassed 0001 - YPbPr 601 to RGB 0011 - YPbPr 709 to RGB 0101 - RGB to YPbPr 601 0111 - RGB to YPbPr 709 1001 - YPbPr 709 to YPbPr 601 1010 - YPbPr 601 to YPbPr 709 1111 - CSC in manual mode xxxx - Reserved	
WD_TIMER_DIS			R/W
0xF5	00000000	Disable watchdog timer. The watchdog timer is used for generating pulses in the absence of frame start detection pulse when parameters like PLL_DIV_RATIO are to be updated on VSync 0 - Enable watchdog timer 1 - Disable watchdog timer	
DIG_SYNC_DEGLITCH_REDUCE			R/W
0xF5	00000000	A control to configure the deglitch filters that processes synchronization signal before there are input to the SSPD section. The value set in this register is effective if DIG_SYNC_DEGLITCH_REDUCE_MAN is set to 1. 1 - Remove 2 XTAL clock wide glitches synchronization signals input to the SSPD sections 0 - Remove 5 XTAL clock wide glitches from synchronization signals input to the SSPD sections	
DIG_SYNC_DEGLITCH_REDUCE_MAN			R/W
0xF5	00000000	A control to manually configure the deglitch filters that process synchronization signals input to the SSPD sections. 1 - Manual Configuration. The deglitch filters are configured via DIG_SYNC_DEGLITCH_REDUCE. 0 - Automatic configuration. The deglitch filters remove 5 XTAL clock wide glitches from the synchronization signals input to the SSPD section.	
BYPASS_STDI1_LOCKING			R/W
0xF5	00000000	Bypass STDI locking for sync channel 1 0 - Update CH1_BL, CH1_LCF and CH1_LCVS only the sync channel 1 STDI locks and CH1_STDI_DVALID is set to 1 1 - Update CH1_BL, CH1_LCF,CH1_LCVS from the sync channel 1 STDI as they are measured	
BYPASS_STDI2_LOCKING			R/W
0xF5	00000000	Bypass STDI locking for sync channel 2 0 - Update CH2_BL, CH2_LCF and CH2_LCVS only the sync channel 2 STDI locks and CH2_STDI_DVALID is set to 1 1 - Update CH2_BL, CH2_LCF,CH2_LCVS from the sync channel 2 STDI as they are measured	
MV_PS_DET			R
0xFF	00000000	Macrovision pseudo pulses detection status. 0 - No Macrovision pseudo synchronization pulses detected. 1 - Detected Macrovision Pseudo Synchronization Pulses	
MV_AGC_DET			R
0xFF	00000000	Macrovision AGC pulses detection status 0 - the CP has not detected Macrovision AGC pulses 1 - the CP has detected Macrovision AGC Pulses	
CP_FREE_RUN			R
0xFF	00000000	Component processor freerun status 0 - The CP is not free running 1 - The CP is free running	

2.3 VDP MAP

Reg	Bits	Description	
VDP_CGMS_TYPEB_DATA[7:0]			R
0x3C	00000000	Byte 1 of Decoded CGMS Type B data xxxxxxxx - Byte 1 of Decoded CGMS Type B data	
VDP_CGMS_TYPEB_DATA[15:8]			R
0x3D	00000000	Byte 2 of Decoded CGMS Type B data xxxxxxxx - Byte 2 of Decoded CGMS Type B data	
VDP_CGMS_TYPEB_DATA_3[23:16]			R
0x3E	00000000	Byte 3 of Decoded CGMS Type B data xxxxxxxx - Byte 3 of Decoded CGMS Type B data	
VDP_CGMS_TYPEB_DATA_4[31:24]			R
0x3F	00000000	Byte 4 of Decoded CGMS Type B data xxxxxxxx - Byte 4 of Decoded CGMS Type B data	
VDP_STATUS_TTXT			R
0x40	0xxxxxxx	Teletext Detection Status Bit 0 - Teletext not detected 1 - Teletext detected	
VDP_STATUS_VITC			R
0x40	x0xxxxxx	VITC Detection Status Bit 0 - VITC data not detected 1 - VITC data detected	
VDP_STATUS_GEMS_TYPE			R
0x40	xx0xxxxx	Gemstar Type Status Bit 0 - Gemstar 1X detected 1 - Gemstar 2X detected	
VDP_STATUS_GS_VPS_PDC_UTC_CGMSTB			R
0x40	xxx0xxxx	Gemstar, VPS, PDC, UTC, CGMS Type B Data Detection Status Bit 0 - Gemstar, VPS, PDC, UTC, CGMS Type B data not detected. 1 - Gemstar, VPS, PDC, UTC, CGMS Type B data detected.	
VDP_STATUS_FAST_I2C			R
0x40	xxxx0xxx	Status of data availability in fast I2C regs 0 - Data is not available since last fast I2C read 1 - Data is available since last fast I2C read	
VDP_STATUS_WSS_CGMS			R
0x40	xxxxx0xx	WSS or CGMS Type A Data Detection Status Bit 0 - WSS or CGMS Type A data not detected. 1 - WSS or CGMS Type A data detected.	
VDP_STATUS_CCAP_EVEN_FIELD			R
0x40	xxxxxx0x	Closed Caption data in even field Status Bit 0 - Closed Caption data not detected in the even field. 1 - Closed Caption data detected in the even field.	
VDP_STATUS_CCAP			R
0x40	xxxxxxx0	Closed Caption Data Detection Status Bit 0 - Closed Caption data not detected 1 - Closed Caption data detected	
VDP_CCAP_DATA[7:0]			R
0x41	00000000	Byte 1 of Decoded Closed Caption data xxxxxxxx - Byte 1 of Decoded Closed Caption data.	
VDP_CCAP_DATA[15:8]			R
0x42	00000000	Byte 2 of Decoded Closed Caption data xxxxxxxx - Byte 2 of Decoded Closed Caption data.	

Reg	Bits	Description	
VDP_CGMS_WSS_DATA[23:0]			R
0x43 0x44 0x45	00000000 00000000 00000000	Decoded data for CGMS Type A and WSS VDP_CGMS_WSS_DATA[23:0] - Decoded CGMS[23:0] data. VDP_CGMS_WSS_DATA[13:0] = Decoded WSS[13:0] data.	
VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[95:0]			R
0x47 0x48 0x49 0x4A 0x4B 0x4C 0x4D 0x4E 0x4F 0x50 0x51 0x52	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000	Decoded Gemstar, PDC, VPS, UTC, CGMS Type B data block readback	
VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[103:96]			R
0x53	00000000	Decoded Gemstar or PDC or VPS or UTC or CGMS Type B data readback xxxxxxxx - Readback value	
VDP_VITC_DATA[71:0]			R
0x55 0x56 0x57 0x58 0x59 0x5A 0x5B 0x5C 0x5D	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000	Decoded VITC data readback	
VDP_VITC_CALC_CRC[7:0]			R
0x5E	00000000	Calculated CRC value for decoded VITC data. xxxxxxxx - Readback value	
EN_FC_WINDOW_AFTER_CRI_DET			R/W
0x60	00001000	Control to select between clock run in detection methods. Scheme 1 specifies a large timing window in which color burst, CRI, and FC must be accommodated. Scheme 2 specifies a timing window for framing code detection only. This is checked after CRI is detected. 1 - Default value	
VDP_TTXT_TYPE_MAN_EN			R/W
0x60	00001000	Enable for manual programming of Teletext decoding 0 - Manual programming of Teletext disabled 1 - Manual programming of Teletext enabled	
VDP_TTXT_TYPE[1:0]			R/W
0x60	00001000	Teletext Type Detected. These bits are functional only if VDP_TTXT_TYPE_MAN_EN is set to 1. 00 - ITU_BT.653-625/50-A - for PAL 01 - ITU_BT.653-625/50-B(WST) - for PAL; ITU_BT.653-525/60-B - for NTSC 10 - ITU_BT.653-625/50-C(WST) - for PAL; ITU_BT.653-525/60-C or EIA516(NABTS) - for NTSC 11 - ITU_BT.653-625/50-D - for PAL; ITU_BT.653-525/60-D - for NTSC	
VDP_CP_CLMP_AVG			R/W
0x61	00011000	Control to set the amount of samples taken to calculate clamp levels 0 - 16 Samples are taken for averaging 1 - 32 Samples are taken for averaging	
NOISE_CLK_DISABLE			R/W
0x61	00011000	Control for noise clock feature for Clock Run In (CRI) detection 0 - Enables noise clock feature for CRI detection 1 - Disables noise clock feature for CRI detection	
AUTO_DETECT_GEM			R/W
0x61	00011000	Control for autodetection of the Gemstar type. 0 - Disables autodetection of Gemstar type 1 - Enables autodetection of Gemstar type	

Reg	Bits	Description	
VITC_STRIP_SYNC_DISABLE			R/W
0x61	0001100	Control for sync stripping on the VITC input 0 - Disables stripping of 10 syncs from the VITC input signal 1 - Enables stripping of 10 syncs from the VITC input signal	
BIPHASE_DECODE_DISABLE			R/W
0x61	00011000	A control for biphase decoding of incoming VPS or WSS signal 0 - Enables biphase decoding of incoming VPS or WSS signal 1 - Disables biphase decoding of incoming VPS or WSS signal	
ADF_EN			R/W
0x62	00010101	Controls insertion of VBI decoded data into the 656 datastream as ancillary data 0 - VBI decoded data not inserted into ancillary 656 stream 1 - VBI decoded data inserted into ancillary 656 stream	
ADF_MODE[1:0]			R/W
0x62	00010101	Control to set ADF mode for ancillary data 00 - Nibble mode 01 - Byte mode, no code restrictions 10 = Byte mode, but 0x00 and 0xFF prevented (0x00 - 0x01) (0xFF->0xFE) 11 - Reserved	
ADF_DID[4:0]			R/W
0x62	00010101	Control to specify the value of the DID sent in the ancillary stream with VBI decoded data xxxxx - User specified DID sent in ancillary stream with VDP decoded data 10101 - Default	
TOGGLE_ADF			R/W
0x63	00101010	Control to specify how the ancillary data is placed in the luma and chroma datastreams 0 - Ancillary data packet is spread across the Y and C data streams 1 - Ancillary data packet is duplicated across the Y and C data streams	
ADF_SDID[5:0]			R/W
0x63	00101010	Control to specify the value of the SDID sent in the ancillary stream with VBI decoded data 0x2A - Default value	
VDP_MAN_LINE_1_21[7:0]			R/W
0x64	00000000	Configuration Register for manual VDP control for lines 1 and 21	
VDP_MAN_LINE_2_22[7:0]			R/W
0x65	00000000	Configuration Register for manual VDP control for lines 2 and 22	
VDP_MAN_LINE_3_23[7:0]			R/W
0x66	00000000	Configuration Register for manual VDP control for line 3 and 23	
VDP_MAN_LINE_4_24[7:0]			R/W
0x67	00000000	Configuration Register for manual VDP control for line 4 and 24	
VDP_MAN_LINE_5_25[7:0]			R/W
0x68	00000000	Configuration Register for manual VDP control for line 5 and 25	
VDP_MAN_LINE_6_26[7:0]			R/W
0x69	00000000	Configuration Register for manual VDP control for line 6 and 26	
VDP_MAN_LINE_7_27[7:0]			R/W
0x6A	00000000	Configuration Register for manual VDP control for line 7 and 27	
VDP_MAN_LINE_8_28[7:0]			R/W
0x6B	00000000	Configuration Register for manual VDP control for line 8 to 28	
VDP_MAN_LINE_9_29[7:0]			R/W
0x6C	00000000	Configuration Register for manual VDP control line 9 and 29	
VDP_MAN_LINE_10_30[7:0]			R/W
0x6D	00000000	Configuration Register for manual VDP control for line 10 and 30	

Reg	Bits	Description	
VDP_MAN_LINE_11_31[7:0]			R/W
0x6E	00000000	Configuration Register for manual VDP control for line 11 and 31	
VDP_MAN_LINE_12_32[7:0]			R/W
0x6F	00000000	Configuration Register for manual VDP control for line 12 and 32	
VDP_MAN_LINE_13_33[7:0]			R/W
0x70	00000000	Configuration Register for manual VDP control for line 13 and 33	
VDP_MAN_LINE_14_34[7:0]			R/W
0x71	00000000	Configuration Register for manual VDP control for line 14 and 34	
VDP_MAN_LINE_15_35[7:0]			R/W
0x72	00000000	Configuration Register for manual VDP control for line 15 and 35	
VDP_MAN_LINE_16_36[7:0]			R/W
0x73	00000000	Configuration Register for manual VDP control for line 16 and 36	
VDP_MAN_LINE_17_37[7:0]			R/W
0x74	00000000	Configuration Register for manual VDP control for line 17 and 37	
VDP_MAN_LINE_18_38[7:0]			R/W
0x75	00000000	Configuration Register for manual VDP control for line 18 and 38	
VDP_MAN_LINE_19_39[7:0]			R/W
0x76	00000000	Configuration Register for manual VDP control for line 19 and 38	
VDP_MAN_LINE_20_40[7:0]			R/W
0x77	00000000	Configuration Register for manual VDP control for line 20 and 40	
STATUS_CLEAR_TTXT			SC
0x78	00000000	Teletext data status clear. Refreshes the teletext status registers 0 - Do not refresh the Teletext status registers 1 - Refresh the Teletext status registers	
STATUS_CLEAR_VITC			SC
0x78	00000000	VITC data status clear. Refreshes the VITC status register 0 - Do not refresh the VITC status registers 1 - Refresh the VITC status registers	
STATUS_CLEAR_GEMS_VPS			SC
0x78	00000000	Gemstar or VPS data status clear. Refreshes the Gemstar and VPS status registers 0 - Do not refresh the VPS status registers 1 - Refresh the VPS readback registers	
VDP_STATUS_CLEAR_FAST_I2C			SC
0x78	00000000	Clears fast I2C status bit (VDP Map 0x40 [3]) 1 - Clears status_fast_i2c bit	
STATUS_CLEAR_WSS_CGMS			SC
0x78	00000000	WSS or CGMS data status clear. Refreshes the WSS and CGMS readback registers 0 - Do not refresh the WSS and CGMS readback registers 1 - Refresh the WSS and CGMS readback registers	
STATUS_CLEAR_CCAP			SC
0x78	00000000	Closed Caption data status clear. Refreshes the CCAP status register 0 - Do not refresh the CCAP status registers 1 - Refresh the CCAP status registers	
LOW_DATA_STD_FILTER_EN			R/W
0x98	10001000	Control for low-data rate filter 0 - Disables filter for low data rate 1 - Enables filter for low data rate	

Reg	Bits	Description	
ADAP1_SL_CONFIG_EN			R/W
0x98	10<u>0</u>01000	Control for duty-cycle based slicer 0 - Disables duty-cycle based slicer calculator 1 - Enables duty-cycle based slicer calculator	
TTX_SEL			R/W
0x98	1000<u>1</u>000	Control for serial Teletext data output 0 - Disables Teletext serial data out enable 1 - Enables Teletext serial data out enable	
ADAP2_SL_CONFIG_EN			R/W
0x98	1000<u>1</u>000	Peak tracking slicer control 0 - Disables peak tracking slicer 1 - Enables peak tracking slicer	
ADAP2_TTXT_STD_EN			R/W
0x99	<u>1</u>1011101	A control to enable standard adaptive slicing for Teletext. 0 - Do not enable Teletext standard 1 - Enable Teletext standard	
ADAP2_VITC_STD_EN			R/W
0x99	1<u>1</u>011101	A control to enable standard adaptive slicing for VITC 0 - Do not enable VITC standard. 1 - Enable VITC standard.	
ADAP2_GEMS_STD_EN			R/W
0x99	11<u>1</u>11101	A control to enable standard adaptive slicing for Gemstar. 0 - Do not enable GEMSTAR-1x, GEMSTAR-2x standard 1 - Enable GEMSTAR-1x,GEMSTAR-2x standard	
ADAP2_VPS_STD_EN			R/W
0x99	1101<u>1</u>101	A control to enable standard adaptive slicing for VPS. 0 - Do not enable VPS standard 1 - Enables VPS standard	
ADAP2_WSS_CGMS_STD_EN			R/W
0x99	11011<u>1</u>01	A control to enable standard adaptive slicing for CGMS and WSS. 0 - WSS-CGMS standard not enabled 1 - Enables WSS-CGMS standard	
ADAP2_CCAP_STD_EN			R/W
0x99	1101110<u>1</u>	A control to enable standard adaptive slicing for Closed captioning. 0 - Do not enable CCAP standard 1 - Enable CCAP standard	
GS_VPS_PDC_UTC_CB_CHANGE			R/W
0x9C	00<u>1</u>00000	A control to allow content based updates of VPS, PDC and UTC data. 0 - Disable content based update of VPS, PDC, UTC data 1 - Enables content based update of UTC, PDC, UTC data	
WSS_CGMS_CB_CHANGE			R/W
0x9C	001<u>0</u>0000	A control to allow content based updates of WSS and CGMS Type A data. 0 - Disable content based update of WSS, CGMS Type A data 1 - Enables content based update of WSS, CGMS Type A data	
RAW_STATUS_ENABLE			R/W
0x9C	0010<u>0</u>000	0 - Disable raw status and data 1 - Enable raw status and data	
GS_VPS_PDC_UTC_CGMSTB[2:0]			R/W
0x9C	00100<u>000</u>	The readback registers for VPS, PDC, UTC and CGMS Type B are shared. These control bits identify which type of data is to be written to the shared registers. 000 - Gemstar 1x/2x 001 - VPS 010 - PDC 011 - UTC 100 - CGMS type B 101 - Reserved 110 - Reserved 111 - Reserved	

Reg	Bits	Description	
SLICE_CORRECTOR_EN			R/W
0x9D	000000<u>1</u>0	A control for slice correction. This feature is designed to improve handling of non-standard data. 0 - Disable slice corrector feature 1 - Enables slice corrector feature.	
ADAP2_VPS_CTB_FAST_LEARN_EN			R/W
0x9E	0000<u>0</u>000	0 - Disables slice-level calculation using fast-learn approach for VPS and CGMS TYPE B data standard 1 - Enables slice-level calculation using fast-learn approach for VPS and CGMS TYPE B data standard	
VDP_USE_PREDEF_FREQ			R/W
0xA5	1<u>0</u>010000	If the video standard is not correctly identified setting this bit forces a pre defined bit frequency for the PAL standard. 0 - Use bit frequency sent by VDP_PARM 1 - Use predefined bit frequency (PAL, XTAL 28MHz)	
VDP_CRI_TOLERANCE			R/W
0xA5	10<u>0</u>10000	Set this bit to allow tolerance in CRI detection. 0 - No tolerance 1 - Allow 1 bit tolerance in CRI detection	
VDP_FRM_CODE_TOLERANCE			R/W
0xA5	100<u>1</u>0000	Deassert this bit to remove tolerance in Framing Code detection. 0 - No tolerance 1 - Allow 1 bit tolerance in framing code detection	
VDP_CRI_8BIT			R/W
0xA5	1001<u>0</u>000	Sets the number of CRI bits that must be detected for a robust detection. 0 - Search for 6 bits of CRI 1 - Search for 8 bits	
VDP_INVERT_EVEN_FIELD			R/W
0xA6	0000<u>0</u>000	This bits allows the user to control the even_field signal polarity, as seen by the VDP. 0 - Use default even field polarity 1 - Invert even field polarity	
VDP_MANUAL_TTXC			R/W
0xA8	0<u>0</u>001000	This bit allows the user to force the VDP block to try and detect teletext type C. 0 - Try to detect only the type of ttxt which VDP_PARM decides 1 - Try to detect TTX type C even when TTX_TYPE given out by VDP_PARM is TTX type B	
VDP_CRI_MAG_TRESH[7:0]			R/W
0xAC	<u>11001000</u>	The magnitude of CRI peaks must be more than this threshold to be detected. 0x00 - Minimum Threshold 0xC8 - Default Threshold 0xFF - Maximum Threshold	
VDP_FAST_REG_CONF_CUS2			R/W
0xC0	<u>0</u>0000000	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_REG_CONF_CUST			R/W
0xC0	0<u>0</u>000000	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_REG_CONF_CCAP			R/W
0xC0	00<u>0</u>00000	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_REG_CONF_GEM1X_2X			R/W
0xC0	000<u>0</u>0000	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_REG_CONF_CGMS_WSS			R/W
0xC0	0000<u>0</u>000	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_REG_CONF_VITC			R/W
0xC0	00000<u>0</u>00	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_REG_CONF_VPS_CGMSTB			R/W
0xC0	000000<u>0</u>0	Selects VBI data that is available through I2C register 0 - Default value	

Reg	Bits	Description	
VDP_FAST_REG_CONF_TTXT			R/W
0xC0	0000000<u>0</u>	Selects VBI data that is available through I2C register 0 - Default value	
VDP_FAST_VBI_STD[3:0]			R
0xC2	0000<u>0000</u>	Readback of the VBI standard in the fast I2C registers 0001 - Teletext 0010 - VPS 0011 - VITC 0100 - WSS / CGMS Type A 0101 - Gemstar 1X 0110 - Gemstar 2X 0111 - CCAP 1000 - CGMS Type B 1001 - Reserved 1010 - Reserved 1011 - Reserved 1100 - Reserved 1101 - Custom 1 1110 - Custom 2 1111 - Reserved	
VDP_FAST_PACKET_SIZE[7:0]			R
0xC3	<u>00000000</u>	Readback of the number of bytes contained in the fast I2C registers xxxxxxxx - Number of bytes contained in the fast I2C registers	
VDP_FAST_REG00[7:0]			R
0xC4	<u>00000000</u>	Fast I2C data byte 0	
VDP_FAST_REG01[7:0]			R
0xC5	<u>00000000</u>	Fast I2C data byte 1	
VDP_FAST_REG02[7:0]			R
0xC6	<u>00000000</u>	Fast I2C data byte 2	
VDP_FAST_REG03[7:0]			R
0xC7	<u>00000000</u>	Fast I2C data byte 3	
VDP_FAST_REG04[7:0]			R
0xC8	<u>00000000</u>	Fast I2C data byte 4	
VDP_FAST_REG05[7:0]			R
0xC9	<u>00000000</u>	Fast I2C data byte 5	
VDP_FAST_REG06[7:0]			R
0xCA	<u>00000000</u>	Fast I2C data byte 6	
VDP_FAST_REG07[7:0]			R
0xCB	<u>00000000</u>	Fast I2C data byte 7	
VDP_FAST_REG08[7:0]			R
0xCC	<u>00000000</u>	Fast I2C data byte 8	
VDP_FAST_REG09[7:0]			R
0xCD	<u>00000000</u>	Fast I2C data byte 9	
VDP_FAST_REG10[7:0]			R
0xCE	<u>00000000</u>	Fast I2C data byte 10	
VDP_FAST_REG11[7:0]			R
0xCF	<u>00000000</u>	Fast I2C data byte 11	
VDP_FAST_REG12[7:0]			R
0xD0	<u>00000000</u>	Fast I2C data byte 12	

Reg	Bits	Description	
VDP_FAST_REG13[7:0]			R
0xD1	00000000	Fast I2C data byte 13	
VDP_FAST_REG14[7:0]			R
0xD2	00000000	Fast I2C data byte 14	
VDP_FAST_REG15[7:0]			R
0xD3	00000000	Fast I2C data byte 15	
VDP_FAST_REG16[7:0]			R
0xD4	00000000	Fast I2C data byte 16	
VDP_FAST_REG17[7:0]			R
0xD5	00000000	Fast I2C data byte 17	
VDP_FAST_REG18[7:0]			R
0xD6	00000000	Fast I2C data byte 18	
VDP_FAST_REG19[7:0]			R
0xD7	00000000	Fast I2C data byte 19	
VDP_FAST_REG20[7:0]			R
0xD8	00000000	Fast I2C data byte 20	
VDP_FAST_REG21[7:0]			R
0xD9	00000000	Fast I2C data byte 21	
VDP_FAST_REG22[7:0]			R
0xDA	00000000	Fast I2C data byte 22	
VDP_FAST_REG23[7:0]			R
0xDB	00000000	Fast I2C data byte 23	
VDP_FAST_REG24[7:0]			R
0xDC	00000000	Fast I2C data byte 24	
VDP_FAST_REG25[7:0]			R
0xDD	00000000	Fast I2C data byte 25	
VDP_FAST_REG26[7:0]			R
0xDE	00000000	Fast I2C data byte 26	
VDP_FAST_REG27[7:0]			R
0xDF	00000000	Fast I2C data byte 27	
VDP_FAST_REG28[7:0]			R
0xE0	00000000	Fast I2C data byte 28	
VDP_FAST_REG29[7:0]			R
0xE1	00000000	Fast I2C data byte 29	
VDP_FAST_REG30[7:0]			R
0xE2	00000000	Fast I2C data byte 30	
VDP_FAST_REG31[7:0]			R
0xE3	00000000	Fast I2C data byte 31	
VDP_FAST_REG32[7:0]			R
0xE4	00000000	Fast I2C data byte 32	

Reg	Bits	Description	
VDP_FAST_REG33[7:0]			R
0xE5	00000000	Fast I2C data byte 33	
VDP_FAST_REG34[7:0]			R
0xE6	00000000	Fast I2C data byte 34	
VDP_FAST_REG35[7:0]			R
0xE7	00000000	Fast I2C data byte 35	
VDP_FAST_REG36[7:0]			R
0xE8	00000000	Fast I2C data byte 36	
VDP_FAST_REG37[7:0]			R
0xE9	00000000	Fast I2C data byte 37	
VDP_FAST_REG38[7:0]			R
0xEA	00000000	Fast I2C data byte 38	
VDP_FAST_REG39[7:0]			R
0xEB	00000000	Fast I2C data byte 39	
VDP_FAST_REG40[7:0]			R
0xEC	00000000	Fast I2C data byte 40	
VDP_FAST_REG41[7:0]			R
0xED	00000000	Fast I2C data byte 41	
VDP_FAST_REG42[7:0]			R
0xEE	00000000	Fast I2C data byte 42	
VDP_FAST_REG43[7:0]			R
0xEF	00000000	Fast I2C data byte 43	
VDP_FAST_REG44[7:0]			R
0xF0	00000000	Fast I2C data byte 44	

2.4 AFE MAP

Reg	Bits	Description	
PDN_ADC_CLK3			R/W
0x00	00001111	Powerdown the clock to the ADC3 circuitry 0 - Powered up. 1 - Powered down.	
PDN_ADC_CLK2			R/W
0x00	00001111	Powerdown the clock to the ADC 2 circuitry 0 - Powered up. 1 - Powered down.	
PDN_ADC_CLK1			R/W
0x00	00001111	Powerdown the clock to the ADC 1 circuitry 0 - Powered up. 1 - Powered down.	
PDN_ADC_CLK0			R/W
0x00	00001111	Powerdown the clock to the ADC 0 circuitry 0 - Powered up. 1 - Powered down.	
PDN_ADC3			R/W
0x00	00001111	This control is used to power down ADC3. 0 - Powered up. 1 - Powered down.	
PDN_ADC2			R/W
0x00	00001111	This control is used to power down ADC2. 0 - Powered up. 1 - Powered down.	
PDN_ADC1			R/W
0x00	00001111	This control is used to power down ADC1. 0 - Powered up. 1 - Powered down.	
PDN_ADC0			R/W
0x00	00001111	This control is used to power down ADC0. 0 - Powered up. 1 - Powered down.	
ADC_SWITCH_MAN			R/W
0x02	00000000	A control to enable manual input muxing to the ADCs. 0 - Automatic Muxing 1 - Manual Muxing	
EMB_SYNC_SEL_MAN_EN			R/W
0x02	00000000	Enable manual selection of embedded synchronization inputs to synchronization strippers. In automatic mode AIN_SEL[3:0] makes the selection. In manual mode EMB_SYNC_1_SELMAN[1:0] and EMB_SYNC_2_SELMAN[1:0] makes the selection. 0 - Automatic Sync Selection 1 - Manual Sync Selection	
AIN_SEL[2:0]			R/W
0x02	00000000	Input Muxing Mode Code - ADC0|ADC1|ADC2|ADC3|EMB_SYNC_SEL1|EMB_SYNC_SEL2 000 - Ain1 | Ain2 | Ain3 | NC | Sync1 | Sync2 001 - Ain4 | Ain5 | Ain6 | NC | Sync2 | Sync1 010 - Ain7 | Ain8 | Ain9 | NC | Sync3 | Sync1 011 - Ain10|Ain11|Ain12| NC | Sync4 | Sync1 100 - Ain9 |Ain4 | Ain5 | Ain6 | Sync2 | Sync1	

Reg	Bits	Description	
ADC0_SW_MAN[3:0]			R/W
0x03	0000 0000	ADC0 Manual Input Muxing. A control to manually route analog inputs to ADC0. 0001 - Ain1 0100 - Ain4 0111 - Ain7 1001 - Ain9 1010 - Ain10 1011 - Ain11 All Other Values - Not Connected	
ADC1_SW_MAN[3:0]			R/W
0x03	0000 0000	ADC1 Manual Input Muxing. A control to manually route analog inputs to ADC 1. 0010 - Ain2 0100 - Ain4 0101 - Ain5 1000 - Ain8 1011 - Ain11 All Other Values - Not Connected	
ADC2_SW_MAN[3:0]			R/W
0x04	0000 0000	ADC2 Manual Input Muxing. A control to manually rout analog inputs to ADC2 0011 - Ain3 0100 - Ain4 0101 - Ain5 0110 - Ain6 1001 - Ain9 1100 - Ain12 All Other Values - Not Connected	
ADC3_SW_MAN[3:0]			R/W
0x04	0000 0000	ADC3 Manual Input Muxing. A control to manually rout analog inputs to ADC3 0100 - Ain4 0110 - Ain6 0111 - Ain7 All Other Values - Not Connected	
AA_FILTER_EN3			R/W
0x05	0000 0000	ADC3 Anti-Aliasing Filter control. 0 - Disabled. 1 - Enabled.	
AA_FILTER_EN2			R/W
0x05	0000 0000	ADC2 Anti-Aliasing Filter control 0 - Disabled. 1 - Enabled.	
AA_FILTER_EN1			R/W
0x05	0000 0000	ADC1 Anti-Aliasing Filter control 0 - Disabled. 1 - Enabled.	
AA_FILTER_EN0			R/W
0x05	0000 0000	ADC0 Anti-Aliasing Filter control 0 - Disabled. 1 - Enabled.	
AA_FILT_HIGH_BW[1:0]			R/W
0x06 0x07	00 00000 0 0000000	Anti Aliasing Filter Bandwidth Control. AA_FILT_PROG_BW combined with AA_FILT_HIGH_BW controls the anti aliasing filter response. Refer to the Anti Alias Filter Frequency Characteristics table. 00 - Default value; pass band < 17 MHz; 01 - Pass band < 42 MHz; 10 - Pass band < 92 MHz; 11 - Pass band < 146 MHz;	
AA_FILT_PROG_BW[1:0]			R/W
0x07	0 00 00000	Anti-Alias Filter Bandwidth Control. To be used in conjunction with AA_FILT_HIGH_BW. Please refer to Anti Alias Filter Frequency Characteristics table 00 - Default value;	

Reg	Bits	Description	
FB_SELECT[3:0]			R/W
0x14	00000000	Select the Trilevel input to use as Fast Blank 0000 - TRI1 0001 - TRI2 0010 - TRI3 0011 - TRI4 0100 - TRI5/HS_IN1 0101 - TRI6/VS_IN2 0110 - TRI7/HS_IN2 0111 - TRI8/VS_IN2 1000 - SOG1 1001 - SOG2 1010 - HSIN1 1011 - HSIN2 1100 - VSIN1 1101 - VSIN2	
EMB_SYNC_1_SEL_MAN[1:0]			R/W
0x15	00001010	Manual embedded synchronization selection for EMB_SYNC1 00 - Sync1 pin 01 - Sync2 pin 10 - Sync3 pin 11 - Sync4 pin	
EMB_SYNC_2_SEL_MAN[1:0]			R/W
0x15	00001010	Manual embedded synchronization selection for EMB_SYNC2 00 - Sync1 pin 01 - Sync2 pin 10 - Sync3 pin 11 - Sync4 pin	
SYNC1_FILTER_SEL[1:0]			R/W
0x15	00001010	Select the clamp filter on the Sync Channel 1 00 - No filter 01 - Sync > 250ns 10 - Sync > 1us 11 - Sync > 2.5us	
SYNC2_FILTER_SEL[1:0]			R/W
0x15	00001010	Select the clamp filter on the Sync Channel 2 00 - No filter 01 - Sync > 250ns 10 - Sync > 1us 11 - Sync > 2.5us	
SLICE_LEVEL[4:0]			R/W
0x16	10011000	Set the slice level in the synchronization strippers. A smaller value corresponds to a higher slice level. For clamp at 300mV slice level is equal to 600mV - ((SLICE_LEVEL + 1) * 9.375mV). 00000 - Highest slice level XXXXX - Clamp at 300mV and slice at 600mV - ((XXXXX + 1) * 9.375mV) 11000 - Default value 11111 - Lowest slice Level	
TRI1_INT_MASKB[1:0]			R/W
0x17	00000000	Configure the interrupt signal for the Tri1 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI2_INT_MASKB[1:0]			R/W
0x17	00000000	Configure the interrupt signal for the Tri2 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	

Reg	Bits	Description	
TRI3_INT_MASKB[1:0]			R/W
0x17	0000<u>00</u>00	Configure the interrupt signal for the Tri3 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI4_INT_MASKB[1:0]			R/W
0x17	000000<u>00</u>	Configure the interrupt signal for the Tri4 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI5_INT_MASKB[1:0]			R/W
0x18	<u>00</u>000000	Configure the interrupt signal for the Tri5 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI6_INT_MASKB[1:0]			R/W
0x18	00<u>00</u>0000	Configure the interrupt signal for the Tri6 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI7_INT_MASKB[1:0]			R/W
0x18	0000<u>00</u>00	Configure the interrupt signal for the Tri7 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI8_INT_MASKB[1:0]			R/W
0x18	000000<u>00</u>	Configure the interrupt signal for the Tri8 input signal. 00 - No Interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI1_INT_CLEAR[1:0]			SC
0x19	<u>00</u>000000	Clear the interrupts on the Tri1 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI2_INT_CLEAR[1:0]			SC
0x19	00<u>00</u>0000	Clear the interrupts on the Tri2 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI3_INT_CLEAR[1:0]			SC
0x19	0000<u>00</u>00	Clear the interrupts on the Tri3 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI4_INT_CLEAR[1:0]			SC
0x19	000000<u>00</u>	Clear the interrupts on the Tri4 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	

Reg	Bits	Description	
TRI5_INT_CLEAR[1:0]			SC
0x1A	00000000	Clear the interrupts on the Tri5 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI6_INT_CLEAR[1:0]			SC
0x1A	00000000	Clear the interrupts on the Tri6 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI7_INT_CLEAR[1:0]			SC
0x1A	00000000	Clear the interrupts on the Tri7 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI8_INT_CLEAR[1:0]			SC
0x1A	00000000	Clear the interrupts on the Tri8 input 00 - None 01 - Clear the lower slice level interrupt 10 - Clear the upper slice level interrupt 11 - Clear both interrupts	
TRI1_INT_STATUS[1:0]			R
0x1B	00000000	Tri1 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI2_INT_STATUS[1:0]			R
0x1B	00000000	Tri2 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI3_INT_STATUS[1:0]			R
0x1B	00000000	Tri3 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI4_INT_STATUS[1:0]			R
0x1B	00000000	Tri4 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI5_INT_STATUS[1:0]			R
0x1C	00000000	Tri5 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI6_INT_STATUS[1:0]			R
0x1C	00000000	Tri6 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	

Reg	Bits	Description	
TRI7_INT_STATUS[1:0]			R
0x1C	000000<u>00</u>	Tri7 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI8_INT_STATUS[1:0]			R
0x1C	000000<u>00</u>	Tri8 interrupt status 00 - No signal change detected 01 - Signal has crossed lower slice level 10 - Signal has crossed upper slice level 11 - Signal has crossed both slice levels	
TRI1_SLICER_PWRDN			R/W
0x1D	0<u>1</u>101101	Powerdown the Tri1 slicer 0 - Powered up 1 - Powerdown down	
TRI1_BILEVEL_SLICE_EN			R/W
0x1D	01<u>1</u>01101	Enable bi-level slicing on Tri1 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI1_UPPER_SLICE_LEVEL[2:0]			R/W
0x1D	011<u>011</u>01	Set the upper slice level on the Tri1 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI1_LOWER_SLICE_LEVEL[1:0]			R/W
0x1D	01101101	Set the lower slice level on the Tri1 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI2_SLICER_PWRDN			R/W
0x1E	0<u>1</u>101101	Powerdown the Tri2 slicer 0 - Powered up 1 - Powerdown down	
TRI2_BILEVEL_SLICE_EN			R/W
0x1E	01<u>1</u>01101	Enable bi-level slicing on Tri2 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI2_UPPER_SLICE_LEVEL[2:0]			R/W
0x1E	011<u>011</u>01	Set the upper slice level on the Tri2 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI2_LOWER_SLICE_LEVEL[1:0]			R/W
0x1E	01101101	Set the lower slice level on the Tri2 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	

Reg	Bits	Description	
TRI3_SLICER_PWRDN			R/W
0x1F	01101101	Powerdown the Tri3 slicer 0 - Powered up 1 - Powerdown down	
TRI3_BILEVEL_SLICE_EN			R/W
0x1F	01101101	Enable bi-level slicing on Tri3 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI3_UPPER_SLICE_LEVEL[2:0]			R/W
0x1F	01101101	Set the upper slice level on the Tri3 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI3_LOWER_SLICE_LEVEL[1:0]			R/W
0x1F	01101101	Set the lower slice level on the Tri3 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI4_SLICER_PWRDN			R/W
0x20	01101101	Powerdown the Tri4 slicer 0 - Powered up 1 - Powerdown down	
TRI4_BILEVEL_SLICE_EN			R/W
0x20	01101101	Enable bi-level slicing on Tri4 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI4_UPPER_SLICE_LEVEL[2:0]			R/W
0x20	01101101	Set the upper slice level on the Tri4 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI4_LOWER_SLICE_LEVEL[1:0]			R/W
0x20	01101101	Set the lower slice level on the Tri4 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI5_SLICER_PWRDN			R/W
0x21	01101101	Powerdown the Tri5 slicer 0 - Powered up 1 - Powerdown down	
TRI5_BILEVEL_SLICE_EN			R/W
0x21	01101101	Enable bi-level slicing on Tri5 input 0 - Bilevel slicing 1 - Trilevel slicing	

Reg	Bits	Description	
TRI5_UPPER_SLICE_LEVEL[2:0]			R/W
0x21	011011<u>01</u>	Set the upper slice level on the Tri5 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI5_LOWER_SLICE_LEVEL[1:0]			R/W
0x21	01101<u>101</u>	Set the lower slice level on the Tri5 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI6_SLICER_PWRDN			R/W
0x22	0<u>1</u>101101	Powerdown the Tri6 slicer 0 - Powered up 1 - Powerdown down	
TRI6_BILEVEL_SLICE_EN			R/W
0x22	0<u>1</u>101101	Enable bi-level slicing on Tri6 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI6_UPPER_SLICE_LEVEL[2:0]			R/W
0x22	011<u>011</u>01	Set the upper slice level on the Tri6 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI6_LOWER_SLICE_LEVEL[1:0]			R/W
0x22	01101<u>101</u>	Set the lower slice level on the Tri6 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI7_SLICER_PWRDN			R/W
0x23	0<u>1</u>101101	Powerdown the Tri7 slicer 0 - Powered up 1 - Powerdown down	
TRI7_BILEVEL_SLICE_EN			R/W
0x23	0<u>1</u>101101	Enable bi-level slicing on Tri7 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI7_UPPER_SLICE_LEVEL[2:0]			R/W
0x23	011<u>011</u>01	Set the upper slice level on the Tri7 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	

Reg	Bits	Description	
TRI7_LOWER_SLICE_LEVEL[1:0]			R/W
0x23	01101101	Set the lower slice level on the Tri7 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI8_SLICER_PWRDN			R/W
0x24	01101101	Powerdown the Tri8 slicer 0 - Powered up 1 - Powerdown down	
TRI8_BILEVEL_SLICE_EN			R/W
0x24	01101101	Enable bi-level slicing on Tri8 input 0 - Bilevel slicing 1 - Trilevel slicing	
TRI8_UPPER_SLICE_LEVEL[2:0]			R/W
0x24	01101101	Set the upper slice level on the Tri8 input 000 - 75mV 001 - 225mV 010 - 375mV 011 - 525mV 100 - 675mV 101 - 825mV 110 - 975mV 111 - 1.125V	
TRI8_LOWER_SLICE_LEVEL[1:0]			R/W
0x24	01101101	Set the lower slice level on the Tri8 input 00 - 75mV 01 - 225mV 10 - 375mV 11 - 525mV	
TRI1_READBACK[1:0]			R
0x27	00000000	Readback Tri1 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	
TRI2_READBACK[1:0]			R
0x27	00000000	Readback Tri2 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	
TRI3_READBACK[1:0]			R
0x27	00000000	Readback Tri3 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	
TRI4_READBACK[1:0]			R
0x27	00000000	Readback Tri4 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	
TRI5_READBACK[1:0]			R
0x28	00000000	Readback Tri5 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	

Reg	Bits	Description	
TRI6_READBACK[1:0]			R
0x28	0000<u>00</u>0000	Readback Tri6 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	
TRI7_READBACK[1:0]			R
0x28	0000<u>00</u>00	Readback Tri7 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	
TRI8_READBACK[1:0]			R
0x28	000000<u>00</u>	Readback Tri8 DC levels 1x - Signal is higher than upper level 0x - Signal is lower than upper level x1 - Signal is higher than lower level x0 - Signal is lower than lower level	

2.5 SDP MAP

Reg	Bits	Description	
SDP_AD_SECAM_EN			R/W
0x00	0<u>0</u>000010	A control to enable autodetection of SECAM standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Do not enable SECAM to be detected. 1 - Enable SECAM to be detected.	
SDP_AD_N443_EN			R/W
0x00	00<u>0</u>00010	A control to enable autodetection of NTSC-443 standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Do not enable NTSC-443 to be detected 1 - Enable NTSC-443 to be detected	
SDP_AD_PAL60_EN			R/W
0x00	000<u>0</u>0010	A control to enable autodetection of PAL-60 standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard,the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Don't enable PAL-60 to be detected 1 - Enable PAL-60 to be detected	
SDP_AD_PALCN_EN			R/W
0x00	0000<u>0</u>010	A control to enable autodetection of PAL-Comb N standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Do not enable PAL-CombN to be detected 1 - Enable PAL-CombN to be detected	
SDP_AD_PALM_EN			R/W
0x00	00000<u>0</u>10	A control to enable autodetection of PAL-M standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Do not enable PAL-M to be detected 1 - Enable PAL-M to be detected	
SDP_AD_NTSC_EN			R/W
0x00	000000<u>1</u>0	A control to enable autodetection of NTSC-M standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Do not enable NTSC-M to be detected 1 - Enable NTSC-M to be detected	
SDP_AD_PAL_EN			R/W
0x00	0000001<u>0</u>	A control to enable autodetection of PAL-BGHID standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, the corresponding enable bit for that standard should only be set. To allow full autodetect enable all standards via the respective bits. 0 - Do not enable PAL-BGHID to be detected 1 - Enable PAL-BGHID to be detected	
SDP_SECAM_PED_EN			R/W
0x01	0<u>0</u>110110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume SECAM inputs do not have a pedestal 1 - Assume SECAM inputs have a pedestal	
SDP_N443_PED_EN			R/W
0x01	00<u>1</u>10110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume NTSC-443 inputs do not have a pedestal 1 - Assume NTSC-443 inputs have a pedestal	
SDP_PAL60_PED_EN			R/W
0x01	00<u>1</u>10110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume PAL-60 inputs don't have a pedestal 1 - Assume PAL-60 inputs have a pedestal	

Reg	Bits	Description
SDP_PALCN_PED_EN		R/W
0x01	00110110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume PAL-CombN inputs do not have a pedestal 1 - Assume PAL-CombN inputs have a pedestal
SDP_PALM_PED_EN		R/W
0x01	00110110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume PAL-M inputs don't have a pedestal 1 - Assume PAL-M inputs have a pedestal
SDP_NTSC_PED_EN		R/W
0x01	00110110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume NTSC-M inputs do not have a pedestal 1 - Assume NTSC-M inputs have a pedestal
SDP_PAL_PED_EN		R/W
0x01	00110110	A control to force the part to assume that the corresponding standard has a pedestal. Standards with pedestal are clamped to the pedestal level, standards without pedestal are clamped to the back porch level. 0 - Assume PAL-BGHID inputs don't have a pedestal 1 - Assume PAL-BGHID inputs have a pedestal
SDP_Y_AGC_EN		R/W
0x03	11000100	A control to select between automatic and manual luma gain control. 0 - Enable manual luma gain, set by SDP_Y_GAIN_MAN 1 - Enable automatic luma gain based on the sync.
SDP_PW_EN		R/W
0x03	11000100	A control to enable Peak-white luma gain feature. 0 - Disable peak-white luma gain control 1 - Enable peak-white luma gain control
SDP_MAN_GAIN_VCR		R/W
0x03	11000100	A control to select gain method used when a VCR input is detected. 0 - Automatic gain used for VCR inputs (Valid only if SDP_Y_AGC_EN set to 1) 1 - Manual gain used for VCR inputs value is SDP_Y_GAIN_MAN
SDP_Y_GAIN_MAN[12:0]		R/W
0x03 0x04	11000100 00001011	Manual luma gain value, used if SDP_Y_AGC_EN = 0. Also applies to G channel in component modes. Range of 0.5 to 4. 0x040B - Default value
SDP_C_AGC_EN		R/W
0x05	11000011	A control to select between automatic and manual chroma gain (C/Pr/Pb/R/B channels also used for G in case of SCART) 0 - Enable manual chroma gain, gain value set by SDP_C_GAIN_ACT_MAN 1 - Enable automatic chroma gain based on burst power
SDP_PC_EN		R/W
0x05	11000011	A control to enable Peak chroma gain feature. Peak-colour chroma overrides and reduces the gain of the chroma AGC if the chroma signal path becomes larger than a set threshold. Peak chroma can only act to reduce the AGC gain. When there are no more violations of the peak white threshold, the peak chrome algorithm allows the chroma AGC to restore the gain (based on synchronization depth). The recovery rate of the AGC gain is set by the peak chroma recovery register. 0 - Disable peak-chroma gain. 1 - Enable peak-chroma gain.
SDP_C_GAIN_ACT_MAN[12:0]		R/W
0x05 0x06	11000011 11000000	Manual chroma gain value, used if SDP_C_AGC_EN = 0. Also applies to Pr, Pb, R, B channels in component modes Range of 0.5 to 8. 0x03C0 - Default value
SDP_CKILL_EN		R/W
0x07	10001011	A control to enable the color kill feature. 0 - Disable colour-kill feature. 1 - Enable colour-kill feature.
SDP_CK_LOW_THR[6:0]		R/W
0x07	10001011	A control to set colour kill low threshold. If the burst power is below this threshold, enter colour kill mode. 0001011 - Color Kill low threshold

Reg	Bits	Description
SDP_CK_HIGH_THR[7:0]		R/W
0x08	00011010	A control to set colour kill high threshold. If the burst power is above this threshold, enter colour kill mode. 00011010 - Color Kill high threshold
SDP_DGAIN_SPEED[4:0]		R/W
0x0A	11100101	Control to adjust the speed of luma digital gain operation. Only values of 1 to 6 are within a valid range. 0x00 - Freeze digital gain 0x05 - Default value 0x06 - Max value
SDP_C_DGAIN_SPEED[4:0]		R/W
0x0B	11100101	Control to adjust the speed of chroma digital gain operation. Only values of 1 to 6 are within a valid range. This register has an effect only if the SDP_C_AGC_EN bit is set to 1 0x00 - Freeze digital gain 0x05 - Default value 0x06 - Max value >0x06 - Reserved
SDP_DCLP_SPEED[4:0]		R/W
0x0C	11100101	Control to adjust the speed of digital clamp operation 0x00 - Freeze digital gain 0x05 - Default value 0x06 - Max value >0x06 - Reserved
SDP_ACLP_SPEED[4:0]		R/W
0x0D	11100100	A control to adjust the speed of the analog clamp operation. 0x00 - Freeze analog clamp 0x04 - Default value 0x06 - Max value >0x06 - Reserved
SDP_SCM_CTI_EN		R/W
0x0E	00110001	A control to enable CTI in SECAM modes. 0 - Disable CTI in SECAM modes 1 - Enable CTI in SECAM modes
SDP_Y_2D_PK_EN		R/W
0x0E	00110001	A control to enable horizontal peaking filter on the 2D combed output. This peaking filter is applied to the 2D portion of the image before it is mixed with the 3D. It is important to note that it will always be applied to the 2D portion regardless or not as to weather 3D comb is enabled. The purpose of this control is that where 3D comb is enabled, 2D peaking reduces the sharpness/resolution difference perceived in areas where motion occurs. 3D areas are always very sharp due to temporal comb; 2D areas need to be peaked to compensate for softness of 2D/1D separation. 0 - Disable horizontal peaking 1 - Enable horizontal peaking
SDP_V_PK_EN		R/W
0x0E	00110001	A control to enable vertical peaking filter 0 - Disable vertical peaking 1 - Enable vertical peaking
SDP_H_PK_EN		R/W
0x0E	00110001	A control to enable horizontal peaking filter. This is a universal peaking control it is applied after the 2D/3D mixing. It is applied regardless of whether or not 3D has been enabled. 0 - Disable horizontal peaking 1 - Enable horizontal peaking
SDP_LTI_EN		R/W
0x0E	00110001	A control to enable Luma Transient Improvement (LTI) 0 - Disable LTI 1 - Enable LTI
SDP_CTI_EN		R/W
0x0E	00110001	A control to enable Chroma Transient Improvement (CTI). 0 - Disable CTI 1 - Enable CTI
SDP_PC_REC_RATE[11:0]		R/W
0x0F 0x11	00000000 00010000	A control to adjust the Peak-chroma gain recovery speed. The speed at which the chroma gain is increased following a gain reduction due to peak colour violation. A larger value results in the faster speed. 000000010000 - Default value

Reg	Bits	Description	
SDP_PW_REC_RATE[11:0]			R/W
0x0F 0x10	0000<u>0000</u> <u>00000001</u>	A control to adjust the peak-white gain recovery speed. The speed at which the luma gain is increased following a gain reduction due to a peak white violation. A larger value corresponds to a faster speed. 000000000001 - Default value	
SDP_SHIP_EN			R/W
0x12	0000<u>0</u>001	Enable interlaced to progressive conversion for 480i and 576i 0 - Disable 480i - 480p and 576i - 576p conversion 1 - Enable 480i - 480p and 576i - 576p conversion	
SDP_FR_TBC_EN			R/W
0x12	00000<u>0</u>01	A control to enable frame time-based correction (TBC) 0 - Disable frame TBC 1 - Enable frame TBC	
SDP_3D_COMB_EN			R/W
0x12	0000000<u>1</u>	A control to enable the 3D comb filter. When the 3D comb is enabled automatic 2D/3D comb switching is applied based on detected video type. When the 3D comb is disabled 2D combing only is applied. 0 - Disable 3D comb filtering, enable 2D comb mode only 1 - Allow 3D comb filtering when it is possible	
SDP_CONTRAST[9:0]			R/W
0x13 0x17	<u>10000000</u> 000000<u>00</u>	A control to set the Contrast level (luma gain). This control has a range of gain from 0 to 2. It is an unsigned number and has a range from 0x000 (lowest contrast, all black) to 0x3FF (highest contrast). 0x000 - Lowest contrast 0x200 - Default contrast 0x3FF - Highest contrast	
SDP_BRIGHTNESS[9:0]			R/W
0x14 0x17	<u>00000000</u> 0000<u>00</u>00	A control to set the brightness level (luma offset). It is a 2s complement number and has a range of 0x200 (darkest) to 0x1FF (brightest). 0x200 - Darkest 0x000 - Default brightness 0x1FF - Brightest	
SDP_SATURATION[9:0]			R/W
0x15 0x17	<u>10000000</u> 00<u>00</u>0000	This is a control to set the saturation level (chroma gain). It has a valid range 0 -> 1.75. It is an unsigned number and has a range of 0x000 (lowest saturation, no color) to 0x3FF (highest saturation). 0x000 - Lowest saturation (No Color) 0x200 - Default value 0x3FF - Highest saturation	
SDP_HUE[9:0]			R/W
0x16 0x17	<u>00000000</u> <u>00</u>000000	A control to set the Hue (chroma phase rotation). It is a twos compliment number and has a range of 0x200 (-180 degrees) to 0x1FF (+180 degrees). 0x1FF - +180° 0x000 - 0° 0x200 - -180°	
SDP_BLANK_C_VBI			R/W
0x18	<u>1</u>1111111	Setting SDP_BLANK_C_VBI high, the Cr and Cb values of all VBI lines are blanked. This is done so that any data that comes during VBI is not decoded as color and output through Cr and Cb. As a result, it should be possible to send VBI lines into the decoder, then output them through an encoder again and they should appear undistorted. Without this blanking, any wrongly decoded color would are encoded by the video encoder and, therefore, the VBI lines would be distorted. 0 - Pass through colour as decoded during VBI lines 1 - Blank colour during VBI lines	
SDP_FORCE_CKILL_HQI			R/W
0x18	1<u>1</u>111111	A control to force the use of high-quality input (HQI) Y shaping filter when color kill is active. When this bit is disabled the autoselection of the Y shaping filter does not consider colour-kill mode. 0 - HQI Y shaping filter is not used when colour-kill is active. 1 - Force use of HQI Y shaping filter when colour-kill is active.	
SDP_Y_SHAPE_SEL_VBI[5:0]			R/W
0x18	11<u>111111</u>	Y shaping filter user selection for VBI region. 111111 - Default	
SDP_Y_SHAPE_AUTO_EN			R/W
0x19	<u>1</u>1001101	A control to allow manual or automatic selection of Y shaping filter. In manual mode the Y shaping filter is determined by the value of using SDP_Y_SHAPE_SEL_HQI[5:0] 0 - Manual Y shaping filter selection. 1 - Enable automatic selection of Y shaping filter.	

Reg	Bits	Description	
SDP_FORCE_COMP_HQI			R/W
0x19	11001101	A control to force the use of high-quality input (HQI) Y shaping filter when a component input is applied. When this bit is disabled the autoselection of the Y shaping filter is employed. 0 - Automatic selection of Y shaping filter used in component modes 1 - Force Y shaping filter selection to use HQI filter selection in component modes	
SDP_Y_SHAPE_SEL_HQI[5:0]			R/W
0x19	11001101	A control to allow manual Y shaping user filter selection for high quality input signals, selects filters as shown in Y shaping filter selection table 001101 - Default	
SDP_HQI_REQ_STD			R/W
0x1A	10010101	Control that allows user to set conditions required to qualify signal as a high-quality 0 - High-quality input (HQI) requires only stable timebase 1 - High-quality input (HQI) requires both stable and standard (nominal) timebase	
SDP_Y_SHAPE_SEL_LQI[5:0]			R/W
0x1A	10010101	Y shaping filter manual selection for low-quality inputs (LQI), selects filters as shown in Y shaping filter selection table 010101 - Default	
SDP_Y_SHAPE_SEL_SCM[5:0]			R/W
0x1B	00011110	This control is used to select the Y shaping filter for SECAM input signals. 011110 - Default	
SDP_C_SHAPE_AUTO_EN			R/W
0x1C	11000100	A control to allow manual or automatic selection of C shaping filter. Manual selection is determined by SDP_C_SHAPE_SEL_HQI[4:0] 0 - Manual C shaping filter selection using SDP_C_SHAPE_SEL_HQI[4:0] 1 - Enable automatic selection of C shaping filter.	
SDP_CSH_WBW_AUTO			R/W
0x1C	11000100	A control to allow automatic selection of the C shaping filter to be influenced by motion detection. In areas where motion is detected and 2D combing is in operation a narrow C shaping filter is used. For still areas where no motion is detected and 3D combing is in operation a wide C shaping filter is applied. Please refer to C shaping filter flowchart. 0 - Disable auto C shaping filter selection based on motion, default c-shape filter selection. 1 - Enable auto C shaping filter selection based on motion	
SDP_C_SHAPE_SEL_HQI[4:0]			R/W
0x1C	11000100	This control is used to manually select C shaping filter for high-quality inputs (HQI). 00100 - Default	
SDP_C_SHAPE_SEL_LQI[4:0]			R/W
0x1D	00000010	This control is used to select C shaping filter for low-quality inputs (LQI). 00010 - Default	
SDP_C_SHAPE_SEL_SCM[4:0]			R/W
0x1E	00000100	This control is used to set the C shaping filter for SECAM input signals 00100 - Default	
SDP_SPLIT_FILTER_SEL[4:0]			R/W
0x1F	00010010	A control to select the split filter frequency response for the pixel-by-pixel split filter alpha blending. 0xxxx - Reserved 10000 - Filter no. 0 10001 - Filter no. 1 10010 - Filter no. 2 10011 - Filter no. 3 10100 - Filter no. 4 10101 - Filter no. 5 10110 - Filter no. 6 10111 - Reserved 11xxx - Reserved	
SDP_IF_FILT_SEL[4:0]			R/W
0x20	00000000	The SDP_IF_FILT_SEL bits allow the user to compensate for SAW filter characteristics on a composite input as would be observed on a tuner output. 00000 - Default	
SDP_U_DEL_LINE_EN			R/W
0x21	11111111	A control to enable a delay line, in the form of a 2 tap vertical filter for the U component. 0 - Disable delay line for U component. 1 - Enable delay line for U component.	

Reg	Bits	Description
SDP_V_DEL_LINE_EN		R/W
0x21	11111111	A control to enable a delay line, in the form of a 2 tap vertical filter for the V component. 0 - Disable delay line for V component 1 - Enable delay line for V component
SDP_H_PK_INV		R/W
0x22	00100000	A control to inverse Horizontal peaking filter operation. 0 - Normal (gain HF) 1 - Inverse peaking (attenuate HF)
SDP_H_PK_GAIN[3:0]		R/W
0x22	00100000	A control to adjust the gain of the horizontal peaking filter. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The filter response is also user selectable using the SDP_H_PK_BAND and SDP_H_PK_INV controls. Range of 0 to 4 or 0 to -1 depending on SDP_H_PK_INV. 0000 - Minimum value; Gain = 0 0100 - Default value; Gain = 1.06, if SDP_V_PK_INV = 0; Gain = -0.27 if SDP_V_PK_INV = 1 1111 - Maximum value; Gain = 4, if SDP_V_PK_INV = 0; Gain = -1 if SDP_V_PK_INV = 1
SDP_H_PK_CORE[2:0]		R/W
0x22	00100000	The SDP_H_PK_CORE[2:0] bits select the horizontal threshold from the eight possible values listed in the following table. If the filtered output is less than the coring threshold, no high frequency is added back to the input. If the filter output is greater than the core threshold, it is passed through unchanged to the next stage. 000 - 0 001 - 8 010 - 16 011 - 24 100 - 32 101 - 40 110 - 48 111 - 56
SDP_V_PK_INV		R/W
0x23	00010000	A control to inverse Vertical peaking filter operation. 0 - Normal (gain HF) 1 - Inverse peaking (attenuate HF)
SDP_V_PK_GAIN[3:0]		R/W
0x23	00010000	A control to adjust the gain for the vertical peaking filter. The user can select to boost or attenuate the mid region of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. To be used in conjunction with SDP_V_PK_INV range of 0 to 4 or 0 to -1 depending on SDP_V_PK_INV. 0000 - Minimum value; Gain = 0 0010 - Default value, Gain = 0.53, if SDP_V_PK_INV = 0; Gain = -0.13 if SDP_V_PK_INV = 1 1111 - Maximum value; Gain = 4, if SDP_V_PK_INV = 0; Gain = -1 if SDP_V_PK_INV = 1
SDP_V_PK_CORE[2:0]		R/W
0x23	00010000	This control sets the coring threshold for Vertical filter. Signals in output of the filter below this level are cored to 0. 000 - 0 001 - 8 010 - 16 011 - 24 100 - 32 101 - 40 110 - 48 111 - 56
SDP_V_PK_FLIP[2:0]		R/W
0x24	01001100	This bit control the upper convergence limit. Filtered input signal amplitude above this threshold receive no peaking enhancement 000 - 64 001 - 128 010 - 256 011 - 512 100 - 1024 101 - 2048 110 - 3072 111 - 4095

Reg	Bits	Description	
SDP_V_PK_CLIP[1:0]			R/W
0x24	01001100	A control to set the maximum amount of enhancement that can be added before the gain is applied. Set the saturation threshold on output of peaking filter. To be used in conjunction with SDP_V_PK_FLIP. 00 - Flip threshold divided by 2 01 - Flip threshold divided by 7/16 10 - Flip threshold divided by 3/8 11 - Flip threshold divided by 4	
SDP_H_PK_BAND[1:0]			R/W
0x24	01001100	Control to set Horizontal peaking filter band. 00 - No filtering 01 - High-Pass Filter 10 - Band-Pass Filter 1 11 - Band-Pass Filter 2	
SDP_LTI_FILT_SEL			R/W
0x25	00000000	A control to select one of two filter response available in LTI operation. 0 - Select filter response 0 as part of LTI 1 - Select filter response 1 as part of LTI	
SDP_LTI_LEVEL[6:0]			R/W
0x25	00000000	A control to set the amount of LTI applied. A larger value corresponds to the sharpening of luma transients. 0000000 - No transient improvement xxxxxxx - More sharpening of luma transients	
SDP_CTI_FILT_SEL			R/W
0x26	10001111	A control to select one of two filter response available for CTI operation. 0 - Select filter response 0 as part of CTI 1 - Select filter response 1 as part of CTI	
SDP_CTI_LEVEL[5:0]			R/W
0x26	10001111	A control to set the amount of CTI applied. A larger value corresponds to the sharpening of chroma transients. 000000 - No transient improvement 001111 - Default value xxxxxx - More sharpening of chroma transients	
SDP_CTI_FLIP[1:0]			R/W
0x27	10101010	Filtered input signal amplitudes above this threshold receive no CTI edge enhancement 00 - 128 01 - 512 10 - 1024 11 - 4096	
SDP_LTI_FLIP[1:0]			R/W
0x27	10101010	Filtered input signal amplitudes above this threshold receive no LTI edge enhancement 00 - 128 01 - 512 10 - 1024 11 - 4096	
SDP_SCM_CTI_GAIN[1:0]			R/W
0x28	00000010	Changes Gain used for CTI (SECAM modes) 00 - *0.125 01 - *0.25 10 - *0.375 11 - *0.5	
SDP_MAN_FB			R/W
0x2A	00000000	A control to select video source for fast blank operation. This control is only valid SDP_MAN_FB_EN is set to 1. 0 - Select CVBS 1 - Select RGB	

Reg	Bits	Description	
SDP_RGB_DELAY_ADJ[2:0]			R/W
0x2A	000	A signed control to advance or delay for SCART RGB signals in increments of one burst-locked pixel. 000 - No delay. 001 - Delay by 1 pixel. 010 - Delay by 2 pixels. 011 - Delay by 3 pixels. 100 - No advance. 101 - Advance by 1 pixel. 110 - Advance by 2 pixels. 111 - Advance by 3 pixels.	
SDP_MAN_FB_EN			R/W
0x2A	0	A control to select between manual fast blank control via SDP_MAN_FB and automatic fast blank control via the FB signal (please refer to FB_SELECT in AFE Map). 0 - Auto fast blank controlled by FB signal 1 - Allow manual control of FB signal	
SDP_FB_DELAY_ADJ[2:0]			R/W
0x2A	000	A signed control to advance or delay for FB signal in increments of one burst-locked pixel 000 - No delay. 001 - Delay by 1 pixel 010 - Delay by 2 pixels. 011 - Delay by 3 pixels. 100 - No advance. 101 - Advance by 1 pixel. 110 - Advance by 2 pixels. 111 - Advance by 3 pixels.	
SDP_TBC_EN			R/W
0x34	1	A control to enable the line Time Base Correction (TBC) feature. 0 - Disable line TBC 1 - Enable line TBC	
SDP_LBOX_BLK_TOP[7:0]			R
0x4C	00000000	A letterbox readback control to indicate the number of black lines detected at the top of the field. xxxxxxxx - Readback	
SDP_LBOX_BLK_BOT[7:0]			R
0x4D	00000000	A letterbox readback control to indicate the number of black lines detected at the bottom of the field. xxxxxxxx - Readback	
SDP_LBOX_BLK_SUB_BOT[7:0]			R
0x4E	00000000	A letterbox readback control to indicate the number of black lines detected at the bottom of the field. This includes subtitle lines. xxxxxxxx - Readback	
SDP_SYNCTIP_NOISE[11:0]			R
0x4F 0x53	00000000 0000	HSync noise power readback 12-bit ADC codes, larger values indicate more measured noise, not saturated. xxxxxxxxxxxx - Readback of Hsync noise power	
SDP_MV_AGC_DETECTED			R
0x50	0	A Macrovision status readback indicating the detection of Macrovision AGC pulses. 0 - Macrovision AGC pulses part of AGC process not detected 1 - Macrovision AGC pulses part of AGC process detected	
SDP_MV_PS_DETECTED			R
0x50	0	A Macrovision status readback indicating the detection of Macrovision AGC pseudo syncs. 0 - Macrovision pseudo-sync part of AGC process not detected 1 - Macrovision pseudo-sync part of AGC process detected	
SDP_MVCS_TYPE3			R
0x50	0	A Macrovision status readback indicating the detection of Macrovision type 3 colourstripe process. This bit is only valid if SDP_MVCS_DETECT is set to 1 0 - Macrovision type 3 colourstripe process not detected 1 - Macrovision type 3 colourstripe process detected, only valid if SDP_MVCS_DETECT = 1	
SDP_MVCS_DETECT			R
0x50	0	A Macrovision status readback indicating the detection of colourstripe process. 0 - Macrovision colourstripe process not detected 1 - Macrovision colourstripe process detected	

Reg	Bits	Description	
SDP_BP_TOTAL_PULSE_BEG[3:0]			R
0x51	0000 0000	A Macrovision readback indicating the total Macrovision back porch pulses detected at the beginning of the field. xxxx - Number of Macrovision back porch pulses detected at the beginning of the field	
SDP_BP_TOTAL_PULSES_END[3:0]			R
0x51	0000 0000	A Macrovision readback Total Macrovision back porch pulses detected at the end of the field xxxx - Number of Macrovision back porch pulses detected at the end of the field	
SDP_STD[3:0]			R
0x52	0000 0000	An input status readback indicating if the currently active standard, detected mode in autodetect mode, manually programmed mode if in manual mode. Valid results are 0x00 - NTSC-M/J 0x02 - NTSC-443 0x03 - 60HzSECAM 0x04 - PAL-M 0x06 - PAL-60 0x0C - PAL-CombN 0x0E - PAL-BGHID 0x0F - SECAM	
SDP_NOISY_IP			R
0x54	0 0000000	A input status readback indicating the detection of a noisy input signal. Refer also to (SDP_VERY_NOISY_IP and SDP_SYNCTIP_NOISE) 0 - Noisy input not detected 1 - Noisy input detected	
SDP_VERY_NOISY_IP			R
0x54	0 0000000	A input status readback indicating the detection of a very noisy input signal. Refer also to (SDP_NOISY_IP and SDP_SYNCTIP_NOISE) 0 - Very noisy input not detected 1 - Very noisy input detected	
SDP_C_CHAN_ACTIVE			R
0x54	00 0 00000	A input status readback indicating the result of the CVBS\YC detection feature. 0 - CVBS input is detected 1 - Y/C input is detected	
SDP_Y_GAIN_MAN_RB[12:0]			R
0x54 0x55	000 00000 00000000	A readback providing the current luma gain. xxxxxxxxxxxxx - Readback	
SDP_HSWITCH_PRESENT			R
0x56	0 0000000	An input status readback indicating the result of the Head switch detection using algorithm 1. 0 - Head switch not detected by algorithm 1 1 - Head switch detected by algorithm 1	
SDP_BLK_NSTD			R
0x56	0 0000000	An input status readback indicating the length of 192 line block of pixels in clock cycles it within the threshold set by SDP_FRM_NSTD_THR of a nominal standard. 0 - Length of 192 line block of pixels in clock cycles is within +- SDP_FRM_NSTD_THR of nominal value 1 - Length of 192 line block of pixels in clock cycles is not within +- SDP_FRM_NSTD_THR of nominal value	
SDP_FLD_NSTD			R
0x56	000 0 00000	An input status readback indicating if the Field length in clock cycles is within the threshold set by SDP_FRM_NSTD_THR of a nominal standard. 0 - Field length in clock cycles is within +- SDP_FRM_NSTD_THR of nominal value 1 - Field length in clock cycles is not within +- SDP_FRM_NSTD_THR of nominal value	
SDP_FRM_NSTD			R
0x56	000 0 0000	An input status readback indicating if the Frame length in clock cycles is within the threshold set by SDP_FRM_NSTD_THR. 0 - Frame length in clock cycles is within +- SDP_FRM_NSTD_THR of nominal value 1 - Frame length in clock cycles is not within +- SDP_FRM_NSTD_THR of nominal value	
SDP_LC_NSTD			R
0x56	0000 0 000	An input status readback indicating if the field length varies by more than one line from field to field. 0 - Field length in terms of number of lines does not vary by more than 1 line from field to field 1 - Field length in terms of number of lines varies by more than 1 line from field to field	

Reg	Bits	Description	
SDP_ALLOW_MED_PLL			R
0x56	00000<u>0</u>00	An input status readback indicating if the input could be from a VCR source. Only valid if SDP_ALLOW_SLOW_PLL is 0. If SDP_ALLOW_SLOW_PLL is 1 this bit is ignored. 0 - Input is a VCR, a fast HSync PLL speed used 1 - Input may be a VCR, a medium HSync PLL speed used	
SDP_ALLOW_SLOW_PLL			R
0x56	0000000<u>0</u>	An input status readback indicating if the input could be from a VCR source. To be used in conjunction SDP_ALLOW_MED_PLL. 0 - Input may be a VCR, refer to SDP_ALLOW_MED_PLL 1 - Input is not a VCR slow HSync PLL speed used	
SDP_FREE_RUN			R
0x56	0000000<u>0</u>	A status readback indicating free-run status. If set the part is free-running due to no video detected on input or forced free run mode. 0 - Part is not free running 1 - Part is free running	
SDP_CKILL_ACT			R
0x57	<u>0</u>0000000	A status readback indicating the Colour kill status. 0 - Colour kill is not active 1 - Colour kill is active (and enabled)	
SDP_VS_STD_MODE			R
0x57	0<u>0</u>000000	An input status readback indicating the detection for regular frame lengths on the input. 0 - Regular frame lengths not detected on input 1 - Regular frame lengths detected on input	
SDP_ALLOW_3D_COMB			R
0x57	000<u>0</u>0000	An input status readback indicating the suitability of the input for 3D combing. 0 - Non-standard input detected, 3D comb not allowed, 2d comb used 1 - Standard input detected, 3D comb allowed	
SDP_INTERLACED			R
0x57	0000<u>0</u>000	A input status readback indicating the detection of an interlaced format on the input. 0 - Alternating field sequence not detected on input 1 - Alternating field sequence detected on input	
SDP_TRICK_MODE			R
0x57	00000<u>0</u>00	An input status readback indicating the detection of a VCR trick mode operation on the input. 0 - VCR trick mode not detected, line TBC not allowed 1 - VCR trick mode detected, line TBC allowed if enabled	
SDP_PR_DETECTED_IN_SD			R
0x58	0<u>0</u>000000	An input status readback indicating mismatch between selected SD mode, and type of input signal. 0 - Normal operation 1 - Indicates SDP is in SD mode but PR input is detected	
SDP_BURST_LOCKED_RB			R
0x59	<u>0</u>0000000	A readback indicating the status of the burst locking loop. 0 - Burst locking loop is not locked 1 - Burst locking loop is locked	
SDP_AD_50_60_HZ			R
0x59	0000<u>0</u>000	A readback indicating the result of the field rate detection on the input. 0 - Vertical refresh rate of 60Hz detected on the input 1 - Vertical refresh rate of 50Hz detected on the input	
SDP_PAL_SW_LOCKED			R
0x59	00000<u>0</u>00	A input status readback indicating the detection of a PAL swinging burst sequence on the input. 0 - PAL swinging burst sequence is not detected. 1 - PAL swinging burst sequence is detected.	
SDP_FSC_FREQ_OK			R
0x59	0000000<u>0</u>	An input status readback indicating if detected frequency subcarrier is close to that of the selected standard. 0 - Detected Fsc frequency is not close to that of selected standard 1 - Detected Fsc frequency is close to that of selected standard.	

Reg	Bits	Description	
SDP_SCM_LOCKED			R
0x59	0000000<u>0</u>	A input status readback indicating the detection of a SECAM input. 0 - SECAM is not detected on the input 1 - SECAM is detected on the input	
SDP_VIDEO_DETECTED			R
0x5A	0000000<u>0</u>	A input status readback indicating the detection of a valid video input. 0 - Input is invalid or no input is connected 1 - Indicates valid SD/PR video input detected	
SDP_EXTEND_VS_MAX_FREQ			R/W
0x7B	0110100<u>1</u>	A control to extend the minimum frequency VSync lock range. 0 - Normal minimum frequency VSync lock range 1 - Extended minimum frequency VSync lock range	
SDP_EXTEND_VS_MIN_FREQ			R/W
0x7B	0110100<u>1</u>	A control to extend the maximum frequency VSync lock range. 0 - Normal maximum frequency VSync lock range 1 - Extended maximum frequency VSync lock range	
SDP_LIMIT_Y_GAIN			R/W
0x89	<u>0</u>0000011	A control to limit the luma gain. 0 - Normal operation. 1 - Limits the luma gain to a range of 50%-200%	
SDP_LIMIT_C_GAIN			R/W
0x89	0<u>0</u>000011	A control to limit the chroma gain. 0 - Normal operation. 1 - Limits the chroma gain to a range of 50%-200%.	
SDP_LIMIT_UV_GAIN			R/W
0x89	00<u>0</u>00011	A control to limit U/V gain. 0 - Normal operation. 1 - limits the U&V gain to a range of 50%-200%	
SDP_LIMIT_G_GAIN			R/W
0x89	000<u>0</u>0011	A control to limit the SD SCART FB RGB gain. 0 - Normal operation. 1 - Limits the SD (FB) RGB gain to a range of 50%-200%	
SDP_NSY_DIS_SFS_STD			R/W
0x98	<u>1</u>0111111	A control to enable HQI shaping filter when a noisy input is detected. 0 - Allow HQI shape filter even if noisy input detected 1 - Disable HQI shape filter if noisy input detected	
SDP_HSW2_DIS_SFS_STD			R/W
0x98	1<u>0</u>111111	A control to enable HQI shaping filter when a head switch is detected on the input by head switch algorithm 1. 0 - Allow HQI shape filter even if head switch detection algorithm 2 detects head switches. 1 - Disable HQI shape filter if head switch detection algorithm 2 detects head switches.	
SDP_HSW1_DIS_SFS_STD			R/W
0x98	10<u>1</u>11111	A control to enable HQI shaping filter when a head switch is detected on the input by head switch algorithm 2. 0 - Allow HQI shape filter even if head switch detection algorithm 1 detects head switches. 1 - Disable HQI shape filter if head switch detection algorithm 1 detects head switches.	
SDP_LC_DIS_SFS_STD			R/W
0x98	101<u>1</u>1111	A control to enable HQI shaping filter when incorrect number of lines per frame have been detected. 0 - Allow HQI shape filter even if incorrect number of lines per frame detected. 1 - Disable HQI shape filter if clean and incorrect lines per frame detected.	
SDP_BLK_DIS_SFS_STD			R/W
0x98	1011<u>1</u>111	A control to enable HQI shaping filter when a non standard block length is detected. 0 - Allow HQI shape filter even if SDP_BLK_NSTD detected 1 - Disable HQI shape filter if clean and SDP_BLK_NSTD detected	
SDP_FLD_SFS_STD			R/W
0x98	10111<u>1</u>11	A control to enable HQI shaping filter when a non-standard field is detected. 0 - Allow HQI shape filter even if SDP_FLD_NSTD detected 1 - Disable HQI shape filter if clean and SDP_FLD_NSTD	

Reg	Bits	Description	
SDP_FRM_DIS_SFS_STD			R/W
0x98	1011111<u>1</u>	A control to enable HQI shaping filter when a non-standard frame is detected. 0 - Allow hqi shape filter even if SDP_FRM_NSTD detected 1 - Disable HQI shape filter if clean input and SDP_FRM_NSTD detected	
SDP_VNSY_DIS_SFS_STD			R/W
0x98	1011111<u>1</u>	A control to enable HQI shaping filter when a very noisy input is detected. 0 - Allow HQI shape filter even if noisy input detected 1 - Disable HQI shape filter if very noisy input detected	
SDP_SHAPE_STD_FILT_SEL[2:0]			R/W
0x99	0<u>001</u>0000	A control to select the length of filter that is used when selecting the shaping filters. 000 - No filtering 001 - 0.25s 010 - 0.55s 011 - 0.81s 100 - 1.10s 101 - 1.36s 110 - 1.63s 111 - 2.00s	
SDP_ALLOW_3D_FILT_SEL[2:0]			R/W
0x9A	00000<u>001</u>	SDP_ALLOW_3D_FILT_SEL[2:0] controls the time constant applied to the deglitching filter for the 3D comb decision. 000 - No filtering 001 - 0.25s 010 - 0.55s 011 - 0.81s 100 - 1.10s 101 - 1.36s 110 - 1.63s 111 - 2.00s	
SDP_NOISY_THR[7:0]			R/W
0xA1	<u>01010000</u>	A control to set the threshold for input to be detected as noisy. A higher value reduces the possibility of detecting the input as noisy. 0x50 - Default value	
SDP_VERY_NOISY_THR[7:0]			R/W
0xA2	<u>10100000</u>	A control to set the threshold for input to be detected as very noisy. A higher value reduces the possibility of detecting the input to be very noisy. 0xA0 - Default value	
SDP_CKILL_DIS_3D			R/W
0xA3	<u>1</u>0111110	A control to enable 3D combing if colour kill mode is active. 0 - Allow 3D comb even if colour kill is active 1 - Disable 3D comb if colour kill is active	
SDP_CKILL_DIS_2D			R/W
0xA4	<u>1</u>0111111	A control to enable 2D combing even if colour kill mode is active. This would effectively be pass through mode. 0 - Use 2D comb even if colour kill is active. 1 - Disable 2D comb if colour kill is active.	
SDP_NOISY_HSW2_DIS_3D			R/W
0xA4	1<u>0</u>111111	A control to enable 3D combing if a noisy input has been detected and a headswitch has been detected on the input by algorithm 2. 0 - Allow 3D comb if noisy input detected even if head switch detection algorithm 2 detects head switches. 1 - Disable 3D comb if noisy input detected and head switch detection algorithm 2 detects head switches.	
SDP_NOISY_HSW1_DIS_3D			R/W
0xA4	10<u>1</u>11111	A control to enable 3D combing if a noisy input has been detected and a headswitch has been detected on the input by algorithm 1. 0 - Allow 3D comb if noisy input detected even if head switch detection algorithm 1 detects head switches. 1 - Disable 3D comb if noisy input detected and head switch detection algorithm 1 detects head switches.	
SDP_NOISY_LC_DIS_3D			R/W
0xA4	101<u>1</u>1111	A control to enable 3D combing if a noisy input has been detected and a non-standard number of lines per frame has been detected on the input 0 - Allow 3D comb if noisy input detected even if incorrect number of lines per frame detected. 1 - Disable 3D comb if noisy input detected and incorrect lines per frame detected.	

Reg	Bits	Description
SDP_NOISY_BLK_DIS_3D		R/W
0xA4	10111111	A control to enable 3D combing if a noisy input is detected and a non standard block length is detected on the input. 0 - Allow 3D comb if noisy input detected even if SDP_BLK_NSTD detected 1 - Disable 3D comb if noisy input detected and SDP_BLK_NSTD detected
SDP_NOISY_FLD_DIS_3D		R/W
0xA4	10111111	A control to enable 3D combing if a noisy input is detected and a non standard field length is detected. 0 - Allow 3D comb if noisy input detected even if SDP_FLD_NSTD detected 1 - Disable 3D comb if noisy input detected and SDP_FLD_NSTD detected
SDP_NOISY_FRM_DIS_3D		R/W
0xA4	10111111	A control to enable 3D combing if a noisy input is detected and a non standard frame length is detected. 0 - Allow 3D comb if noisy signal even if SDP_FRM_NSTD detected. 1 - Disable 3D comb if noisy input detected and SDP_FRM_NSTD detected.
SDP_NOISY_DIS_3D		R/W
0xA4	10111111	A control to enable 3D combing if a noisy input is detected . 0 - Allow 3D comb if noisy input detected. 1 - Disable 3D comb if noisy input detected.
SDP_P60_N443_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing for PAL-60 and NTSC-443 even though it does not work perfectly due to sub-optimal mathematical relationship of subcarrier frequency versus horizontal frequency for those standards. 0 - Use 3D comb on PAL-60 and NTSC-443 inputs. 1 - Disable 3D comb for PAL-60 and NTSC-443 inputs.
SDP_VNOISY_HSW2_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input is detected and head switch is detected on the input by algorithm 2. 0 - Allow 3D comb if very noisy input detected even if head switch detection algorithm 2 detects head switches. 1 - Disable 3D comb if very noisy input detected and head switch detection algorithm 2 detects head switches.
SDP_VNOISY_HSW1_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input is detected and head switch is detected on the input by algorithm 1 0 - Allow 3D comb if very noisy input detected even if head switch detection algorithm 1 detects head switches. 1 - Disable 3D comb if very noisy input detected and head switch detection algorithm 1 detects head switches.
SDP_VNOISY_LC_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input is detected and an incorrect frame length is detected on the input. 0 - Allow 3D comb if very noisy input detected even if incorrect number of lines per frame detected. 1 - Disable 3D comb if very noisy input detected and incorrect lines per frame detected.
SDP_VNOISY_BLK_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input is detected and a non-standard block length is detected on the input. 0 - Allow 3D comb if very noisy input detected even if SDP_BLK_NSTD detected 1 - Disable 3D comb if very noisy input detected and SDP_BLK_NSTD detected
SDP_VNOISY_FLD_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input is detected and a non-standard field length has been detected on the input. 0 - Allow 3D comb if very noisy input detected even if SDP_FLD_NSTD detected 1 - Disable 3D comb if very noisy input detected and SDP_FLD_NSTD detected
SDP_VNOISY_FRM_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input is detected and a non-standard frame length has been detected on the input. 0 - Allow 3D comb if very noisy signal even if SDP_FRM_NSTD detected 1 - Disable 3D comb if very noisy input detected and SDP_FRM_NSTD detected
SDP_VNOISY_DIS_3D		R/W
0xA5	10111111	A control to enable 3D combing if a very noisy input has been detected. 0 - Allow 3D comb if very noisy input detected 1 - Disable 3D comb if very noisy input detected
SDP_3D_COMB_NOISE_SNS[6:0]		R/W
0xA8	01000000	A control to set the 3D Comb Noise Sensitivity. Larger values allow more temporal comb for noisy RF signals but may also introduce motion error. This is an unsigned control. 0000000 - Minimum value 1000000 - Default value 1111111 - Maximum value

Reg	Bits	Description
SDP_3D_COMB_CHROMA_CORE[3:0]		R/W
0xA9	1000[1000]	A control to set 3D Comb Chroma Coring. Larger values decrease 3D comb motion detection sensitivity to chroma motion and noise. This is an unsigned control. 0000 - Minimum value 1000 - Default value 1111 - Maximum value
SDP_3D_COMB_CHROMA_SNS[3:0]		R/W
0xA9	[1000]1000	A control to set 3D Comb Chroma Sensitivity. Larger values increase 3D comb motion detection sensitivity to chroma motion and noise. This is an unsigned control. 0000 - Minimum value 1000 - Default value 1111 - Maximum value
SDP_3D_COMB_LUMA_CORE[3:0]		R/W
0xAA	1000[1000]	A control to set the 3D Comb Luma Coring. Larger values decrease 3D comb motion detection sensitivity to luma motion and noise. This is an unsigned control. 1000 - Larger values increase 3D processing
SDP_3D_COMB_LUMA_SNS[3:0]		R/W
0xAA	[1000]1000	A control to set the 3D Comb Luma Sensitivity. Larger values increase 3D comb motion detection sensitivity to luma motion and noise. This is an unsigned control. 0000 - Minimum value 1000 - Default value 1111 - Maximum value
SDP_SHIP_INT_EN		R/W
0xD9	0[1]000100	Selects method of interlaced to progressive conversion. This control is valid only if SDP_SHIP_EN is set to 1. 0 - Use line doubling mode for 480i-> 480p and 576i-> 576p conversion 1 - Use line interpolation mode for 480i-> 480p and 576i-> 576p conversion
SDP_LBOX_END_DEL[3:0]		R/W
0xDB	1000[1000]	A control to set delay letterbox detection end line versus default position. 1000 - Letterbox detection ends with the last active line of video on a field
SDP_LBOX_BEG_DEL[3:0]		R/W
0xDB	[1000]1000	A control to delay letterbox detection begin line versus default position. 1000 - Letterbox detection aligned with the start line of active video. Window starts after VBI data line.
SDP_LBOX_BLK_LVL[2:0]		R/W
0xDC	000[00010]	A control to set expected blank level at lbox detection block. A larger value corresponds to a higher blank level. 000 - Default value
SDP_LBOX_THR[4:0]		R/W
0xDC	[00010]	A control to set threshold for black line detection in letterbox detection. A larger value increases the possibility of detecting a line as black. 00010 - Default threshold for detection of black lines. The larger the value the more likely to detect the line as black.
SDP_FREE_RUN_AUTO		R/W
0xDD	1011[1]100	A control to enable automatic free-run operation. The part will enter free run if no valid input video detected. 0 - Do not free run even if no valid input video detected 1 - Free run if no valid input video detected.
SDP_FREE_RUN_MAN_COL_EN		R/W
0xDD	10111[1]00	A control to enable manual setting of video data output in video mode. If set free run luma and chroma values are set by SDP_FREE_RUN_Y, SDP_FREE_RUN_V, SDP_FREE_RUN_U. 0 - If in free run output decoded video data. 1 - If in free run output manual luma and chroma values as set by SDP_FREE_RUN_Y, SDP_FREE_RUN_V, SDP_FREE_RUN_U
SDP_FREE_RUN_CBAR_EN		R/W
0xDD	101111[0]0	A control to select colour bar data to be output in manual mode. 0 - If in free run mode output free- run mode data. 1 - If in free run mode output colour bar data
SDP_FORCE_FREE_RUN		R/W
0xDD	1011110[0]	A control to force free-run mode irrespective of input lock status . 0 - Normal operation 1 - Force free run

Reg	Bits	Description	
SDP_FREE_RUN_Y[7:0]			R/W
0xDE	00100011	Control to set Luma level to output in free run mode if SDP_FREE_RUN_MAN_COL_EN = 1 0x23 - Default value	
SDP_FREE_RUN_V[3:0]			R/W
0xDF	0111 1101	Control to set V level to output in free run mode if SDP_FREE_RUN_MAN_COL_EN = 1 0111 - Default value	
SDP_FREE_RUN_U[3:0]			R/W
0xDF	0111 1101	Control to set U level to output in free run mode if SDP_FREE_RUN_MAN_COL_EN = 1 1101 - Default value	

2.6 CEC MAP

Reg	Bits	Description	
CEC_TX_FRAME_HEADER[7:0]			R/W
0x00	00000000	Header block in the transmitted frame	
CEC_TX_FRAME_DATA0[7:0]			R/W
0x01	00000000	Opcode block in the transmitted frame	
CEC_TX_FRAME_DATA1[7:0]			R/W
0x02	00000000	Operand 1 in the transmitted frame	
CEC_TX_FRAME_DATA2[7:0]			R/W
0x03	00000000	Operand 2 in the transmitted frame	
CEC_TX_FRAME_DATA3[7:0]			R/W
0x04	00000000	Operand 3 in the transmitted frame	
CEC_TX_FRAME_DATA4[7:0]			R/W
0x05	00000000	Operand 4 in the transmitted frame	
CEC_TX_FRAME_DATA5[7:0]			R/W
0x06	00000000	Operand 5 in the transmitted frame	
CEC_TX_FRAME_DATA6[7:0]			R/W
0x07	00000000	Operand 6 in the transmitted frame	
CEC_TX_FRAME_DATA7[7:0]			R/W
0x08	00000000	Operand 7 in the transmitted frame	
CEC_TX_FRAME_DATA8[7:0]			R/W
0x09	00000000	Operand 8 in the transmitted frame	
CEC_TX_FRAME_DATA9[7:0]			R/W
0x0A	00000000	Operand 9 in the transmitted frame	
CEC_TX_FRAME_DATA10[7:0]			R/W
0x0B	00000000	Operand 10 in the transmitted frame	
CEC_TX_FRAME_DATA11[7:0]			R/W
0x0C	00000000	Operand 11 in the transmitted frame	
CEC_TX_FRAME_DATA12[7:0]			R/W
0x0D	00000000	Operand 12 in the transmitted frame	
CEC_TX_FRAME_DATA13[7:0]			R/W
0x0E	00000000	Operand 13 in the transmitted frame	
CEC_TX_FRAME_DATA14[7:0]			R/W
0x0F	00000000	Operand 14 in the transmitted frame	
CEC_TX_FRAME_LENGTH[4:0]			R/W
0x10	00000000	Message size of the transmitted frame. This is the number of byte in the outgoing message including the header. xxxxx - Total number of bytes (including header byte) to be sent	

Reg	Bits	Description	
CEC_TX_ENABLE			R/W
0x11	0000000<u>0</u>	This bit enables the TX section. When set to 1 it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is completed this bit is automatically reset to 0. If it is manually set to 0 during a message transmission it may terminate the transmission depending on what stage of the transmission process has been reached. If the message transmission is sill in the 'signal free time' stage the message transmission will be terminated. If data transmission has begun then the transmission will continue until the message is fully sent, or until an error condition occurs. 0 - Transmission mode disabled 1 - Transmission mode enabled and message transmission started	
CEC_TX_RETRY[2:0]			R/W
0x12	0<u>001</u>0011	The number of times the CEC TX should try to retransmit the message if an error condition is encountered. Per the CEC spec this value should not be set to a value greater than 5. 001 - Try to retransmit the message 1 time if an error occurs xxx - Try to retransmit the message xxx times if an error occurs	
CEC_RETRY_SFT[3:0]			R/W
0x12	0001<u>0011</u>	Signal Free Time of periods for retransmission retry. This parameter should be set to a value equal to or greater than 3 and strictly less than 5.	
CEC_TX_SFT[3:0]			R/W
0x13	<u>0101</u>0111	Signal Free Time if the device is a new initiator. This parameter should be set to a value equal to or greater than 5 and strictly less than 7.	
CEC_TX_SFT[3:0]			R/W
0x13	0101<u>0111</u>	Signal Free Time if the device transmits a next frame immediately after its previous frame. This parameter should be set to a value equal to or greater than 7 and strictly less than 10.	
CEC_TX_LOWDRIVE_COUNTER[3:0]			R
0x14	<u>0000</u>0000	The number of times that the LOWDRIVE error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1. 0000 - No error condition XXXX - The number of times the LOWDRIVE error condition was encountered	
CEC_TX_NACK_COUNTER[3:0]			R
0x14	0000<u>0000</u>	The number of times that the NACK error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1. 0000 - No error condition XXXX - The number of times the NACK error condition was encountered	
CEC_BUF0_RX_FRAME_HEADER[7:0]			R
0x15	<u>00000000</u>	Header block of the received frame stored in receiver frame buffer 0.	
CEC_BUF0_RX_FRAME_DATA0[7:0]			R
0x16	<u>00000000</u>	Opcode block of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA1[7:0]			R
0x17	<u>00000000</u>	Operand 1 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA2[7:0]			R
0x18	<u>00000000</u>	Operand 2 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA3[7:0]			R
0x19	<u>00000000</u>	Operand 3 of the received frame in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA4[7:0]			R
0x1A	<u>00000000</u>	Operand 4 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA5[7:0]			R
0x1B	<u>00000000</u>	Operand 5 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA6[7:0]			R
0x1C	<u>00000000</u>	Operand 6 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA7[7:0]			R
0x1D	<u>00000000</u>	Operand 7 of the received frame stored in receiver frame buffer 0	

Reg	Bits	Description	
CEC_BUF0_RX_FRAME_DATA8[7:0]			R
0x1E	00000000	Operand 8 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA9[7:0]			R
0x1F	00000000	Operand 9 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA10[7:0]			R
0x20	00000000	Operand 10 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA11[7:0]			R
0x21	00000000	Operand 11 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA12[7:0]			R
0x22	00000000	Operand 12 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA13[7:0]			R
0x23	00000000	Operand 13 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA14[7:0]			R
0x24	00000000	Operand 14 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_LENGTH[4:0]			R
0x25	00000000	xxxxx - The total number of bytes (including header byte) that were received into buffer 0	
CEC_LOGICAL_ADDRESS_MASK_2			R/W
0x27	00010000	Mask bit for logical address 2 0 - Logical address 2 disabled 1 - Logical address 2 enabled	
CEC_LOGICAL_ADDRESS_MASK_1			R/W
0x27	00010000	Mask bit for logical address 1 0 - Logical address 1 disabled 1 - Logical address 1 enabled	
CEC_LOGICAL_ADDRESS_MASK_0			R/W
0x27	00010000	Mask bit for logical address 0 0 - Logical address 0 disabled 1 - Logical address 0 enabled	
CEC_ERROR_REPORT_MODE			R/W
0x27	00010000	Error report mode 0 - Only report short bit period errors 1 - Report both short and long bit period errors	
CEC_ERROR_DET_MODE			R/W
0x27	00010000	Error detection mode 0 - If any short bit period error, except for start bit, is detected, the CEC controller immediately drives the CEC line low for 3.6ms 1 - If a short bit period is detected in the data block where the destination is the CEC section or a target CEC device, the CEC controller immediately drives the CEC line low for 3.6ms	
CEC_FORCE_NACK			R/W
0x27	00010000	Force NO-ACK Control Setting this bit forces the CEC controller not acknowledge any received messages. 0 - Acknowledge received messages 1 - Do not acknowledge received messages	
CEC_FORCE_IGNORE			R/W
0x27	00010000	Force Ignore Control. Setting this bit forces the CEC controller to ignore any directly addressed messages. Normal operation should be kept for the broadcast message 0 - Do not ignore directly address messages 1 - Ignore any directly addressed message	
CEC_LOGICAL_ADDRESS1[3:0]			R/W
0x28	11111111	Logical address 1 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[1] to 1 1111 - Default value xxxx - User specified logical address	

Reg	Bits	Description	
CEC_LOGICAL_ADDRESS0[3:0]			R/W
0x28	1111<u>1111</u>	Logical address 0 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[0] to 1 1111 - Default value xxxx - User specified logical address	
CEC_LOGICAL_ADDRESS2[3:0]			R/W
0x29	0000<u>1111</u>	Logical address 2 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[2] to 1 1111 - Default value xxxx - User specified logical address	
CEC_POWER_UP			R/W
0x2A	0011111<u>0</u>	Power Mode of CEC module 0 - Power down the CEC module 1 - Power up the CEC module	
CEC_GLITCH_FILTER_CTRL[5:0]			R/W
0x2B	00<u>000111</u>	The CEC input signal is sampled by the input clock (XTAL clock). CEC_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths less than the minimum specified width are considered glitches and will be removed by the filter. 000000 - Disable the glitch filter 000001 - Filter out pulses with width less than 1 clock cycle 000010 - Filter out pulses with width less than 2 clock cycles - ... 000111 - Filter out pulses with width less than 7 clock cycles - ... 111111 - Filter out pulses with width less than 63 clock cycles	
CEC_CLR_RX_RDY2			SC
0x2C	0000<u>0</u>000	Clear control for CEC_RX_RDY2 0 - Retain the value of the CEC_RX_RDY2 flag 1 - Clear the value of the CEC_RX_RDY2 flag	
CEC_CLR_RX_RDY1			SC
0x2C	00000<u>0</u>00	Clear control for CEC_RX_RDY1 0 - Retain the value of the CEC_ RX_RDY1 flag 1 - Clear the value of the CEC_RX_RDY1 flag	
CEC_CLR_RX_RDY0			SC
0x2C	000000<u>0</u>0	Clear control for CEC_RX_RDY0 0 - Retain the value of the CEC_RX_RDY0 flag 1 - Clear the value of the CEC_RX_RDY0 flag	
CEC_SOFT_RESET			SC
0x2C	0000000<u>0</u>	CEC module software reset. 0 - No function 1 - Reset the CEC module	
CEC_DIS_AUTO_MODE			R/W
0x4C	00000<u>0</u>00	A control to disable the automatic CEC power up feature when in chip powerdown mode. 0 - Automatic power up feature enabled 1 - Automatic power up feature disabled	
CEC_BUF2_TIMESTAMP[1:0]			R
0x53	00<u>00</u>0000	Time stamp for frame stored in receiver frame buffer 2. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buffered, this frame was the third to be received	
CEC_BUF1_TIMESTAMP[1:0]			R
0x53	0000<u>00</u>00	Time stamp for frame stored in receiver frame buffer 1. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buffered, this frame was the third to be received	

Reg	Bits	Description	
CEC_BUF0_TIMESTAMP[1:0]			R
0x53	000000<u>00</u>	Time stamp for frame stored in receiver frame buffer 0. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buffered, this frame was the third to be received	
CEC_BUF1_RX_FRAME_HEADER[7:0]			R
0x54	<u>00000000</u>	Header block of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA0[7:0]			R
0x55	<u>00000000</u>	Opcode block of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA1[7:0]			R
0x56	<u>00000000</u>	Operand 1 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA2[7:0]			R
0x57	<u>00000000</u>	Operand 2 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA3[7:0]			R
0x58	<u>00000000</u>	Operand 3 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA4[7:0]			R
0x59	<u>00000000</u>	Operand 4 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA5[7:0]			R
0x5A	<u>00000000</u>	Operand 5 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA6[7:0]			R
0x5B	<u>00000000</u>	Operand 6 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA7[7:0]			R
0x5C	<u>00000000</u>	Operand 7 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA8[7:0]			R
0x5D	<u>00000000</u>	Operand 8 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA9[7:0]			R
0x5E	<u>00000000</u>	Operand 9 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA10[7:0]			R
0x5F	<u>00000000</u>	Operand 10 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA11[7:0]			R
0x60	<u>00000000</u>	Operand 11 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA12[7:0]			R
0x61	<u>00000000</u>	Operand 12 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA13[7:0]			R
0x62	<u>00000000</u>	Operand 13 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA14[7:0]			R
0x63	<u>00000000</u>	Operand 14 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_LENGTH[4:0]			R
0x64	000<u>00000</u>	xxxxx - The total number of bytes (including header byte) that were received into buffer 1	
CEC_BUF2_RX_FRAME_HEADER[7:0]			R
0x65	<u>00000000</u>	Header block of the received frame in receiver frame buffer 2	

Reg	Bits	Description	
CEC_BUF2_RX_FRAME_DATA0[7:0]			R
0x66	00000000	Opcode block of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA1[7:0]			R
0x67	00000000	Operand 1 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA2[7:0]			R
0x68	00000000	Operand 2 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA3[7:0]			R
0x69	00000000	Operand 3 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA4[7:0]			R
0x6A	00000000	Operand 4 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA5[7:0]			R
0x6B	00000000	Operand 5 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA6[7:0]			R
0x6C	00000000	Operand 6 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA7[7:0]			R
0x6D	00000000	Operand 7 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA8[7:0]			R
0x6E	00000000	Operand 8 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA9[7:0]			R
0x6F	00000000	Operand 9 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA10[7:0]			R
0x70	00000000	Operand 10 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA11[7:0]			R
0x71	00000000	Operand 11 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA12[7:0]			R
0x72	00000000	Operand 12 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA13[7:0]			R
0x73	00000000	Operand 13 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA14[7:0]			R
0x74	00000000	Operand 14 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_LENGTH[4:0]			R
0x75	00000000	xxxxx - The total number of bytes (including header byte) that were received into buffer 2	
CEC_RX_RDY2			R
0x76	0000000	CEC_RX_RDY2 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY2 before another message can be received in receiver frame buffer 2. 0 - No CEC frame available in buffer 2 1 - A CEC frame is available in buffer 2	
CEC_RX_RDY1			R
0x76	0000000	CEC_RX_RDY1 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY1 before another message can be received in receiver frame buffer 1. 0 - No CEC frame available in buffer 1 1 - A CEC frame is available in buffer 1	

Reg	Bits	Description
CEC_RX_RDY0		R
0x76	0000000<u>0</u>	CEC_RX_RDY0 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY0 before another message can be received in receiver frame buffer 0. 0 - No CEC frame available in buffer 0 1 - A CEC frame is available in buffer 0
CEC_USE_ALL_BUFS		R/W
0x77	0000000<u>0</u>	Control to enable supplementary receiver frame buffers. 0 - Use only buffer 0 to store CEC frames 1 - Use all 3 buffers to stores the CEC frames
CEC_WAKE_OPCODE0[7:0]		R/W
0x78	<u>01101101</u>	CEC_WAKE_OPCODE0 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01101101 - POWER ON xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE1[7:0]		R/W
0x79	<u>10001111</u>	CEC_WAKE_OPCODE1 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 10001111 - GIVE POWER STATUS xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE2[7:0]		R/W
0x7A	<u>10000010</u>	CEC_WAKE_OPCODE2 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 10000010 - ACTIVE SOURCE xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE3[7:0]		R/W
0x7B	<u>00000100</u>	CEC_WAKE_OPCODE3 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 00000100 - IMAGE VIEW ON xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE4[7:0]		R/W
0x7C	<u>00001101</u>	CEC_WAKE_OPCODE4 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 00001101 - TEXT VIEW ON xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE5[7:0]		R/W
0x7D	<u>01110000</u>	CEC_WAKE_OPCODE5 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01110000 - SYSTEM AUDIO MODE REQUEST xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE6[7:0]		R/W
0x7E	<u>01000010</u>	CEC_WAKE_OPCODE6 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01000010 - DECK CONTROL xxxxxxxx - User specified OPCODE to respond to
CEC_WAKE_OPCODE7[7:0]		R/W
0x7F	<u>01000001</u>	CEC_WAKE_OPCODE7 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01000001 - PLAY xxxxxxxx - User specified OPCODE to respond to

2.7 AVLINK MAP

Reg	Bits	Description	
AVL_TX_FRAME_MODE[1:0]			R/W
0x00	000000<u>00</u>	AV.link frame mode transmission. 00 - mode 1 01 - mode 2 10 - mode 3 11 - Reserved	
AVL_TX_FRAME_HEADER[7:0]			R/W
0x01	<u>00000000</u>	Header block of the transmitted frame. Note the size of the header block varies for different frame modes. mode 1 - TX_FRAME_HEADER[4:0], 5-bit header. mode 2 - TX_FRAME_HEADER[7:0], 8-bit header mode 3 - TX_FRAME[2:0], 3-bit Application ID	
AVL_TX_FRAME_DATA0[7:0]			R/W
0x02	<u>00000000</u>	Transmitted frame data block 0. There data blocks can contain the signal quality bits, the command block and the application bits for the various frame modes of AV.link operation. The datablock can be up to 12 bytes of data.	
AVL_TX_FRAME_DATA1[7:0]			R/W
0x03	<u>00000000</u>	Transmitted frame data block 1	
AVL_TX_FRAME_DATA2[7:0]			R/W
0x04	<u>00000000</u>	Transmitted frame data block 2	
AVL_TX_FRAME_DATA3[7:0]			R/W
0x05	<u>00000000</u>	Transmitted frame data block 3	
AVL_TX_FRAME_DATA4[7:0]			R/W
0x06	<u>00000000</u>	Transmitted frame data block 4	
AVL_TX_FRAME_DATA5[7:0]			R/W
0x07	<u>00000000</u>	Transmitted frame data block 5	
AVL_TX_FRAME_DATA6[7:0]			R/W
0x08	<u>00000000</u>	Transmitted frame data block 6	
AVL_TX_FRAME_DATA7[7:0]			R/W
0x09	<u>00000000</u>	Transmitted frame data block 7	
AVL_TX_FRAME_DATA8[7:0]			R/W
0x0A	<u>00000000</u>	Transmitted frame data block 8	
AVL_TX_FRAME_DATA9[7:0]			R/W
0x0B	<u>00000000</u>	Transmitted frame data block 9	
AVL_TX_FRAME_DATA10[7:0]			R/W
0x0C	<u>00000000</u>	Transmitted frame data block 10	
AVL_TX_FRAME_DATA11[7:0]			R/W
0x0D	<u>00000000</u>	Transmitted frame data block 11	
AVL_TX_FRAME_ECT			R/W
0x0E	0000000<u>0</u>	AV.link Extended Command Table (ECT) bit in the frame to be transmitted. The ECT bit is the ninth bit in the command block and is intended as an escape to an Extended Command Table for future use. 0 - For future use 1 - Specifies that the operand is specified in the present command table	
AVL_TX_FRAME_LENGTH[7:0]			R/W
0x0F	<u>00000000</u>	Message size of the transmitted frame. This is the number of byte in the outgoing message including the header. Caters for a maximum frame size of 100 bits for mode 3. xxxxxxxx - Total number of bytes (including header byte) to be sent	

Reg	Bits	Description	
AVL_TX_ENABLE			R/W
0x10	0000000<u>0</u>	This bit enables the TX section. When set to 1 it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is completed this bit is automatically reset to 0. If it is manually set to 0 during a message transmission it may terminate the transmission depending on what stage of the transmission process has been reached. If the message transmission is sill in the 'signal free time' stage the message transmission will be terminated. If data transmission has begun then the transmission will continue until the message is fully sent, or until an error condition occurs. 0 - Transmitter mode disabled 1 - Transmitter mode enabled and message transmission started	
AVL_TX_SFT3[3:0]			R/W
0x11	0<u>0011</u>100	Signal Free Time for transmission retry of mode 1 frames.	
AVL_TX_RETRY[2:0]			R/W
0x11	00011<u>100</u>	The number of times the AV.link TX should try to retransmit the message if an error condition is encountered. 100 - Try to retransmit the message 4 times if an error occurs xxx - Try to retransmit the message xxx times if an error occurs	
AVL_TX_SFT7[3:0]			R/W
0x12	<u>0111</u>0101	Signal Free Time if the device is a new initiator for mode 2 and mode 3 frames.	
AVL_TX_SFT5[3:0]			R/W
0x12	0111<u>0101</u>	Signal Free Time for transmission retry of mode 2 and mode 3 frames.	
AVL_TX_SFT9[3:0]			R/W
0x13	0000<u>1001</u>	Signal Free Time if the device transmits a next frame immediately after its previous frame for mode 2 and mode 3 frames.	
AVL_TX_NACK_COUNTER[3:0]			R
0x14	0000<u>0000</u>	The number of times that the NACK error condition was encountered while trying to send the current message. This register is reset to 0b0000 when AVL_TX_ENABLE is set to 1. 0000 - No error condition xxxx - The number of times the NACK error condition was encountered	
AVL_RX_FRAME_MODE[1:0]			R
0x15	000000<u>00</u>	Frame mode of the received frame. 00 - mode 1 01 - mode 2 10 - mode 3 11 - Reserved	
AVL_RX_FRAME_HEADER[7:0]			R
0x16	<u>00000000</u>	Received frame header	
AVL_RX_FRAME_DATA0[7:0]			R
0x17	<u>00000000</u>	Received frame data block 0	
AVL_RX_FRAME_DATA1[7:0]			R
0x18	<u>00000000</u>	Received frame data block 1	
AVL_RX_FRAME_DATA2[7:0]			R
0x19	<u>00000000</u>	Received frame data block 2	
AVL_RX_FRAME_DATA3[7:0]			R
0x1A	<u>00000000</u>	Received frame data block 3	
AVL_RX_FRAME_DATA4[7:0]			R
0x1B	<u>00000000</u>	Received frame data block 4	
AVL_RX_FRAME_DATA5[7:0]			R
0x1C	<u>00000000</u>	Received frame data block 5	
AVL_RX_FRAME_DATA6[7:0]			R
0x1D	<u>00000000</u>	Received frame data block 6	

Reg	Bits	Description	
AVL_RX_FRAME_DATA7[7:0]			R
0x1E	00000000	Received frame data block 7	
AVL_RX_FRAME_DATA8[7:0]			R
0x1F	00000000	Received frame data block 8	
AVL_RX_FRAME_DATA9[7:0]			R
0x20	00000000	Received frame data block 9	
AVL_RX_FRAME_DATA10[7:0]			R
0x21	00000000	Received frame data block 10	
AVL_RX_FRAME_DATA11[7:0]			R
0x22	00000000	Received frame data block 11	
AVL_RX_FRAME_ECT			R
0x23	0000000[0]	AV.link ECT bit in frame received	
AVL_RX_FRAME_LENGTH[7:0]			R
0x24	00000000	Received message size (Number of data block + header)	
AVL_RX_ENABLE			R/W
0x25	0000000[0]	Receiver mode enable 0 - Receiver mode disabled 1 - Receiver mode enabled	
AVL_LOGICAL_ADDRESS_MASK_2			R/W
0x26	0[0]010000	Mask bit for logical address 2 0 - Logical address 2 disabled 1 - Logical address 2 enabled	
AVL_LOGICAL_ADDRESS_MASK_1			R/W
0x26	00[0]10000	Mask bit for logical address 1 0 - Logical address 1 disabled 1 - Logical address 1 enabled	
AVL_LOGICAL_ADDRESS_MASK_0			R/W
0x26	000[1]0000	Mask bit for logical address 0 0 - Logical address 0 disabled 1 - Logical address 0 enabled	
AVL_ERROR_REPORT_MODE			R/W
0x26	0001[0]000	Error reporting mode 0 - Report short bit errors 1 - Report short and long bit errors	
AVL_ERROR_DET_MODE			R/W
0x26	00010[0]00	Error detection mode 0 - If any short bit period error, except the start bit is detected, the AV.link immediately drives the AV.link line low for 7.2ms. 1 - If only a short bit period error is detected on data blocks of a directly addressed message or a broadcast message, the AV.link controller immediately drives the AV.link line low for 7.2ms.	
AVL_FORCE_NACK			R/W
0x26	000100[0]0	Force NO-ACK Control Setting this bit forces the AV.link controller to not acknowledge any received messages. 0 - Acknowledge received messages 1 - Do acknowledge received messages	
AVL_FORCE_IGNORE			R/W
0x26	0001000[0]	Force Ignore Control. Setting this bit will force the CEC controller to ignore any directly addressed messages to the AV.link device. Normal operation will be maintained for the broadcast message. 0 - Do not ignore directly address messages. 1 - Ignore any directly addressed message.	

Reg	Bits	Description	
AVL_AVLINK_POWER_UP			R/W
0x27	0000000<u>0</u>	Power Mode of AV.link module 0 - Power down the AV.link module 1 - Power up the AV.link module	
AVL_GLITCH_FILTER_CTRL[5:0]			R/W
0x28	00<u>000111</u>	Glitch filter control for the AV.link input. The AV.link input signal is sampled by the input clock (XTAL clock). AVL_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths less than the minimum specified width are considered glitches and will be removed by the filter. 000000 - Disable the glitch filter 000001 - Filter out pulses with width less than 1 clock cycle 000010 - Filter out pulses with width less than 2 clock cycles - ... 000111 - Filter out pulses with width less than 7 clock cycles - ... 111111 - Filter out pulses with width less than 63 clock cycles	
AVL_FORCE_ERROR			R/W
0x29	000000<u>0</u>0	Force the next state of the AV.link controller to error if this bit is set to 1. 0 - Do not force the next state to error 1 - Force the next state to error	
AVL_SOFT_RESET			SC
0x29	0000000<u>0</u>	AV.link module software reset. 0 - No function 1 - Reset the AV.link module	
AVL_LOGICAL_ADDRESS1[3:0]			R/W
0x2A	<u>1111</u>1111	Logical address 1 (mode 2). This address must be enabled by setting AVL_LOGICAL_ADDRESS_MASK[1] to 0b1 1111 - Default value xxxx - User specified logical address	
AVL_LOGICAL_ADDRESS0[3:0]			R/W
0x2A	1111<u>1111</u>	Logical address 0 (mode 2). This address must be enabled by setting AVL_LOGICAL_ADDRESS_MASK[0] to 0b1 1111 - Default value xxxx - User specified logical address	
AVL_LOGICAL_ADDRESS2[3:0]			R/W
0x2B	0000<u>1111</u>	Logical address 2 (mode 2). This address must be enabled by setting AVL_LOGICAL_ADDRESS_MASK[2] to 0b1 1111 - Default value xxxx - User specified logical address	
AVL_ST_TOTAL_H[7:0]			R/W
0x2C	<u>00001111</u>	AV.link start bit total period. Typically 9ms	
AVL_ST_TOTAL_L[7:0]			R/W
0x2D	<u>10111011</u>	AV.link start bit total period. Typically 9ms	
AVL_ST_TOTAL_MIN_H[7:0]			R/W
0x2E	<u>00001110</u>	AV.link minimum start bit period (MSB). This period is 8.6ms but keep 0.1ms for default margin	
AVL_ST_TOTAL_MIN_L[7:0]			R/W
0x2F	<u>11011011</u>	AV.link minimum start bit period (LSB). This period is 8.6ms but keep 0.1ms for default margin	
AVL_ST_TOTAL_MAX_H[7:0]			R/W
0x30	<u>00010000</u>	AV.link maximum start bit period (MSB). This period is 9.4ms but keep 0.1ms for default margin	
AVL_ST_TOTAL_MAX_L[7:0]			R/W
0x31	<u>10011011</u>	AV.link maximum start bit period (LSB). This period is 9.4ms, keep 0.1ms for default margin	
AVL_ST_LOW_H[7:0]			R/W
0x32	<u>00001100</u>	AV.link start bit low period (MSB) This period is 7.4ms	
AVL_ST_LOW_L[7:0]			R/W
0x33	<u>11101111</u>	AV.link start bit low period (LSB) This period is 7.4ms	

Reg	Bits	Description	
AVL_ST_LOW_MINIMUM_H[7:0]			R/W
0x34	00001100	AV.link start bit low minimum period (MSB) This period is 7ms, keep 0.1ms for default	
AVL_ST_LOW_MINIMUM_L[7:0]			R/W
0x35	00001111	AV.link start bit low minimum period (LSB) This period is 7ms, keep 0.1ms for default	
AVL_ST_LOW_MAXIMUM_H[7:0]			R/W
0x36	00001101	AV.link start bit low maximum period (MSB) This period is 7.8ms, keep 0.1ms for default	
AVL_ST_LOW_MAXIMUM_L[7:0]			R/W
0x37	11001111	AV.link start bit low maximum period (LSB) This period is 7.8ms, keep 0.1ms for default	
AVL_BIT_TOTAL_H[7:0]			R/W
0x38	00001000	AV.link nominal bit period (MSB) This period is 4.8ms (mean of 4.1ms and 5.5ms)	
AVL_BIT_TOTAL_L[7:0]			R/W
0x39	01100100	AV.link nominal bit period (LSB) This period is 4.8ms (mean of 4.1ms and 5.5ms)	
AVL_BIT_TOTAL_MIN_H[7:0]			R/W
0x3A	00000110	AV.link minimum bit period (MSB) This period is 4.1ms, keep default 0.1ms margin	
AVL_BIT_TOTAL_MIN_L[7:0]			R/W
0x3B	11111110	AV.link minimum bit period (LSB) This period is 4.1ms, keep default 0.1ms margin	
AVL_BIT_TOTAL_MAX_H[7:0]			R/W
0x3C	00001001	AV.link maximum bit period (MSB) This period is 5.5ms, keep 0.1ms default margin	
AVL_BIT_TOTAL_MAX_L[7:0]			R/W
0x3D	11001010	AV.link maximum bit period (LSB) This period is 5.5ms, keep 0.1ms default margin	
AVL_BIT_LOW_ONE_H[7:0]			R/W
0x3E	00000010	AV.link logical "1" nominal data bit low period (MSB) This period is 1.2ms (mean of 0.8ms and 1.6ms)	
AVL_BIT_LOW_ONE_L[7:0]			R/W
0x3F	00011001	AV.link logical "1" nominal data bit low period (LSB) This period is 1.2ms (mean of 0.8ms and 1.6ms)	
AVL_BIT_LOW_ONE_MIN_H[7:0]			R/W
0x40	00000001	AV.link logical "1" data bit low minimum period (MSB) This period is 0.8ms, use 0.1ms margin	
AVL_BIT_LOW_ONE_MIN_L[7:0]			R/W
0x41	00111001	AV.link logical "1" data bit low minimum period (LSB) This period is 0.8ms, use 0.1ms margin	
AVL_BIT_LOW_ONE_MAX_H[7:0]			R/W
0x42	00000010	AV.link logical "1" data bit low maximum period (MSB) This period is 1.6ms, use 0.1ms margin	
AVL_BIT_LOW_ONE_MAX_L[7:0]			R/W
0x43	11111001	AV.link logical "1" data bit low maximum period (LSB) This period is 1.6ms, use 0.1ms margin	
AVL_BIT_LOW_ZERO_H[7:0]			R/W
0x44	00000101	AV.link logical "0" nominal data bit low period (MSB) This period is 3ms (mean of 2.6ms and 3.4ms)	
AVL_BIT_LOW_ZERO_L[7:0]			R/W
0x45	00111110	AV.link logical "0" nominal data bit low period (LSB) This period is 3ms (mean of 2.6ms and 3.4ms)	
AVL_BIT_LOW_MAX_H[7:0]			R/W
0x46	00000101	AV.link logical "0" data bit low maximum period (MSB) This period is 3.4ms	
AVL_BIT_LOW_MAX_L[7:0]			R/W
0x47	11110001	AV.link logical "0" data bit low maximum period (LSB) This period is 3.4ms	

Reg	Bits	Description	
AVL_BIT_LOW_ZERO_MIN_H[7:0]			R/W
0x48	00000100	AV.link logical "0" minimum low data bit period (MSB) This period is 2.6ms	
AVL_BIT_LOW_ZERO_MIN_L[7:0]			R/W
0x49	10001011	AV.link logical "0" minimum low data bit period (LSB) This period is 2.6ms	
AVL_SAMPLE_TIME_H[7:0]			R/W
0x4A	00000011	AV.link nominal sampling time (MSB) This period is 2.1ms (mean of 1.7ms and 2.5ms)	
AVL_SAMPLE_TIME_L[7:0]			R/W
0x4B	10101100	AV.link nominal sampling time (LSB) This period is 2.1ms (mean of 1.7ms and 2.5ms)	
AVL_LINE_ERROR_TIME_H[7:0]			R/W
0x4C	00001100	AV.link line error handling time (MSB) This period is 1.5 times the nominal bit period ~ 7.2ms	
AVL_LINE_ERROR_TIME_L[7:0]			R/W
0x4D	10010110	AV.link line error handling time (LSB) This period is 1.5 times the nominal bit period ~ 7.2ms	
AVL_RISE_TIME_H[7:0]			R/W
0x4E	00000000	Rise Time (MSB) This parameter is needed to give allowance to the rising edge of the signal on the AV.link control signal line	
AVL_RISE_TIME_L[7:0]			R/W
0x4F	01110000	Rise Time (LSB) This parameter is needed to give allowance to the rising edge of the signal on the AV.link control signal line	
AVL_BIT_LOW_DETMODE			R/W
0x50	0000000[0]	Error detection mode for data bit low period. If any low bit period of data bit does not meet the AV.link timing requirement, the AV.link section immediately drives the AV.link line low for 7.2ms. 0 - Disable error mode detection 1 - Enable error mode detection.	
AVL_TIMING_MAN			R/W
0x51	0000000[0]	Select between hardcoded values and the manual values in of the AV.link timing registers. 0 - Select hardcoded values for timing registers and the AV.link clock divider based on XTAL frequency. 1 - Use the I2C values for the timing registers and the clock divider.	
AVL_MODE00_HEADER_VALIDATE			R/W
0x52	0000000[0]	Enable the validation of header for mode 0 frames 0 - Disable validation of the header for mode 0 frames 1 - Enable validation of the header for mode 0 frames	
AVL_PROP_DELAY_H[7:0]			R/W
0x53	00000000	Propagation Delay (MSB) Programmable propagation delay for signal change on AVLINK_OUT to reflect on AVLINK_IN	
AVL_PROP_DELAY_L[7:0]			R/W
0x54	00000000	Propagation Delay (LSB) Programmable propagation delay for signal change on AVLINK_OUT to reflect on AVLINK_IN	
AVL_RX_DEVICE_CAPABILITY_ARB[5:0]			R/W
0x55	00[111111]	The values of the arbitration type bits that corresponds to the receiver for mode 0 frames	
AVL_TX_RECEIVED_ARB[5:0]			R
0x56	00[000000]	Received values for the arbitration type bits for mode 0 frames	
AVL_RX_EXPECT_FRAME_LENGTH[7:0]			R/W
0x58	01111100	Programmable control to set the frame length for the receiver to receive for mode 2 frames.	

2.8 SDP IO MAP

Reg	Bits	Description	
SDP_TRI_MEMORY_IF			R/W
0x29	00000000	This control is used to tristate memory interface pins. Setting this bit tristates the interface address, data control, data strobe and mask lines. 0 - Tristates memory interface pins 1 - Does not tristate memory interface pins	
SDP_RING_RED_EN			R/W
0x51	00000000	Enable ringing reduction block to remove ringing artifact from around sharp edges 0 - Disables ringing reduction block 1 - Enables ringing reduction block	
SDP_RING_RED_LEVEL[6:0]			R/W
0x51	00000000	Level control for ringing reduction algorithm. Higher values give more dramatic ringing reduction 0000000 - No ringing reduction	
SDP_MEM_SM_RESET			SC
0x60	00000000	A control to reset the memory controller state machine. This allows user allows to change parameters and re-initialize without full reset. This is a self clearing control. 0 - Don't reset memory controller state machine. 1 - Reset memory controller state machine. (self clearing bit)	
SDP_MAN_SFL_STANDARD[3:0]			R/W
0x66	00000001	Manual SFL output format used if SDP_MAN_SFL_STD_EN set to 1. 0000 - NTSC-MJ 0001 - Reserved 0010 - NTSC-MJ 0011 - NTSC-MJ 0100 - PAL-M 0101 - NTSC-MJ 0110 - Reserved 0111 - NTSC-MJ 1000 - PAL-CombN 1001 - PAL-BGHID/NTSC443 1010 - PAL-BGHID/NTSC443 1011 - PAL-BGHID/NTSC443 1100 - PAL-CombN 1101 - PAL-BGHID/NTSC443 1110 - PAL-BGHID/NTSC443 1111 - PAL-BGHID/NTSC443	
SDP_MAN_SFL_STD_EN			R/W
0x66	00000001	A control to enable manual standard selection for SFL 0 - Automatically configuration of SFL output to convert all 50 Hz inputs (including SECAM) to PAL-BGHID and all 60 Hz to inputs to NTSC-MJ. 1 - Configure SFL output to convert input to standard given by SDP_MAN_SFL_STDconverted to PAL-BGHID and 60Hz SECAM is converted to NTSC-MJ.	
SDP_AUTO_SFL_STD_EN			R/W
0x66	00000001	A control to enable automatic standard selection for SFL 0 - Uses SDP_MAN_SFL_STD, dependant on SDP_MAN_SFL_STD_EN 1 - Automatic configuration of SFL output to convert all 50Hz inputs to PAL-BGHID and all 60Hz inputs to NTSC-MJ	
SDP_SFL_EN			R/W
0x67	00000100	A control to output the SFL signal on the SFL pin. Valid for SD core modes only. 0 - Disable SFL Signal 1 - Enable SFL signal	
SDP_SFL_INV_PSW			R/W
0x67	00000100	A control to invert PAL switch in SFL stream. 0 - Do not invert PAL switch in SFL stream 1 - Invert PAL switch in SFL stream, (compatibility with some older video encoders)	

Reg	Bits	Description
SDP_FREEZE_FRAME		R/W
0x6F	0000000<u>0</u>	A control to continously loop out a frame of video data from the TBC block. This feature will effectively allow the image to be paused on screen. When this bit is set, new data will not be updated into the Frame memory. This bit is only valid when frame TBC is enabled. 0 - Don't freeze frame TBC input 1 - Freeze frame TBC input
SDP_SDRAM_MEM		R/W
0x6F	0000000<u>0</u>	A control to configure the memory controller for either SDR or DDR interface. Refer to the Hardware Manual for further memory interface configuration. 0 - Select DDR external memory 1 - Select SDR external memory
SDP_AUX_EAV_POS_ADJ[11:0]		R/W
0x8C 0x8D	0000<u>0000</u> <u>00000000</u>	A control to adjust the EAV position in the auxiliary pixel bus datastream. This a 2s complement control. To be used in parallel modes only. 0x000 - Default position
SDP_AUX_SAV_POS_ADJ[11:0]		R/W
0x8E 0x8F	0000<u>0000</u> <u>00000000</u>	A control to adjust the SAV position in the auxiliary pixel bus datastream. This a 2s complement control. To be used in parallel modes only. 0x000 - Default position
SDP_EAV_POS_ADJ[11:0]		R/W
0x90 0x91	0000<u>0000</u> <u>00000000</u>	A control to adjust the EAV position from its default position. This a 2s complement control. 000000000000 - EAV code default position xxxxxxxxxxxx - EAV code position adjustment
SDP_SAV_POS_ADJ[11:0]		R/W
0x92 0x93	0000<u>0000</u> <u>00000000</u>	A control to adjust the SAV position from its default position. This a 2s complement control. 000000000000 - SAV code default position xxxxxxxxxxxx - SAV code adjustment
SDP_HS_BEG_ADJ[11:0]		R/W
0x94 0x95	0000<u>0000</u> <u>00000000</u>	The SDP_HS_BEG_ADJ[11:0] and SDP_HS_WIDTH[11:0] bits allow the user to freely position the HSync signal applied to the output pin within the video line. The values in the SDP_HS_BEG_ADJ[11:0] and SDP_HS_WIDTH[11:0] bits are measured in pixel units from the default falling edge position of the HSync. Using both values, the user can program both the position and the width of the HSync output signal. The SDP_HS_BEG_ADJ[11:0] adjusts the leading and trailing edge positions, hence adjusting the HSync pulse. The number applied to the register offsets the HSync pulse position with respect to the default value. The number is a twos complement value, which allows both positive and negative edge movement. 0x000 - Default value
SDP_HS_WIDTH[11:0]		R/W
0x96 0x97	0000<u>0000</u> <u>00100000</u>	The SDP_HS_WIDTH[11:0] bits allow the user to freely adjust the width of the HSync pulse within the video line. The values in the SDP_HS_WIDTH[11:0] bits are measured in pixel units from the falling edge of HSync. The position of this edge is controlled by placing an unsigned binary number into the SDP_HS_BEG_ADJ[11:0] bits. 0x020 - Default value (unsigned control)
SDP_DE_H_BEG_ADJ[11:0]		R/W
0x98 0x99	0000<u>0000</u> <u>00000000</u>	Adjust SDP DE horizontal begin position versus default, 2s complement 0x000 - Default value
SDP_DE_H_END_ADJ[11:0]		R/W
0x9A 0x9B	0000<u>0000</u> <u>00000000</u>	Adjust SDP DE horizontal end position versus default, 2s complement 0x000 - Default value
SDP_VSF_H_BEG_ADJ[11:0]		R/W
0x9C 0x9D	0000<u>0000</u> <u>00000000</u>	The SDP_VSF_H_BEG_ADJ[11:0] bits adjust the VS/FIELD output relative to the HSync position. The values are measured in pixel units from the falling edge of HSync. This control is used when the VSync and Field outputs are coincident with HSync. The position of the VSync and Field relative to the HSync is controlled by placing a two's complement number into the SDP_VSF_H_BEG_ADJ[11:0] bits. 0x000 - Default value
SDP_VSF_H_MID_ADJ[11:0]		R/W
0x9E 0x9F	0000<u>0000</u> <u>00000000</u>	The SDP_VSF_H_MID_ADJ[11:0] bits adjust the SDP VS/FIELD output relative to the HSync position within the video line. The values are measured in pixel units from the falling edge of HSync. This control is used when the VSync or Field changes approximately midway between HSyncs. The position of the VSync and Field relative to the HSync is controlled by placing a twos complement number into the SDP_VSF_H_MID_ADJ[11:0] bits. 0x000 - Default value

Reg	Bits	Description	
SDP_V_BEG_O_ADJ[5:0]			R/W
0xA0	00000100	Adjust SDP 656 code V bit low to high transition relative to default, only +ve recommended, 2s complement 000100 - Default value	
SDP_V_BEG_E_ADJ[5:0]			R/W
0xA1	00000100	Adjust SDP 656 code V bit low to high transition relative to default.This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_V_END_O_ADJ[5:0]			R/W
0xA2	00000100	Adjust SDP 656 code V bit high to low transition relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_V_END_E_ADJ[5:0]			R/W
0xA3	00000100	Adjust SDP 656 code V bit high to low transition relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_F_TOG_O_ADJ[5:0]			R/W
0xA4	00000100	Adjust SDP 656 code F bit transition relative to default.This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_F_TOG_E_ADJ[5:0]			R/W
0xA5	00000100	Adjust SDP 656 code F bit transition relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_FLD_TOG_O_ADJ[5:0]			R/W
0xA6	00000100	Adjust SDP field pin transition relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_FLD_TOG_E_ADJ[5:0]			R/W
0xA7	00000100	Adjust SDP field pin transition relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_VS_V_BEG_O_ADJ[5:0]			R/W
0xA8	00000100	Adjust SDP VSync pin begin line relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_VS_V_BEG_E_ADJ[5:0]			R/W
0xA9	00000100	Adjust SDP VSync pin begin line relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_VS_V_END_O_ADJ[5:0]			R/W
0xAA	00000100	Adjust SDP VSync pin end line relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_VS_V_END_E_ADJ[5:0]			R/W
0xAB	00000100	Adjust SDP VSync pin end line relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_DE_V_BEG_O_ADJ[5:0]			R/W
0xAC	00000100	Adjust SDP DE pin begin line relative to default.This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	
SDP_DE_V_BEG_E_ADJ[5:0]			R/W
0xAD	00000100	Adjust SDP DE pin begin line relative to default.This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value	

Reg	Bits	Description
SDP_DE_V_END_O_ADJ[5:0]		R/W
0xAE	00000100	Adjust SDP DE pin end line relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value
SDP_DE_V_END_E_ADJ[5:0]		R/W
0xAF	00000100	Adjust SDP DE pin end line relative to default. This is a 2's complement adjustment control, only positive adjustment is recommended. 000100 - Default value
SDP_VBLANK_EN		R/W
0xB0	11000000	A control to insert blanking codes or pass-through decoded video data during vertical blanking interval. 0 - Pass through decoded video data during vertical blanking interval 1 - Insert blanking codes during vertical blanking interval (location equal to V bit)
SDP_HBLANK_EN		R/W
0xB0	11000000	A control to insert blanking codes or pass-through decoded video data during horizontal blanking interval. 0 - Pass through decoded video data during horizontal blanking interval 1 - Insert blanking codes during horizontal blanking interval (location equal to H bit)
SDP_FHE_TOG_INV		R/W
0xB0	11000000	A control to change the default field transition position for the field signal for even fields. The field transition can be at the beginning or in the middle of the line. 0 - Use default horizontal transition position for field signal on even fields 1 - Swap horizontal transition position for field signal on even fields. Swap between beginning of the line and middle of the line
SDP_FHO_TOG_INV		R/W
0xB0	11000000	A control to change the default field transition position for the field signal for odd fields. The field transition can be at the beginning or in the middle of the line. 0 - Use default horizontal transition position for field signal on odd fields 1 - Swap horizontal transition position for field signal on odd fields. Swap between beginning of the line and middle of the line
SDP_VHE_END_INV		R/W
0xB0	11000000	A control to change the default field transition and end of Vsync positions for the VSync signal for even fields. The field transition can be at the beginning or in the middle of the line. 0 - Use default horizontal field transition and end of Vsync positions for VSync signals on even fields. 1 - Swap horizontal field transitionand end of Vsync positions for Vsync signals on even fields. Swap between beginning and middle of the line.
SDP_VHO_END_INV		R/W
0xB0	11000000	A control to change the default field transition and end of Vsync positions for the VSync signal for odd fields. The field transition can be at the beginning or in the middle of the line. 0 - Use default horizontal field transition and end of Vysnc positions for VSync signals on odd fields. 1 - Swap horizontal field transition and end of Vsync positions for Vsync on odd fields. Swap between the beginning and middle of the line.
SDP_VHE_BEG_INV		R/W
0xB0	11000000	A control to change the default field transition and begining of Vsync positions for the VSync signal for even fields. The field transition can be at the beginning or in the middle of the line. 0 - Use default horizontal field transition and beginning of Vsync positions for VSync signals on even fields. 1 - Swap horizontal field transition position and beginning of VSync postions for Vsync signals on even fields. Swap between the beginning and middle of the line
SDP_VHO_BEG_INV		R/W
0xB0	11000000	A control to change the default field transition and begining of Vsync positions for the VSync signal for odd fields. The field transition can be at the beginning or in the middle of the line. 0 - Use default horizontal field transition and beginning of Vsync positions for VSync signals on odd fields. 1 - Swap horizontal field transition position and beginning of VSync postions for Vsync signals on odd fields. Swap between the beginning and middle of the line
SDP_V_BIT_POL		R/W
0xB1	01111101	A control to change polarity of V bit 0 - Inverted V bit polarity 1 - Default V bit polarity
SDP_F_BIT_POL		R/W
0xB1	01111101	A control to change polarity of FIELD bit 0 - Inverted FIELD bit polarity 1 - Default FIELD bit polarity

Reg	Bits	Description	
SDP_DE_POL			R/W
0xB1	01111101	A control to change polarity of DE 0 - Inverted DE polarity 1 - Default DE polarity	
SDP_CS_POL			R/W
0xB1	01111101	A control to change polarity of HS/CS 0 - Inverted HS/CS polarity 1 - Default HS/CS polarity	
SDP_FLD_POL			R/W
0xB1	01111101	A control to change polarity of FIELD/DE 0 - Inverted FIELD/DE pin polarity 1 - Default FIELD/DE pin polarity	
SDP_VS_POL			R/W
0xB1	01111101	A control to change polarity of VS/FIELD 0 - Default VS/FIELD pin polarity 1 - Inverted VS/FIELD pin polarity	
SDP_HS_POL			R/W
0xB1	01111101	A control to change polarity of HS/CS 0 - Inverted HS/CS pin polarity 1 - Default HS/CS pin polarity	
SDP_EAV_EN			R/W
0xB2	01101100	A control to enable the insertion of EAV codes into the digital data-stream for SD core modes. 0 - Do not insert EAV codes 1 - Insert EAV codes	
SDP_SAV_EN			R/W
0xB2	01101100	A control to enable the insertion of SAV codes into the digital data-stream for SD core modes. 0 - Do not insert SAV codes 1 - Insert SAV codes	
SDP_FRZ_F_BIT			R/W
0xB2	01101100	0 - Don't freeze F bit, only valid for SDP modes 1 - Freeze F bit at INV (SDP_F_BIT_POL)	
SDP_REPL_ANC_DATA			R/W
0xB3	00100000	A control to enable replication anncillary data on all channels 0 - Ancillary data on Y/G channel only (if CLK is fast enough) 1 - Replicate SDP ancillary data on all channels	
SDP_SPLIT_ANC_DATA			R/W
0xB3	00100000	A control to enable splitting ancillary data across channels. 0 - Don't split SDP ancillary data across channels. Overwritten by SDP_REPL_ANC_DATA 1 - Split SDP ancillary data across channels	
SDP_SPLIT_AV_CODE			R/W
0xB3	00100000	A control to enable splitting SDP SAV/EAV codes across all channels 0 - Don't split SDP SAV/EAV codes across all channels. 1 - Split SDP SAV/EAV codes across channels	
SDP_V_BEG_TRICK_O_ADJ[5:0]			R/W
0xB4	00000100	Adjust SDP 656 code V bit low to high transition in VCR trick modes relative to default. This is a 2's complement control, only positive adjustments are recommended. Adjustment applied when a VCR trick modes is detected. 000100 - Default value	
SDP_V_BEG_TRICK_E_ADJ[5:0]			R/W
0xB5	00000100	Adjust SDP 656 code V bit low to high transition in VCR trick modes relative to default. This is a 2's complement control, only positive adjustments are recommended. Adjustment applied when a VCR trick modes is detected. 000100 - Default value	
SDP_V_END_TRICK_O_ADJ[5:0]			R/W
0xB6	00000100	Adjust SDP 656 code V bit high to low transition in VCR trick modes relative to default. This is a 2's complement control, only positive adjustments are recommended. Adjustment applied when a VCR trick modes is detected. 000100 - Default value	

Reg	Bits	Description
SDP_V_END_TRICK_E_ADJ[5:0]		R/W
0xB7	00000100	Adjust SDP 656 code V bit high to low transition in VCR trick modes relative to default. This is a 2's complement control, only positive adjustments are recommended. Adjustment applied when a VCR trick modes is detected. 000100 - Default value
SDP_F_TOG_TRICK_O_ADJ[5:0]		R/W
0xB8	00000100	Adjust SDP 656 code F bit transition in VCR trick modes relative to default. This is a 2's complement control, only positive adjustments are recommended. Adjustment applied when a VCR trick modes is detected. 000100 - Default value
SDP_F_TOG_TRICK_E_ADJ[5:0]		R/W
0xB9	00000100	Adjust SDP 656 code F bit transition in VCR trick modes relative to default. This is a 2's complement control, only positive adjustments are recommended. Adjustment applied when a VCR trick modes is detected. 000100 - Default value
SDP_AUX_V_BEG_O_ADJ[5:0]		R/W
0xC2	00000100	A control to adjust the 656 code V bit low to high transition on the odd field relative to default position in the auxiliary pixel bus datastream. This is a 2s complement control. Only positive adjustments recommended. 000100 - Default value
SDP_AUX_V_BEG_E_ADJ[5:0]		R/W
0xC3	00000100	A control to adjust the 656 code V bit low to high transition on the even field relative to default position in the auxiliary pixel bus datastream. This is a 2s complement control. Only positive adjustments recommended. 000100 - Default value
SDP_AUX_V_END_O_ADJ[5:0]		R/W
0xC4	00000100	A control to adjust the 656 code V bit high to low transition on the odd field relative to default position in the auxiliary pixel bus datastream. This is a 2s complement control. Only positive adjustments are recommended. 000100 - Default value
SDP_AUX_V_END_E_ADJ[5:0]		R/W
0xC5	00000100	A control to adjust the 656 code V bit high to low transition on the even field relative to default position in the auxiliary pixel bus datastream. This is a 2s complement control. Only positive adjustments are recommended. 000100 - Default value
SDP_AUX_F_TOG_O_ADJ[5:0]		R/W
0xC6	00000100	A control to adjust the 656 code F bit transition position on the odd field relative to default in the auxiliary pixel bus datastream. This is a 2s complement control. Only positive adjustments are recommended. 000100 - Default value
SDP_AUX_F_TOG_E_ADJ[5:0]		R/W
0xC7	00000100	A control to adjust the 656 code F bit transition position on the even field relative to default in the auxiliary pixel bus datastream. This is a 2s complement control. Only positive adjustments are recommended. 000100 - Default value
SDP_AUX_V_BIT_POL		R/W
0xC8	11101011	A control to invert the V bit polarity inserted in the auxiliary pixel bus datastream. This should be used in parallel modes only. 0 - Inverted V bit polarity 1 - Default V bit polarity
SDP_AUX_F_BIT_POL		R/W
0xC8	11101011	A control to invert the F bit polarity inserted in the auxiliary pixel bus datastream. This should be used in parallel modes only. 0 - Inverted F bit polarity 1 - Default F bit polarity
SDP_ANC_MAIN_EN		R/W
0xC8	11101011	A control to enable the ancillary data on the main pixel bus datastream. Note only one pixelbus, main or auxiliary, should be enabled for ancillary data at a time. 0 - Ancillary data if enabled does not come on main channel 1 - Ancillary data if enabled comes on main channel
SDP_ANC_AUX_EN		R/W
0xC8	11101011	A control to enable the ancillary data on the auxiliary pixel bus datastream. Note only one pixelbus, main or auxiliary, should be enabled for ancillary data at a time. 0 - Ancillary data if enabled does not come on aux channel 1 - Ancillary data if enabled comes on aux channel

Reg	Bits	Description
SDP_AUX_VBLANK_EN		R/W
0xC8	1110101**1**	A control to select the insertion of blanking codes or decoded video data during the vertical interval (location equal to V bit) for the auxiliary pixel bus datastream. 0 - Pass through decoded video data during vertical blanking interval 1 - Insert blanking codes during vertical blanking interval (location equal to V bit)
SDP_AUX_HBLANK_EN		R/W
0xC8	1110101**1**	A control to select the insertion of blanking codes or decoded video data during the horizontal interval (location equal to H bit) for the auxiliary pixel bus datastream. 0 - Pass through decoded video data during horizontal blanking interval 1 - Insert blanking codes during horizontal blanking interval (location equal to H bit)
SDP_AUX_REPL_AV_CODE		R/W
0xC9	0110**0**1100	A control to select that embedded timing be replicated on the chroma channel on the auxiliary pixel bus. 0 - Output single SAV/EAV codes on auxiliary luma channel only. 1 - Replicate SAV/EAV codes on auxiliary Cr/Cb channel.
SDP_AUX_EAV_EN		R/W
0xC9	0110**1**1100	A control to enable the insertion of EAV codes into the datastream on the auxiliary pixel bus in parallel modes. Note only embedded timing is supported on the auxiliary pixel bus. 0 - Don't insert EAV codes, only valid for SDP modes 1 - Insert EAV codes
SDP_AUX_SAV_EN		R/W
0xC9	0110**1**1100	A control to enable the insertion of SAV codes into the datastream on the auxiliary pixel bus in parallel modes. Note only embedded timing is supported on the auxiliary pixel bus. 0 - Don't insert SAV codes, only valid for SDP modes 1 - Insert SAV codes
SDP_CSC_SCALE		R/W
0xE0	**0**1000111	A control to set CSC gain 0 - CSC scaler set to 1 1 - CSC scaler set to 2
SDP_CSC_AUTO		R/W
0xE0	0**1**000111	A control to select CSC operation 0 - Use manual CSC coefficients 1 - Use automatic CSC coefficients
SDP_RET_VID_ADJ		R/W
0xE0	010**0**0111	A control to enable retiming video adjustments to VBI. 0 - Apply video adjustments when programmed 1 - Retime video adjustments to VBI
SDP_A1[12:0]		R/W
0xE0 0xE1	01000111 11010010	CSC A1 coefficient for SDP output colour space converter 0x07D2 - Default value
SDP_A2[12:0]		R/W
0xE2 0xE3	00000000 00000000	CSC A2 coefficient for SDP output colour space converter 0x0000 - Default value
SDP_A3[12:0]		R/W
0xE4 0xE5	00000000 01000000	CSC A3 coefficient for SDP output colour space converter 0x0040 - Default value
SDP_A4[14:0]		R/W
0xE6 0xE7	01111111 00000000	CSC A4 coefficient for SDP output colour space converter 0x7F00 - Default value
SDP_B1[12:0]		R/W
0xE8 0xE9	00000000 00000000	CSC B1 coefficient for SDP output colour space converter 0x0000 - Default value
SDP_B2[12:0]		R/W
0xEA 0xEB	00001001 00100110	CSC B2 coefficient for SDP output colour space converter 0x0926 - Default value

Reg	Bits	Description	
SDP_B3[12:0]			R/W
0xEC 0xED	00000<u>00</u> <u>00000000</u>	CSC B3 coefficient for SDP output colour space converter 0x0000 - Default value	
SDP_B4[14:0]			R/W
0xEE 0xEF	0<u>0000000</u> <u>00000000</u>	CSC B4 coefficient for SDP output colour space converter 0x0000 - Default value	
SDP_C1[12:0]			R/W
0xF0 0xF1	00000<u>00</u> <u>00000000</u>	CSC C1 coefficient for SDP output colour space converter 0x0000 - Default value	
SDP_C2[12:0]			R/W
0xF2 0xF3	00000<u>00</u> <u>00000000</u>	CSC C2 coefficient for SDP output colour space converter 0x0000 - Default value	
SDP_C3[12:0]			R/W
0xF4 0xF5	00000<u>110</u> <u>10000001</u>	CSC C3 coefficient for SDP output colour space converter 0x0681 - Default value	
SDP_C4[14:0]			R/W
0xF6 0xF7	0<u>0000000</u> <u>00000000</u>	CSC C4 coefficient for SDP output colour space converter 0x0000 - Default value	

2.9 HDMI MAP

Reg	Bits	Description	
EN_BG_PORT_A			R/W
0x00	00<u>0</u>00000	Background mode enable for Port A. Sets Port A in background mode to establish a HDCP link with its source, even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by HDMI_PORT_SELECT. 0 - Port disabled, unless selected with HDMI_PORT_SELECT 1 - Port enabled in background mode.	
EN_BG_PORT_B			R/W
0x00	000<u>0</u>0000	Background mode enable for Port B. Sets Port B in background mode to establish a HDCP link with its source, even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by HDMI_PORT_SELECT. 0 - Port disabled, unless selected with HDMI_PORT_SELECT 1 - Port enabled in background mode.	
BG_MEAS_PORT_SEL[1:0]			R/W
0x00	0000<u>00</u>00	BG_MEAS_PORT_SEL[1:0] selects a background port on which HDMI measurements are to be made and provided in the background measurement registers. The port in question must be set as a background port in order for this setting to be effective. There is no conflict if this matches the port selected by HDMI_PORT_SELECT. 10 - Port A 11 - Port B	
HDMI_PORT_SELECT[1:0]			R/W
0x00	000000<u>00</u>	HDMI primary port selection control. 10 - Port A 11 - Port B	
TERM_AUTO			R/W
0x01	<u>0</u>1111000	This bit allows the user to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected via HDMI_PORT_SELECT[1:0] is enabled. The termination is disabled on all other ports. When automatic mode is disabled the termination for each port is set individually by the CLOCK_TERMx_DISABLE. 0 - Disable Termination automatic control 1 - Enable Termination automatic control	
CLOCK_TERMB_DISABLE			R/W
0x01	0<u>1</u>111000	Disable clock termination on Port B. Can be used when TERM_AUTO set to 0 0 - Enable Termination Port B 1 - Disable Termination Port B	
CLOCK_TERMA_DISABLE			R/W
0x01	01<u>1</u>11000	Disable clock termination on Port A. Can be used when TERM_AUTO set to 0 0 - Enable Termination Port A 1 - Disable Termination Port A	
HDCP_ONLY_MODE			R/W
0x01	01111<u>0</u>00	This control is used to configure a HDCP only mode for simultaneous analog and HDMI modes. Refer to the ADC_HDMI_SIMULTANEOUS_MODE bit. By selecting HDCP only mode, HDMI activity is reduced and it can be used as a power saving feature in simultaneous analog and HDMI operation. 0 - Normal operation 1 - HDCP only mode	
OVR_MUX_HBR			R/W
0x01	0111100	A control to select automatic or manual configuration for HBR outputs. Automatically, HBR outputs are encoded as SPDIF streams. In manual mode MUX_HBR_OUT selects the audio output interface. 0 - Automatic HBR output control 1 - Manual HBR output control	
MUX_HBR_OUT			R/W
0x01	01111000	A control to manually select the audio output interface for HBR data. Valid when OVR_MUX_HBR is set to 1. 0 - Override by outputting I2S data 1 - Override by outputting SPDIF data	
OVR_MUX_DSD_OUT			R/W
0x02	0000000	DSD override control. In automatic control, DSD or I2S interface is selected according to the type of packet received.DSD or audio sample packet received. I2S interface is enabled when part receives audio sample packets or when no packet is received. DSD interface is enabled when DSD packets are received. In manual mode MUX_DSD_OUT selects the output interface for DSD operation. 0 - Automatic DSD output control 1 - Manual DSD output control	

Reg	Bits	Description	
MUX_DSD_OUT			R/W
0x02	0000000<u>0</u>	An override control for the DSD output 0 - Output I2S data in DSD mode 1 - Output DSD data in DSD Mode	
I2SOUTMODE[1:0]			R/W
0x03	0<u>00</u>11000	A control to configure the I2S output interface. 00 - I2S Mode 01 - Right Justified 10 - Left Justified 11 - Raw SPDIF (IEC60958) Mode	
I2SBITWIDTH[4:0]			R/W
0x03	000<u>11000</u>	A control to adjust the bit width for right justified mode on the I2S interface. 00000 - 0 bit 00001 - 1 bit 00010 - 2 bits - ... 11000 - 24 bits 11110 - 30 bits 11111 - 31 bits	
AV_MUTE			R
0x04	0<u>0</u>000000	Readback of AVMUTE status received in the last General Control packet received. 0 - AVMUTE not set 1 - AVMUTE set	
HDCP_KEYS_READ			R
0x04	00<u>0</u>00000	A readback to indicate a successful read of the HDCP keys and/or KSV from the internal HDCP Key OTP ROM. A logic high is returned when the read is successful. 0 - HDCP keys and/or KSV not yet read 1 - HDCP keys and/or KSV read	
HDCP_KEY_ERROR			R
0x04	000<u>0</u>0000	A readback to indicate if a checksum error occurred while reading the HDCP and/or KSV from the HDCP Key ROM. Returns 1 when the HDCP Key master encounters an error while reading the HDCP Key OTP ROM. 0 - No error occurred while reading HDCP keys 1 - HDCP keys read error	
TMDS_PLL_LOCKED			R
0x04	000000<u>0</u>0	A readback to indicate if the TMDS PLL is locked to the TMDS clock input to the selected HDMI port. 0 - The TMDS PLL is not locked 1 - The TMDS PLL is locked to the TMDS clock input to the selected HDMI port.	
AUDIO_PLL_LOCKED			R
0x04	0000000<u>0</u>	A readback to indicate the Audio DPLL lock status. 0 - The audio DPLL is not locked 1 - The audio DPLL is locked	
HDMI_MODE			R
0x05	<u>0</u>0000000	A readback to indicate whether the stream processed by the HDMI core is a DVI or an HDMI stream. 0 - DVI Mode Detected 1 - HDMI Mode Detected	
HDMI_CONTENT_ENCRYPTED			R
0x05	0<u>0</u>000000	A readback to indicate the use of HDCP encryption. 0 - The input stream processed by the HDMI core is not HDCP encrypted 1 - The input stream processed by the HDMI core is HDCP encrypted	
DVI_HSYNC_POLARITY			R
0x05	00<u>0</u>00000	A readback to indicate the polarity of the HSync encoded in the input stream 0 - The HSync is active low 1 - The HSync is active high	
DVI_VSYNC_POLARITY			R
0x05	000<u>0</u>0000	A readback to indicate the polarity of the VSync encoded in the input stream 0 - The VSync is active low 1 - The VSync is active high	

Reg	Bits	Description	
HDMI_PIXEL_REPETITION[3:0]			R
0x05	0000<u>0000</u>	A readback to provide the current HDMI pixel repetition value decoded from the AVI Infoframe received. The HDMI receiver automatically discards repeated pixel data and divides the pixel clock frequency appropriately as per the pixel repetition value. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
VERT_FILTER_LOCKED			R
0x07	<u>0</u>0000000	Vertical filter lock status. Indicates whether or not the vertical filter is locked and vertical synchronization parameter measurements are valid for readback. 0 - Vertical filter has not locked 1 - Vertical filter has locked	
AUDIO_CHANNEL_MODE			R
0x07	0<u>0</u>000000	Flags stereo or multichannel audio packets. Note stereo packets may carry compressed multi-channel audio. 0 - Stereo Audio (may be compressed multichannel) 1 - Multichannel uncompressed audio detected (3-8 channels).	
DE_REGEN_FILTER_LOCKED			R
0x07	00<u>0</u>00000	DE regeneration filter lock status. Indicates that the DE regeneration section has locked to the received DE and horizontal synchronization parameter measurements are valid for readback. 0 - DE regeneration filter is not locked. 1 - DE regeneration filter is locked.	
LINE_WIDTH[12:0]			R
0x07 0x08	000<u>00000</u> <u>00000000</u>	Line width is a horizontal synchronization measurement. The gives the number of active pixels in a line. This measurement is only valid when the DE regeneration filter is locked. 00000000000 - Default value xxxxxxxxxxx - Total number of active pixels per line.	
FIELD0_HEIGHT[12:0]			R
0x09 0x0A	000<u>00000</u> <u>00000000</u>	Field 0 Height is a vertical filter measurement. This readback gives the number of active lines in field 0. This measurement is valid only when the vertical filter has locked. 0000000000000 - Default value xxxxxxxxxxxxx - The number of active lines in Field 0	
DEEP_COLOR_MODE[1:0]			R
0x0B	<u>00</u>000000	A readback of the deep color mode information extracted from the general control packets. 00 - 8-bits per channel 01 - 10-bits per channel 10 - 12-bits per channel 11 - 16-bits per channel (not supported)	
HDMI_INTERLACED			R
0x0B	00<u>0</u>00000	HDMI input Interlace status, a vertical filter measurement. 0 - Progressive Input 1 - Interlaced Input	
FIELD1_HEIGHT[12:0]			R
0x0B 0x0C	000<u>00000</u> <u>00000000</u>	Field 1 height is a vertical filter measurement. This readback gives the number of active lines in field. This measurement is valid only when the vertical filter has locked. Field 1 measurements are only valid when HDMI_INTERLACED is set to 1. 0000000000000 - Default value xxxxxxxxxxxxx - The number of active lines in Field 1	
FREQTOLERANCE[3:0]			R/W
0x0D	0000<u>0100</u>	Sets the tolerance in MHz for new TMDS frequency detection. This tolerance is used for the audio mute mask MT_MSK_VCLK_CHNG and the HDMI status bit NEW_TMDS_FRQ_RAW. 0100 - Default tolerance in MHz for new TMDS frequency detection xxxx - Tolerance in MHz for new TMDS frequency detection	

Reg	Bits	Description	
MAN_AUDIO_DL_BYPASS			R/W
0x0F	00011111	Audio Delay Bypass Manual Enable. The audio delay line is automatically active for stereo samples and bypassed for multichannel samples. By setting MAN_AUDIO_DL_BYPASS to 1 the Audio delay bypass configuration can be set by the user with the AUDIO_DELAY_LINE_BYPASS control. 0 - Audio delay line is automatically bypassed if multichannel audio is received. The audio delay line is automatically enabled if stereo audio is received. 1 - Overrides automatic bypass of audio delay line. Audio delay line is applied depending on the AUDIO_DELAY_LINE_BYPASS control.	
AUDIO_DELAY_LINE_BYPASS			R/W
0x0F	00011111	Manual bypass control for the audio delay line. Only valid if MAN_AUDIO_DL_BYPASS is set to 1. 0 - Enables the audio delay line. 1 - Bypasses the audio delay line.	
AUDIO_MUTE_SPEED[4:0]			R/W
0x0F	00011111	Number of samples between each volume change of 1.5dB when muting and unmuting 11111 - 31 samples between each volume change of 1.5dB when muting and unmuting xxxxx - Number of samples between each volume change of 1.5dB when muting and unmuting	
CTS_CHANGE_THRESHOLD[5:0]			R/W
0x10	00100101	Sets the tolerance for change in the CTS value. This tolerance is used for the audio mute mask MT_MSK_NEW_CTS and the HDMI status bit CTS_PASS_THRSH_RAW and the HDMI interrupt status bit CTS_PASS_THRSH_ST. This register controls the amounts of LSBs that the CTS can change before an audio mute, status change or interrupt is triggered. 100101 - Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS xxxxxx - Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS	
AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0]			R/W
0x11	01111101	Sets the threshold used for FIFO_NEAR_OVRFL_RAW. FIFO_NEAR_OVRFL_ST interrupt is triggered if audio FIFO reaches this level 1111101 - Default value xxxxxx - Sets threshold used for FIFO_NEAR_OVFLOW_RAW	
AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0]			R/W
0x12	00000010	Sets the threshold used for FIFO_NEAR_UFLO_RAW. FIFO_NEAR_UFLO_ST interrupt is triggered if audio FIFO goes below this level 0000010 - Default value xxxxxxx - Sets threshold used for FIFO_NEAR_UFLO_RAW	
AC_MSK_VCLK_CHNG			R/W
0x13	01111111	Audio Coast Mask for TMDS clock change. When set the audio DPLL coasts if the TMDS clock has any irregular/missing pulses. 1 - Audio DPLL coasts if TMDS clock any irregular/missing pulses. 0 - Audio DPLL does not coast if TMDS clock any irregular/missing pulses.	
AC_MSK_VPLL_UNLOCK			R/W
0x13	01111111	Audio Coast Mask for TMDS PLL Unlock. When set the audio DPLL coasts if the TMDS PLL unlocks. 1 - Audio DPLL coasts if TMDS DPLL unlocks. 0 - Audio DPLL does not coast if TMDS DPLL unlocks.	
AC_MSK_NEW_CTS			R/W
0x13	01111111	Audio Coast Mask for a new ACR CTS value. When set the audio DPLL coasts if CTS changes by more than threshold defined in CTS_CHANG_THRESHOLD[5:0]. 1 - Audio DPLL coasts if CTS changes by more than the threshold set in register CTS_CHANGE_THRESHOLD[5:0]. 0 - Audio DPLL does not coast if CTS changes by more than the threshold set in register CTS_CHANGE_THRESHOLD[5:0].	
AC_MSK_NEW_N			R/W
0x13	01111111	Audio Coast Mask for a new ACR N value. When set the audio DPLL coasts if N value changes. 1 - Audio DPLL coasts if a change in the N value occurs. 0 - Audio DPLL does not coast if a change in the N value occurs.	
AC_MSK_CHNG_PORT			R/W
0x13	01111111	Audio Coast Mask for a HDMI port change. When set the audio DPLL coasts if a change in the active port occurs. 1 - Audio DPLL coasts if the active port is changed. 0 - Audio DPLL does not coast if the active port is changed	
AC_MSK_VCLK_DET			R/W
0x13	01111111	Audio Coast Mask for a TMDS clock detection. It sets the audio PLL to coast if no TMDS clock is detected on the active port. 1 - Audio DPLL coasts if a TMDS clock is not detected on the active port. 0 - Audio DPLL does not coast if a TMDS clock is not detected on the active port.	

Reg	Bits	Description
MT_MSK_COMPRS_AUD		R/W
0x14	00111111	Audio Mute Mask for compressed audio. It sets the audio mutes if the audio received is in a compressed format. 1 - Audio mute occurs if audio is received in compressed format.
MT_MSK_AUD_MODE_CHNG		R/W
0x14	00111111	Audio Mute Mask for audio mode change. It sets audio mutes if audio changes between any of the following PCM, DSD, HBR or DST formats. 1 - Audio mute occurs if audio changes between any of the following PCM, DSD, HBR or DST formats.
MT_MSK_PARITY_ERR		R/W
0x14	00111111	Audio Mute Mask for a parity error. It sets the audio mutes if an audio sample packet is received with an incorrect parity bit. 1 - Audio mute occurs if an audio sample packet is received with an incorrect parity bit.
MT_MSK_VCLK_CHNG		R/W
0x14	00111111	Audio Mute Mask for TMDS Clock Change. It sets the audio mutes if the TMDS clock has irregular/missing pulses. 1 - Audio mute occurs if the TMDS clock has irregular/missing pulses.
MT_MSK_APLL_UNLOCK		R/W
0x15	11111111	Audio Mute Mask for Audio PLL Unlock. It sets the audio mutes if the Audio PLL unlocks. 1 - Audio mute occurs if the Audio PLL unlocks.
MT_MSK_VPLL_UNLOCK		R/W
0x15	11111111	Audio Mute Mask for TMDS PLL Unlock. When set audio mutes if the TMDS PLL unlocks. 1 - Audio mute occurs if the TMDS PLL unlocks.
MT_MSK_ACR_NOT_DET		R/W
0x15	11111111	Audio Mute Mask for ACR packet. When set the audio mutes if an ACR packet has not been received within one VSync. 1 - Audio mute occurs if an ACR packet has not been received within one VSync.
MT_MSK_FLATLINE_DET		R/W
0x15	11111111	Audio Mute Mask for Flatline bit. When set the audio mutes if an audio packet is received with the flatline bit set. 1 - Audio mute occurs if an audio packet is received with the flatline bit set.
MT_MSK_FIFO_UNDERLFOW		R/W
0x15	11111111	Audio Mute Mask - FIFO Underflow
MT_MSK_FIFO_OVERFLOW		R/W
0x15	11111111	Audio Mute Mask - FIFO Overflow
MT_MSK_AVMUTE		R/W
0x16	11111111	Audio Mute Mask for AVMUTE. When set the audio mutes if a general Control packet is received with the SET_AVMUTE bit set. 1 - Audio mute occurs if AVMUTE is set by a general control packet
MT_MSK_NOT_HDMIMODE		R/W
0x16	11111111	Audio Mute Mask for a non HDMI input stream. When set the audio mutes if the HDMI_MODE bit goes low. 1 - Audio mute occurs if HDMI mode bit goes low
MT_MSK_NEW_CTS		R/W
0x16	11111111	Audio Mute Mask for a change of ACR CTS. When set the audio mutes if the CTS changes by more than the specified threshold. CTS_CHANGE_THRESHOLD register sets this threshold. 1 - Audio mute occurs if CTS changes
MT_MSK_NEW_N		R/W
0x16	11111111	Audio Mute Mask for a New ACR N. If set the audio mutes if there is a change in the N value. 1 - Audio mute occurs if N changes
MT_MSK_CHMODE_CHNG		R/W
0x16	11111111	Audio Mute Mask for a audio channel mode change. When set the audio mutes if the channel mode changes between stereo and multichannel. 1 - Audio mute occurs if channel mode changes
MT_MSK_APCKT_ECC_ERR		R/W
0x16	11111111	Audio Mute Mask for Audio Packet ECC Error. When set the audio mutes if an uncorrectable error is detected in audio packet by the ECC block. 1 - Audio mute occurs if an uncorrectable error is detected in the audio packet by the ECC block

Reg	Bits	Description	
MT_MSK_CHNG_PORT			R/W
0x16	1111111<u>1</u>	Audio Mute Mask for HDMI Port Change. When set the audio mutes if HDMI port selection is changed. 1 - Audio mute occurs if HDMI port selection is changed	
MT_MSK_VCLK_DET			R/W
0x16	1111111<u>1</u>	Audio Mute Mask for TMDS Clock. When set the audio mutes if a TMDS clock is not detected. 1 - Audio mute occurs if TMDS is not detected	
HBR_AUDIO_PCKT_DET			R
0x18	0000<u>0</u>000	HBR Packet detection bit. This bit resets to zero on the 11th HSync leading edge following an HBR packet if a subsequent HBR packet has not been detected. It also resets if an Audio Sample Packet or DSD packet has been received and after an HDMI reset condition 0 - No HBR audio packet received within the last 10 HSync. 1 - HBR audio packet received within the last 10 HSync.	
DSD_PACKET_DET			R
0x18	0000000<u>0</u>	DSD Audio Packet Detection bit. This bit resets to zero on the 11th HSync leading edge following a DSD packet or if an Audio sample packet or HBR packet has been received or after an HDMI reset condition. 0 - No DSD packet received within the last 10 HSync. 1 - DSD packet received within the last 10 HSync.	
AUDIO_SAMPLE_PCKT_DET			R
0x18	0000000<u>0</u>	Audio Sample Packet Detection bit. This bit resets to zero on the 11th HSync leading edge following an Audio packet if a subsequent audio sample packet has not been received or if a DSD or HBR Audio packet sample packet has been received. 0 - No L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSync. 1 - L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSyncs.	
IGNORE_PARITY_ERR			R/W
0x1A	1<u>0</u>000000	A control to select the processing of audio samples even when they have a parity error. 0 - Discard audio sample packet that have an invalid parity bit. 1 - Process audio sample packets that have an invalid parity bit.	
MUTE_AUDIO			R/W
0x1A	100<u>0</u>0000	A control to force an internal mute independently of the mute mask conditions 0 - Audio in normal operation 1 - Force audio mute	
WAIT_UNMUTE[2:0]			R/W
0x1A	1000<u>000</u>0	A control to delay audio unmute. Once all mute conditions are inactive WAIT_UNMUTE[2:0] can specify a further delay time before unmuting. NOT_AUTO_UNMUTE must be set to 0 for this control to be effective. 000 - 0ms Disables/cancels delayed unmute. Audio unmutes directly after all mute conditions become inactive 001 - Unmutes 10 ms after all mute conditions become inactive 010 - Unmutes 25 ms after all mute conditions become inactive 011 - Unmutes 50 ms after all mute conditions become inactive 100 - Unmutes 75 ms after all mute conditions become inactive 101 - Unmutes 100 ms after all mute conditions become inactive 110 - Unmutes 250 ms after all mute conditions become inactive 111 - Unmutes 1000 ms (1s) after all mute conditions become inactive	
NOT_AUTO_UNMUTE			R/W
0x1A	1000000<u>0</u>	A control to disable the auto unmute feature. When set to 1 audio can be unmuted manually if all mute conditions are inactive by setting NOT_AUTO_UNMUTE to 0 and then back to 1. 0 - Audio unmutes following a delay set by WAIT_UNMUTE after all mute conditions have become inactive. 1 - Prevents audio from unmuting automatically	
DCFIFO_RESET_ON_LOCK			R/W
0x1B	0001<u>1</u>000	Enables the reset/re-centering of video FIFO on video PLL unlock 0 - Do not reset on video PLL lock 1 - Reset FIFO on video PLL lock	
DCFIFO_KILL_NOT_LOCKED			R/W
0x1B	0001<u>1</u>000	DCFIFO_KILL_NOT_LOCKED controls whether or not the output of the Video FIFO is set to zero when the video PLL is unlocked. 0 - FIFO data is output regardless of video PLL lock status 1 - FIFO output is zeroed if video PLL is unlocked	

Reg	Bits	Description
DCFIFO_KILL_DIS		R/W
0x1B	00011000	The Video FIFO output is zeroed if there is more than one resynchronization of the pointers within 2 FIFO cycles. This behavior can be disabled with this bit. 0 - FIFO output set to zero if more than one resynchronization is necessary during two FIFO cycles 1 - FIFO output never set to zero regardless of how many resynchronizations occur
DCFIFO_LOCKED		R
0x1C	00000000	A readback to indicates if Video FIFO is locked. 0 - Video FIFO is not locked. Video FIFO had to resynchronize between previous two Vsyncs 1 - Video FIFO is locked. Video FIFO did not have to resynchronize between previous two Vsyncs
DCFIFO_LEVEL[2:0]		R
0x1C	00000000	A readback that indicates the distance between the read and write pointers. Overflow/underflow would read as level 0. Ideal centered functionality would read as 0b100. 000 - FIFO has underflowed or overflowed 001 - FIFO is about to overflow 010 - FIFO has some margin. 011 - FIFO has some margin. 100 - FIFO perfectly balanced 101 - FIFO has some margin. 110 - FIFO has some margin. 111 - FIFO is about to underflow
UP_CONVERSION_MODE		R/W
0x1D	00000000	A control to select linear or interpolated 4:2:2 to 4:4:4 conversion. A 4:2:2 incoming stream is upconverted to a 4:4:4 stream before being sent to the CP. 0 - Cr and Cb samples are repeated in their respective channel. 1 - Interpolate Cr and Cb values.
TOTAL_LINE_WIDTH[13:0]		R
0x1E 0x1F	00000000 00000000	Total line width is a horizontal synchronization measurement. This gives the total number of pixels per line. This measurement is valid only when the DE regeneration filter has locked. 00000000000000 - Default value xxxxxxxxxxxxxx - Total number of pixels per line.
HSYNC_FRONT_PORCH[12:0]		R
0x20 0x21	00000000 00000000	HSync front porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. 0000000000000 - Default value xxxxxxxxxxxxx - Total number of pixels in the front porch.
HSYNC_PULSE_WIDTH[12:0]		R
0x22 0x23	00000000 00000000	HSync pulse width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. 0000000000000 - Default value xxxxxxxxxxxxx - Total number of pixels in the hsync pulse.
HSYNC_BACK_PORCH[12:0]		R
0x24 0x25	00000000 00000000	HSync Back Porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. 0000000000000 - Default value xxxxxxxxxxxxx - Total number of pixels in the back porch.
FIELD0_TOTAL_HEIGHT[13:0]		R
0x26 0x27	00000000 00000000	Field 0 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 0. (Divide readback value by 2 to get number of lines.) This measurement is valid only when the vertical filter has locked. 0000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in Field 0.
FIELD1_TOTAL_HEIGHT[13:0]		R
0x28 0x29	00000000 00000000	Field 1 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 1. (Divide readback by 2 to get number of lines) This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1. 00000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in Field 1.
FIELD0_VS_FRONT_PORCH[13:0]		R
0x2A 0x2B	00000000 00000000	Field 0 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. (Divide readback by 2 to get number of lines) This measurement is valid only when the vertical filter has locked. 00000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in the VSync Front Porch of Field 0.

Reg	Bits	Description	
FIELD1_VS_FRONT_PORCH[13:0]			R
0x2C 0x2D	00000000 00000000	Field 1 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. (Divide readback value by 2 to get number of lines) This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1 00000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in the VSync Front Porch of Field 1.	
FIELD0_VS_PULSE_WIDTH[13:0]			R
0x2E 0x2F	00000000 00000000	Field 0 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. (Divide readback value by 2 to get number of lines) This measurement is valid only when the vertical filter has locked. 00000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in the VSync Pulse of Field 0.	
FIELD1_VS_PULSE_WIDTH[13:0]			R
0x30 0x31	00000000 00000000	Field 1 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. (Divide readback value by 2 to get number of lines) This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1 00000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in the VSync Pulse of Field 1.	
FIELD0_VS_BACK_PORCH[13:0]			R
0x32 0x33	00000000 00000000	Field 0 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. (Divide readback value by 2 to get number of lines) 00000000000000 - Default value xxxxxxxxxxxxxx - The total number of half lines in the VSync Back Porch of Field 0.	
FIELD1_VS_BACK_PORCH[13:0]			R
0x34 0x35	00000000 00000000	Field 1 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. (Divide readback by 2 to get number of lines)This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1. 00000000000000 - Default value xxxxxxxxxxxxx - The number of half lines in the VSync Back Porch of Field 1.	
CS_DATA[39:0]			R
0x36 0x37 0x38 0x39 0x3A	00000000 00000000 00000000 00000000 00000000	Readback registers for the Channel Status data bits collected from audio channel 0.Refer to hardware manual for more details on the CS Data readbacks.	
OVERRIDE_DEEP_COLOR_MODE			R/W
0x40	00000000	A control to override the Deep Color mode. 0 - The HDMI section unpacks the video data according to the deep-color information extracted from the General Control packets. (Normal operation) 1 - Override the deep color mode extracted from the General Control Packet. The HDMI section unpacks the video data according to the Deep Color mode set in DEEP_COLOR_MODE_USER[1:0].	
DEEP_COLOR_MODE_USER[1:0]			R/W
0x40	00000000	A control to manually set the Deep Color mode. The value set in this register is only effective when OVERRIDE_DEEP_COLOR_MODE is set to 1. 00 - 8 bits per channel 01 - 10 bits per channel 10 - 12 bits per channel 11 - 16 bits per channel (not supported)	
DEREP_N_OVERRIDE			R/W
0x41	01000000	This control allows the user to override the pixel repetition factor. The ADV7844 then uses DEREP_N instead of HDMI_PIXEL_REPETITION[3:0] to discard video pixel data from the incoming HDMI stream. 0 - Automatic detection and processing of procession of pixel repeated modes using the AVI infoframe information. 1 - Enables manual setting of the pixel repetition factor as per DEREP_N[3:0].	
DEREP_N[3:0]			R/W
0x41	01000000	Sets the derepetition value if derepetition is overridden by setting DEREP_N_OVERRIDE. 0000 - DEREP_N+1 indicates the pixel and clock discard factor xxxx - DEREP_N+1 indicates the pixel and clock discard factor	

Reg	Bits	Description
QZERO_ITC_DIS		R/W
0x47	00000000	A control to select manual control of the RGB colorimetry when the AVI infoframe field Q[1:0]=00. To be used in conjunction with QZERO_RGB_FULL 0 - AVI InfoFrame ITC bit decides RGB-full or limited range in case Q[1:0]=00 1 - Manual RGB range as per QZERO_RGB_FULL.
QZERO_RGB_FULL		R/W
0x47	00000000	A control to manually select the HDMI colorimetry when AVI infoframe field Q[1:0]=00. Valid only when QZERO_ITC_DIS is set to 1. 0 - RGB-limited range when Q[1:0]=00 1 - RGB-full when Q[1:0]=00
ALWAYS_STORE_INF		R/W
0x47	00000000	A control to force InfoFrames with checksum errors to be stored. 0 - Stores data from received InfoFrames only if their checksum is correct 1 - Always store the data from received InfoFrame regardless of their checksum
DIS_PWRDNB		R/W
0x48	00000000	This control is used to disable the effect of the PWRDN1 pin. DIS_PWRDNB should be set to 1 if the PWRDN1 pin is unused and unconnected. 0 - PWRDN1 pin is used to set the power mode of the part (e.g. Power Down mode 0, Power Down mode 1 or Normal mode). 1 - PWRDN1 has no effect
DIS_CABLE_DET_RST		R/W
0x48	00000000	This control disables the reset effect of cable detection. 0 - Resets the HDMI section if the 5 V input pin corresponding to the selected HDMI port (e.g. RXA_5V for port A) is inactive 1 - Do not use the 5 V input pins as reset signal for the HDMI section
GAMUT_IRQ_NEXT_FIELD		R/W
0x50	00000000	A control to set the NEW_GAMUT_MDATA_RAW interrupt to detect when the new contents are applicable to next field or to indicate that the Gamut packet is new. This is done using header information of the gamut packet. 0 - Interrupt flag indicates that Gamut packet is new 1 - Interrupt flag indicates that Gamut packet is to be applied next field
CS_COPYRIGHT_MANUAL		R/W
0x50	00000000	A control to select automatic or manual setting of the copyright value of the channel status bit that is passed to the SPDIF output. Manual control is set with the CS_COPYRIGHT_VALUE bit. 0 - Automatic CS copyright control 1 - Manual CS copyright control. Manual value is set by CS_COPYRIGHT_VALUE
CS_COPYRIGHT_VALUE		R/W
0x50	00000000	A control to set the CS Copyright value when in manual configuration of the CS Copyright bit that is passed to the SPDIF output. 0 - Copyright value of channel status bit is 0. Valid only if CS_COPYRIGHT_MANUAL is set to 1 1 - Copyright value of channel status bit is 1. Valid only if CS_COPYRIGHT_MANUAL is set to 1
TMDSFREQ[8:0]		R
0x51 0x52	00000000 00000000	This register provides a full precision integer TMDS frequency measurement 000000000 - Default value xxxxxxxxx - Outputs 9-bit TMDS frequency measurement in MHz
TMDSFREQ_FRAC[6:0]		R
0x52	00000000	A readback to indicate the fractional bits of measured frequency of PLL recovered TMDS clock. The unit is 1/128 MHz. 0000000 - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz xxxxxxx - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz
HDMI_COLORSPACE[3:0]		R
0x53	00000000	A readback of the HDMI input colorspace decoded from several fields in the AVI infoframe. 0000 - RGB_LIMITED 0001 - RGB_FULL 0010 - YUV_601 0011 - YUV_709 0100 - XVYCC_601 0101 - XVYCC_709 0110 - YUV_601_FULL 0111 - YUV_709_FULL 1000 - sYCC 601 1001 - Adobe YCC 601 1010 - Adobe RGB

Reg	Bits	Description	
FILT_5V_DET_DIS			R/W
0x56	01011000	This bit is a control to disable the digital glitch filter on the HDMI 5V detect signals. The filtered signals are used as interrupt flags, and also used to reset the HDMI section. The filter works from an internal ring oscillator clock and is therefore available in power-down mode. The clock frequency of the ring oscillator is 42MHz +/-10%. 0 - Enabled 1 - Disabled	
FILT_5V_DET_TIMER[6:0]			R/W
0x56	01011000	These bits control the timer for the digital glitch filter on the HDMI +5 V detect inputs. The unit of this parameter is 2 clock cycles of the ring oscillator (~ 47ns). The input must be constantly high for the duration of the timer, otherwise the filter output remains low. The output of the filter returns low as soon as any change in the +5 V power signal is detected. 1011000 - Approximately 4.2us xxxxxxx - Time duration of +5 V deglitch filter. The unit of this parameter is 2 clock cycles of the ring oscillator (~ 47ns)	
BG_MEAS_REQ			SC
0x5A	00000000	This bit must be set to get correct measurements of the selected background port. Setting this control sends a request to update the synchronization parameter measurements of the currently selected background port. The port on which the measurement will be made is selected by BG_MEAS_PORT_SEL[1:0]. 0 - No request to update selected background port synchronization parameter measurements 1 - Requests an update of the selected background port synchronization parameter measurements	
HDCP_REPT_EDID_RESET			SC
0x5A	00000000	A reset control for the E-EDID/Repeater controller. When asserted it resets the E-EDID/Repeater controller. 0 - Normal operation 1 - Resets the E-EDID/Repeater controller.	
DCFIFO_RECENTER			SC
0x5A	00000000	A reset to recenter the Video FIFO. This is a self clearing bit. 0 - Video FIFO normal operation. 1 - Video FIFO to re-centre.	
FORCE_N_UPDATE			SC
0x5A	00000000	A control to force an N and CTS value update to the audio DPLL. The audio DPLL regenerates the audio clock. 0 - No effect 1 - Forces an update on the N and CTS values for audio clock regeneration	
CTS[19:0]			R
0x5B 0x5C 0x5D	00000000 00000000 00000000	A readback for the CTS value received in the HDMI datastream. 00000000000000000000 - Default CTS value readback from HDMI stream xxxxxxxxxxxxxxxxxxxx - CTS value readback from HDMI stream	
N[19:0]			R
0x5D 0x5E 0x5F	00000000 00000000 00000000	A readback for the N value received in the HDMI datastream 00000000000000000000 - Default N value readback from HDMI stream xxxxxxxxxxxxxxxxxxxx - N value readback from HDMI stream	
HPA_DELAY_SEL[3:0]			R/W
0x69	10100010	Sets a delay between +5 V detection and hot plug assertion on the HPA output pins, in increments of 100ms per bit. 0000 - No Delay 0001 - 100 ms Delay 0010 - 200 ms Delay 1010 - 1 s Delay 1111 - 1.5 s Delay	
HPA_OVR_TERM			R/W
0x69	10100010	A control to set termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port will be set according to the HPA status of that port. 0 - Automatic or manual I2C control of port termination. 1 - Termination controls disabled and overridden by HPA controls.	

Reg	Bits	Description
HPA_AUTO_INT_EDID[1:0]		R/W
0x69	10100010	Selects the type of automatic control on the HPA output pins. This bit has no effect when HPA_MANUAL is set to 1. 00 - The HPA of an HDMI port is asserted high immediately after the internal EDID has been activated for that port. The HPA of a specific HDMI port is de-asserted low immediately after the internal E-EDID is de-activated for that port. 01 - The HPA of an HDMI port is asserted high following a programmable delay after the part detects an HDMI cable plug on that port. The HPA of an HDMI port is immediately de-asserted after the part detects a cable disconnect on that HDMI port. 10 - The HPA of an HDMI port is asserted high after two conditions have been met. The conditions are detailed as follows. 1. The internal EDID is active for that port. 2. The delayed version of the cable detect signal CABLE_DET_X_RAW for that port is high. The HPA of an HDMI port is immediately de-asserted after any of the following two conditions have been met 1. The internal EDID is de-activated for that port 2. The cable detect signal CABLE_DET_X_RAW for that port is low. 11 - The HPA of an HDMI port is asserted high after three conditions have been met. The conditions are detailed as follows. 1. The internal EDID is active for that port. 2. The delayed version of the cable detect signal CABLE_DET_X_RAW for that port is high. 3. The user has set the manual HPA control for that port to 1 via the HPA_MAN_VALUE_X controls. The HPA of an HDMI port is immediately de-asserted after any of the following three conditions have been met 1.The internal EDID is de-activated for that port 2.The cable detect signal CABLE_DET_X_RAW for that port, is low. 3.The user sets the manual HPD control for that port to 0 via the HPA_MAN_VALUE_X controls
HPA_MANUAL		R/W
0x69	10100010	Manual control enable for the Hot Plug Assert output pins. By setting this bit any automatic control of these pins is disabled. Manual control is determined by the HPA_MAN_VALUE_X (where X = A, B) 0 - HPA takes its value based on HPA_AUTO_INT_EDID 1 - HPA takes its value from HPA_MAN_VALUE_X
I2S_SPDIF_MAP_INV		R/W
0x6A	00000000	A control to invert the arrangement of the I2S/SPDIF interface on the audio output port pins. Note the arrangement of the I2S/SPDIF interface on the audio output port pins is determined by I2S_SPDIF_MAP_ROT. 0 - Do not invert arrangement of I2S/SPDIF channels in audio output port pins 1 - Invert arrangement of I2S/SPDIF channels in audio output port pins
I2S_SPDIF_MAP_ROT[1:0]		R/W
0x6A	00000000	A control to select the arrangement of the I2S/SPDIF interface on the audio output port pins. 00 - [I2S0/SPDIF0 on AP1] [I2S1/SPDIF1 on AP2] [I2S2/SPDIF2 on AP3] [I2S3/SPDIF3 on AP4] 01 - [I2S3/SPDIF3 on AP1] [I2S0/SPDIF0 on AP2] [I2S1/SPDIF1 on AP3] [I2S2/SPDIF2 on AP4] 10 - [I2S2/SPDIF2 on AP1] [I2S3/SPDIF3 on AP2] [I2S0/SPDIF0 on AP3] [I2S1/SPDIF1 on AP4] 11 - [I2S1/SPDIF1 on AP1] [I2S2/SPDIF2 on AP2] [I2S3/SPDIF3 on AP3] [I2S0/SPDIF0 on AP4]
DSD_MAP_INV		R/W
0x6A	00000000	A control to invert the arrangement of the DSD interface on the audio output port pins. Note the arrangement of the DSD interface on the audio output port pins is determined by DSD_MAP_ROT. 0 - Do not invert arrangement of the DSD channels on the audio output port pins 1 - Invert arrangement of the DSD channels on the audio output port pins
DSD_MAP_ROT[2:0]		R/W
0x6A	00000000	A control to select the arrangement of the DSD interface on the audio output port pins. 000 - [DSD0A on AP0] [DSD0B on AP1] [DSD1A on AP2] [DSD1B on AP3] [DSD2A on AP4] [DSD2B on AP5] 001 - [DSD2B on AP0] [DSD0A on AP1] [DSD0B on AP2] [DSD1A on AP3] [DSD1B on AP4] [DSD2A on AP5] 010 - [DSD2A on AP0] [DSD2B on AP1] [DSD0A on AP2] [DSD0B on AP3] [DSD1A on AP4] [DSD1B on AP5] 011 - [DSD1B on AP0] [DSD2A on AP1] [DSD2B on AP2] [DSD0A on AP3] [DSD0B on AP4] [DSD1A on AP5] 100 - [DSD1A on AP0] [DSD1B on AP1] [DSD2A on AP2] [DSD2B on AP3] [DSD0A on AP4] [DSD0B on AP5] 101 - [DSD0B on AP0] [DSD1A on AP1] [DSD1B on AP2] [DSD2A on AP3] [DSD2B on AP4] [DSD0A on AP5] 110 - Reserved 111 - Reserved
VGA_PWRDN		R/W
0x72	00000100	This control is used to power down for the VGA EDID pads. 0 - Power up VGA EDID pads 1 - Powerdown VGA EDID pads
DDC_PDN_B		R/W
0x73	00000000	Powerdown control for HDMI DDC pads on Port B. 0 - Power up HDMI DDC pads. 1 - Powerdown HDMI DDC pads.
DDC_PDN_A		R/W
0x73	00000000	Powerdown control for HDMI DDC pads on Port A. 0 - Power up HDMI DDC pads. 1 - Powerdown HDMI DDC pads.

Reg	Bits	Description	
EQ_DYN_FREQ2[3:0]			R/W
0x8C	1010 0011	A control to set the upper limit, limit 2, for the HDMI Equalizer Dynamic Control Frequency range. The frequency must be specified in MHz divided by 16. 0000 - Reserved. Do not use. 1010 - Default dynamic equalizer frequency limit 2. The default value corresponds to 160 MHz. xxxx - Frequency for limit 2.	
EQ_DYN_FREQ1[3:0]			R/W
0x8C	1010 0011	A control to set the lower limit, limit 1, for the HDMI equalizer dynamic control frequency range. The frequency must be specified in MHz divided by 16. 0000 - Reserved. Do not use. 0011 - Default dynamic equalizer frequency limit 1. The default value corresponds to 48 MHz. xxxx - Frequency for limit 1	
EQ_DYN1_LF[7:0]			R/W
0x8D	00001011	HDMI Equalizer Dynamic Control LF for frequencies below limit1, i.e. range1 00001011 - Default LF gain equalizer settings for dynamic mode range 1 xxxxxxxx - LF gain equalizer settings for dynamic mode range 1	
EQ_DYN1_HF[7:0]			R/W
0x8E	00100000	HDMI Equalizer Dynamic Control HF for frequencies below limit1, i.e. range1 00100000 - Default HF gain equalizer settings for dynamic mode range 1 xxxxxxxx - HF gain equalizer settings for dynamic mode range 1	
EQ_DYN2_LF[7:0]			R/W
0x90	00001011	HDMI Equalizer Dynamic Control LF for frequencies below limit2 and above limit1, i.e. range2 00001011 - Default LF gain equalizer settings for dynamic mode range 2 xxxxxxxx - LF gain equalizer settings for dynamic mode range 2	
EQ_DYN2_HF[7:0]			R/W
0x91	00100000	HDMI Equalizer Dynamic Control HF for frequencies below limit2 and above limit1, i.e. range2 00100000 - Default HF gain equalizer settings for dynamic mode range 2 xxxxxxxx - HF gain equalizer settings for dynamic mode range 2	
EQ_DYN3_LF[7:0]			R/W
0x93	00001011	HDMI Equalizer Dynamic Control LF for frequencies above limit2, i.e. range3 00001011 - Default LF gain equalizer settings for dynamic mode range 3 xxxxxxxx - LF gain equalizer settings for dynamic mode range 3	
EQ_DYN3_HF[7:0]			R/W
0x94	00100000	HDMI Equalizer Dynamic Control HF for frequencies above limit2, i.e. range3 00100000 - Default HF gain equalizer settings for dynamic mode range 3 xxxxxxxx - HF gain equalizer settings for dynamic mode range 3	
EQ_DYN_EN			R/W
0x96	0000000 0	Enable for HDMI Equalizer Dynamic Control 0 - Disables equalizer dynamic mode. The equalizer is configured in static mode. 1 - Enables equalizer dynamic mode. Equaliser is configured via EQ_DYNx_HF and EQ_DYNx_LF settings.	
BG_TMDSFREQ[8:0]			R
0xE0 0xE1	00000000 0 0000000	This register provides a precision integer TMDS frequency measurement on the background port selected by BG_MEAS_PORT_SEL. The value provided is the result of a single measurement of the TMDS PLL frequency in MHz. This value is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 000000000 - Outputs 9-bit TMDS frequency measurement in MHz xxxxxxxxx - Outputs 9-bit TMDS frequency measurement in MHz	
BG_TMDSFREQ_FRAC[6:0]			R
0xE1	0 0000000	This register provides a precision fractional measurement of the TMDS frequency on the background port selected by BG_MEAS_PORT_SEL. The unit is 1/128 MHz and the value is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 0000000 - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz xxxxxxx - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz	
BG_LINE_WIDTH[12:0]			R
0xE2 0xE3	000 00000 00000000	Background port line width, a horizontal synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the number of active pixels in a line and is updated when a update request is made via the BG_MEAS_REQ control bit. 0000000000000 - The number of active pixels per line on the background measurement port. xxxxxxxxxxxxx - The number of active pixels per line on the background measurement port.	

Reg	Bits	Description	
BG_TOTAL_LINE_WIDTH[13:0]			R
0xE4 0xE5	00000000 00000000	Background port total line width, a horizontal synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the total number of pixels in a line and is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. xxxxxxxxxxxx - The total number of pixels per line on the background measurement port	
BG_FIELD_HEIGHT[12:0]			R
0xE6 0xE7	00000000 00000000	Background port field height is a vertical synchronization measurement for a background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the number of active lines in a field and is updated when a update request is made via the BG_MEAS_REQ control bit. 0000000000000 - The number of active lines in a Field on the background measurement port xxxxxxxxxxxxx - The number of active lines in a Field on the background measurement port	
BG_TOTAL_FIELD_HEIGHT[12:0]			R
0xE8 0xE9	00000000 00000000	Background port total field height is a vertical synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the total number of lines in a field and is updated when an update request is made via the BG_MEAS_REQ control bit. 0000000000000 - The total number of lines in a Field on the background measurement port xxxxxxxxxxxxx - The total number of lines in a Field on the background measurement port	
BG_PIX_REP[3:0]			R
0xEA	00000000	Background port pixel repetition status for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The readback provides the pixel repetition value in AVI Infoframe and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
BG_DEEP_COLOR_MODE[1:0]			R
0xEA	00000000	This readback provides the deep-color status for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The readback provides the HDMI color depth and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 00 - 8-bit color per channel 01 - 10-bit color per channel 10 - 12-bit color per channel 11 - 16-bit color per channel	
BG_PARAM_LOCK			R
0xEA	00000000	A flag to indicate that vertical and horizontal parameters have been locked during a background measurement. 0 - Horizontal and Vertical were not locked when measurements for selected background HDMI port were taken. 1 - Horizontal and Vertical were locked when measurements for selected background HDMI port were taken.	
BG_HDMI_INTERLACED			R
0xEA	00000000	Background port HDMI input interlace status is a vertical filter measurement for a background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The status readback is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 0 - Progressive Input 1 - Interlaced Input	
BG_HDMI_MODE			R
0xEB	00000000	This readback provides the HDMI/DVI mode status of the background port determined by BG_MEAS_PORT_SEL[1:0] and is updated continuously. 0 - DVI Mode Detected 1 - HDMI Mode Detected	

2.10 REPEATER MAP

Reg	Bits	Description	
BKSV[39:0]			R
0x00 0x01 0x02 0x03 0x04	00000000 00000000 00000000 00000000 00000000	The receiver Key Selection Vector (BKSV) can be read back once the part has successfully accessed the HDCP ROM. The following registers contain the BKSV read from the EEPROM. 0x00[7:0] - BKSV[7:0] 0x01[7:0] - BKSV[15:8] 0x02[7:0] - BKSV[23:16] 0x03[7:0] - BKSV[31:24] 0x04[7:0] - BKSV[39:32]	
RI[15:0]			R
0x08 0x09	00000000 00000000	Ri generated by HDCP core	
PJ[7:0]			R
0x0A	00000000	Pj generated by HDCP core	
AKSV[39:0]			R/W
0x10 0x11 0x12 0x13 0x14	00000000 00000000 00000000 00000000 00000000	The AKSV of the transmitter attached to the active HDMI port can be read back after an AKSV update. The following registers contain the AKSV written by the Tx. 0x10[7:0] - AKSV[7:0] 0x11[7:0] - AKSV[15:8] 0x12[7:0] - AKSV[23:16] 0x13[7:0] - AKSV[31:24] 0x14[7:0] - AKSV[39:32]	
AINFO[7:0]			R/W
0x15	00000000	AINFO written by Tx	
AN[63:0]			R/W
0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000	AN written by Tx 0x10[7 - 0] AKSV[7:0]	
SHA_A[31:0]			R/W
0x20 0x21 0x22 0x23	00000000 00000000 00000000 00000000	SHA Hash Part A generated by inchip micro 0x11[7 - 0] AKSV[15:8]	
SHA_B[31:0]			R/W
0x24 0x25 0x26 0x27	00000000 00000000 00000000 00000000	SHA Hash Part B generated by inchip micro 0x12[7 - 0] AKSV[23:16]	
SHA_C[31:0]			R/W
0x28 0x29 0x2A 0x2B	00000000 00000000 00000000 00000000	SHA Hash Part C generated by inchip micro 0x13[7 - 0] AKSV[31:24]	
SHA_D[31:0]			R/W
0x2C 0x2D 0x2E 0x2F	00000000 00000000 00000000 00000000	SHA Hash Part D generated by inchip micro 0x14[7 - 0] AKSV[39:32]	

Reg	Bits	Description	
SHA_E[31:0]			R/W
0x30 0x31 0x32 0x33	00000000 00000000 00000000 00000000	SHA Hash Part E generated by inchip micro	
BCAPS[7:0]			R/W
0x40	10000011	This is the BCAPS register presented to the Tx attached to the active HDMI port. 10000011 - Default BCAPS register value presented to the Tx xxxxxxxx - BCAPS register value presented to the Tx	
BSTATUS[15:0]			R/W
0x41 0x42	00000000 00000000	These registers contain the BSTATUS information presented to the Tx attached to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater. xxxxxxxxxxxxxxxx - BSTATUS register presented to Tx 0000000000000000 - Reset value. BSTATUS register is reset only after power up. 0x41[7:0] - BSTATUS[7:0] 0x42[7:0] - BSTATUS[15:8]	
SPA_PORT_A[15:0]			R/W
0x72 0x73	00000000 00000000	Source Physical Address for Port A. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID. 0000000000000000 - Default value xxxxxxxxxxxxxxxx - Source physical address of Port A	
SPA_PORT_B[15:0]			R/W
0x74 0x75	00000000 00000000	Source Physical Address for Port B. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID. 0000000000000000 - Default value xxxxxxxxxxxxxxxx - Source physical address of Port B	
SPA_LOCATION[7:0]			R/W
0x76	11000000	This is the location in the E-EDID data where the SPA is located. 11000000 - Default value xxxxxxxx - Location of source physical address in internal E-EDID for ports A and B	
KSV_LIST_READY			R/W
0x77	0xxxxxxx	The system sets this bit in order to indicate that the KSV list has been read from the Tx IC(s) and written into the Repeater Map. The system must also set bits [11:0] of Bstatus before setting this bit. 0 - Not Ready 1 - Ready	
SPA_LOCATION_MSB			R/W
0x77	x0xxxxxx	Additional MSB of SPA_location (i.e. spa_location[8]) needed to point to SPAs stored in second segment.	
DISABLE_AUTO_EDID			R/W
0x77	xx0xxxxx	Disables all automatic enables for internal E-EDID 0 - Automatic enable of internal E-EDID on HDMI ports when the part comes out of powerdown mode 1 - Disable automatic enable of internal E-EDID on HDMI ports when the part comes out of powerdown mode	
EDID_SEGMENT_POINTER			R/W
0x77	xxx0xxxx	Segment pointer for internal EDID in main i2c	
EDID_B_ENABLE			R/W
0x77	xxxx0xxx	Enables I2C access to internal EDID RAM from DDC Port B 0 - E-EDID for Port B disabled 1 - E-EDID for Port B enabled	
EDID_A_ENABLE			R/W
0x77	xxxxx0xx	Enables I2C access to internal EDID RAM from DDC Port A 0 - E-EDID for Port A disabled 1 - E-EDID for Port A enabled	
EXT_EEPROM_TRI			R/W
0x78	x0xxxxxx	Tri-states the output pins to the external SPI EEPROM 0 - SPI interface outputs enabled 1 - SPI interface outputs tri-stated	

Reg	Bits	Description	
VGA_EDID_ENABLE_CPU			R
0x79	00<u>0</u>00000	Flags internal EDID enabling in VGA port 0 - Disabled 1 - Enabled	
PORT_A_CHECKSUM[7:0]			R/W
0x7B	<u>00000000</u>	This is the checksum for the second half of the Port A EDID. This is calculated automatically. 00000000 - Default value xxxxxxxx - Checksum for E-EDID block containing SPA for Port A	
PORT_B_CHECKSUM[7:0]			R/W
0x7C	<u>00000000</u>	This is the checksum for the second half of the Port B EDID. This is calculated automatically. 00000000 - Default value xxxxxxxx - Checksum for E-EDID block containing SPA for Port B	
EDID_B_ENABLE_CPU			R
0x7D	0000<u>0</u>000	Flags internal EDID enabling on Port B 0 - Disabled 1 - Enabled	
EDID_A_ENABLE_CPU			R
0x7D	00000<u>0</u>00	Flags internal EDID enabling on Port A 0 - Disabled 1 - Enabled	
KSV_LIST_READY_CLEAR_A			SC
0x7E	00<u>0</u>00000	Clears BCAPS KSV list ready bit in port A	
KSV_LIST_READY_CLEAR_B			SC
0x7E	000<u>0</u>0000	Clears BCAPS KSV list ready bit in port B	
LOAD_EDID			SC
0x7E	0000000<u>0</u>	Force loading internal E-EDID RAM with SPI EEPROM contents. This self clearing bit returns to 0 after successfully loading the internal E-EDID RAM with the SPI EEPROM contents. 0 - No effect 1 - Load internal E-EDID RAM with SPI EEPROM contents	
STORE_EDID			SC
0x7E	0000000<u>0</u>	Write internal E-EDID RAM contents to SPI EEPROM. This self clearing bit returns to 0 after successfully writing the contents of the internal E-EDID RAM to SPI EEPROM. 0 - No effect 1 - Write contents of internal E-EDID RAM to SPI EEPROM	
VGA_EDID_ENABLE			R/W
0x7F	<u>0</u>0000100	Enables I2C access to internal EDID ram for VGA port. Note that enabling this bits disables access to upper segment in DDC ports	
AUTO_HDCP_MAP_ENABLE			R/W
0x7F	00000<u>1</u>00	Selects which port will be accessed for HDCP addresses: the HDMI active port (selected by HDMI_PORT_SELECT, HDMI map) or the one selected in HDCP_MAP_SELECT 0 - HDCP data read from port given by HDCP_MAP_SELECT 1 - HDCP data read from the active HDMI port	
HDCP_MAP_SELECT[1:0]			R/W
0x7F	000001<u>00</u>	Selects which port will be accessed for HDCP addresses (0x00 to 0x42 in Repeater map). This only takes effect when AUTO HDCP MAN ENABLE is 0 00 - Reserved 01 - Reserved 10 - Select port A 11 - Select port B	
KSV_0[39:0]			R/W
0x80 0x81 0x82 0x83 0x84	<u>00000000</u> <u>00000000</u> <u>00000000</u> <u>00000000</u> <u>00000000</u>	This is a KSV in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_1[39:0]			R/W
0x85 0x86 0x87 0x88 0x89	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_2[39:0]			R/W
0x8A 0x8B 0x8C 0x8D 0x8E	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_3[39:0]			R/W
0x8F 0x90 0x91 0x92 0x93	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_4[39:0]			R/W
0x94 0x95 0x96 0x97 0x98	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_5[39:0]			R/W
0x99 0x9A 0x9B 0x9C 0x9D	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_6[39:0]			R/W
0x9E 0x9F 0xA0 0xA1 0xA2	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_7[39:0]			R/W
0xA3 0xA4 0xA5 0xA6 0xA7	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_8[39:0]			R/W
0xA8 0xA9 0xAA 0xAB 0xAC	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_9[39:0]			R/W
0xAD 0xAE 0xAF 0xB0 0xB1	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_10[39:0]			R/W
0xB2 0xB3 0xB4 0xB5 0xB6	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_11[39:0]			R/W
0xB7 0xB8 0xB9 0xBA 0xBB	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_12[39:0]			R/W
0xBC 0xBD 0xBE 0xBF 0xC0	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_13[39:0]			R/W
0xC1 0xC2 0xC3 0xC4 0xC5	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_14[39:0]			R/W
0xC6 0xC7 0xC8 0xC9 0xCA	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_15[39:0]			R/W
0xCB 0xCC 0xCD 0xCE 0xCF	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_16[39:0]			R/W
0xD0 0xD1 0xD2 0xD3 0xD4	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_17[39:0]			R/W
0xD5 0xD6 0xD7 0xD8 0xD9	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_18[39:0]			R/W
0xDA 0xDB 0xDC 0xDD 0xDE	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_19[39:0]			R/W
0xDF 0xE0 0xE1 0xE2 0xE3	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_20[39:0]			R/W
0xE4 0xE5 0xE6 0xE7 0xE8	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_21[39:0]			R/W
0xE9 0xEA 0xEB 0xEC 0xED	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_22[39:0]			R/W
0xEE 0xEF 0xF0 0xF1 0xF2	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	
KSV_23[39:0]			R/W
0xF3 0xF4 0xF5 0xF6 0xF7	00000000 00000000 00000000 00000000 00000000	This is a KSV in the KSV list used for the HDCP repeater protocol.	

2.11 INFOFRAME MAP

Reg	Bits	Description	
AVI_INF_PB[223:0]			R
0x00	00000000	AVI infoframe data	
0x01	00000000		
0x02	00000000		
0x03	00000000		
0x04	00000000		
0x05	00000000		
0x06	00000000		
0x07	00000000		
0x08	00000000		
0x09	00000000		
0x0A	00000000		
0x0B	00000000		
0x0C	00000000		
0x0D	00000000		
0x0E	00000000		
0x0F	00000000		
0x10	00000000		
0x11	00000000		
0x12	00000000		
0x13	00000000		
0x14	00000000		
0x15	00000000		
0x16	00000000		
0x17	00000000		
0x18	00000000		
0x19	00000000		
0x1A	00000000		
0x1B	00000000		
AUD_INF_PB[111:0]			R
0x1C	00000000	Audio infoframe data	
0x1D	00000000		
0x1E	00000000		
0x1F	00000000		
0x20	00000000		
0x21	00000000		
0x22	00000000		
0x23	00000000		
0x24	00000000		
0x25	00000000		
0x26	00000000		
0x27	00000000		
0x28	00000000		
0x29	00000000		

Reg	Bits	Description	
SPD_INF_PB[223:0]			R
0x2A	00000000	Source Prod infoframe data	
0x2B	00000000		
0x2C	00000000		
0x2D	00000000		
0x2E	00000000		
0x2F	00000000		
0x30	00000000		
0x31	00000000		
0x32	00000000		
0x33	00000000		
0x34	00000000		
0x35	00000000		
0x36	00000000		
0x37	00000000		
0x38	00000000		
0x39	00000000		
0x3A	00000000		
0x3B	00000000		
0x3C	00000000		
0x3D	00000000		
0x3E	00000000		
0x3F	00000000		
0x40	00000000		
0x41	00000000		
0x42	00000000		
0x43	00000000		
0x44	00000000		
0x45	00000000		
MS_INF_PB[111:0]			R
0x46	00000000	MPEG Source infoframe data	
0x47	00000000		
0x48	00000000		
0x49	00000000		
0x4A	00000000		
0x4B	00000000		
0x4C	00000000		
0x4D	00000000		
0x4E	00000000		
0x4F	00000000		
0x50	00000000		
0x51	00000000		
0x52	00000000		
0x53	00000000		

Reg	Bits	Description	
VS_INF_PB[223:0]			R
0x54	00000000	Vendor Specific infoframe data	
0x55	00000000		
0x56	00000000		
0x57	00000000		
0x58	00000000		
0x59	00000000		
0x5A	00000000		
0x5B	00000000		
0x5C	00000000		
0x5D	00000000		
0x5E	00000000		
0x5F	00000000		
0x60	00000000		
0x61	00000000		
0x62	00000000		
0x63	00000000		
0x64	00000000		
0x65	00000000		
0x66	00000000		
0x67	00000000		
0x68	00000000		
0x69	00000000		
0x6A	00000000		
0x6B	00000000		
0x6C	00000000		
0x6D	00000000		
0x6E	00000000		
0x6F	00000000		
ACP_PB[223:0]			R
0x70	00000000	ACP infoframe data	
0x71	00000000		
0x72	00000000		
0x73	00000000		
0x74	00000000		
0x75	00000000		
0x76	00000000		
0x77	00000000		
0x78	00000000		
0x79	00000000		
0x7A	00000000		
0x7B	00000000		
0x7C	00000000		
0x7D	00000000		
0x7E	00000000		
0x7F	00000000		
0x80	00000000		
0x81	00000000		
0x82	00000000		
0x83	00000000		
0x84	00000000		
0x85	00000000		
0x86	00000000		
0x87	00000000		
0x88	00000000		
0x89	00000000		
0x8A	00000000		
0x8B	00000000		

Reg	Bits	Description	
ISRC1_PB[223:0]			R
0x8C	00000000	ISRC 1 infoframe data	
0x8D	00000000		
0x8E	00000000		
0x8F	00000000		
0x90	00000000		
0x91	00000000		
0x92	00000000		
0x93	00000000		
0x94	00000000		
0x95	00000000		
0x96	00000000		
0x97	00000000		
0x98	00000000		
0x99	00000000		
0x9A	00000000		
0x9B	00000000		
0x9C	00000000		
0x9D	00000000		
0x9E	00000000		
0x9F	00000000		
0xA0	00000000		
0xA1	00000000		
0xA2	00000000		
0xA3	00000000		
0xA4	00000000		
0xA5	00000000		
0xA6	00000000		
0xA7	00000000		
ISRC2_PB[223:0]			R
0xA8	00000000	ISRC 2 infoframe data	
0xA9	00000000		
0xAA	00000000		
0xAB	00000000		
0xAC	00000000		
0xAD	00000000		
0xAE	00000000		
0xAF	00000000		
0xB0	00000000		
0xB1	00000000		
0xB2	00000000		
0xB3	00000000		
0xB4	00000000		
0xB5	00000000		
0xB6	00000000		
0xB7	00000000		
0xB8	00000000		
0xB9	00000000		
0xBA	00000000		
0xBB	00000000		
0xBC	00000000		
0xBD	00000000		
0xBE	00000000		
0xBF	00000000		
0xC0	00000000		
0xC1	00000000		
0xC2	00000000		
0xC3	00000000		

Reg	Bits	Description	
GBD[223:0]			R
0xC4	00000000	Gamut infoframe data	
0xC5	00000000		
0xC6	00000000		
0xC7	00000000		
0xC8	00000000		
0xC9	00000000		
0xCA	00000000		
0xCB	00000000		
0xCC	00000000		
0xCD	00000000		
0xCE	00000000		
0xCF	00000000		
0xD0	00000000		
0xD1	00000000		
0xD2	00000000		
0xD3	00000000		
0xD4	00000000		
0xD5	00000000		
0xD6	00000000		
0xD7	00000000		
0xD8	00000000		
0xD9	00000000		
0xDA	00000000		
0xDB	00000000		
0xDC	00000000		
0xDD	00000000		
0xDE	00000000		
0xDF	00000000		
AVI_PACKET_ID[7:0]			R/W
0xE0	10000010	AVI infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x00 to 0x1B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x00 to 0x1B	
AVI_INF_VERS[7:0]			R
0xE1	00000000	AVI infoframe version	
AVI_INF_LEN[7:0]			R
0xE2	00000000	AVI infoframe length	
AUD_PACKET_ID[7:0]			R/W
0xE3	10000100	Audio infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x1C to 0x29 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x1C to 0x29	
AUD_INF_VERS[7:0]			R
0xE4	00000000	Audio infoframe version	
AUD_INF_LEN[7:0]			R
0xE5	00000000	Audio infoframe length	
SPD_PACKET_ID[7:0]			R/W
0xE6	10000011	Source Prod infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x2A to 0x45 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x2A to 0x45	
SPD_INF_VERS[7:0]			R
0xE7	00000000	Source Prod infoframe version	
SPD_INF_LEN[7:0]			R
0xE8	00000000	Source Prod infoframe length	
MS_PACKET_ID[7:0]			R/W
0xE9	10000101	MPEG Source infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x46 to 0x53 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x46 to 0x53	

Reg	Bits	Description	
MS_INF_VERS[7:0]			R
0xEA	00000000	MPEG Source infoframe version	
MS_INF_LEN[7:0]			R
0xEB	00000000	MPEG Source infoframe length	
VS_PACKET_ID[7:0]			R/W
0xEC	10000001	Vendor Specific infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F 1xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F	
VS_INF_VERS[7:0]			R
0xED	00000000	Vendor Specific infoframe version	
VS_INF_LEN[7:0]			R
0xEE	00000000	Vendor Specific infoframe length	
ACP_PACKET_ID[7:0]			R/W
0xEF	00000100	ACP infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x70 to 0x8B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x70 to 0x8B	
ACP_TYPE[7:0]			R
0xF0	00000000	ACP infoframe version	
ACP_HEADER2[7:0]			R
0xF1	00000000	ACP infoframe length	
ISRC1_PACKET_ID[7:0]			R/W
0xF2	00000101	ISRC1 infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x8C to 0xA7 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x8C to 0xA7	
ISRC1_HEADER1[7:0]			R
0xF3	00000000	ISRC1 infoframe version	
ISRC1_HEADER2[7:0]			R
0xF4	00000000	ISRC1 infoframe length	
ISRC2_PACKET_ID[7:0]			R/W
0xF5	00000110	ISRC2 infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xA8 to 0xC3 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0xA8 to 0xC3	
ISRC2_HEADER1[7:0]			R
0xF6	00000000	ISRC2 infoframe version	
ISRC2_HEADER2[7:0]			R
0xF7	00000000	ISRC2 infoframe length	
GAMUT_PACKET_ID[7:0]			R/W
0xF8	00001010	Gamut infoframe ID 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xC4 to 0xDF 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0xC4 to 0xDF	
GAMUT_HEADER1[7:0]			R
0xF9	00000000	Gamut infoframe version	
GAMUT_HEADER2[7:0]			R
0xFA	00000000	Gamut infoframe length	

2.12 DPLL MAP

Reg	Bits	Description	
MCLK_FS_N[2:0]			R/W
0xB5	00000001	Selects the multiple of 128fs used for MCLK out. 000 - 128fs 001 - 256fs 010 - 384fs 011 - 512fs 100 - 640fs 101 - 768fs 110 - Not Valid 111 - Not Valid	
DLL_PHASE[5:0]			R/W
0xC8	00000000	This control is used to adjust the phase of the ADC sampling clock. 000000 - Default xxxxxx - Adjusts the phase of the ADC sampling clock	
FB_PHASE_ADJUST[3:0]			R/W
0xC9	00000000	SCART fast blank phase delay adjustment in increments of 1/8th of the ADC clock cycle. The critical information extracted from the SCART fast blank signal is the time at which it switches relative to the input video. Due to small timing inequalities, either on the IC or on the PCB, it may be necessary to adjust the result by fractions of one clock cycle. This is controlled by FB_PHASE_ADJ[3:0]. 1001 - Default xxxx - Adjust the phase in increments of 1/8th of a ADC clock cycle.	

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