

# APIX2 Receiver with LVDS, HDCP, and MIPI Support

Data Sheet ADV7782

#### **FEATURES**

**APIX2 receiver with HDCP** 

High-bandwidth Digital Content Protection (HDCP) 1.4 support with internal preprogrammed HDCP keys HDCP decryption of video and audio

**HDCP** repeater support

Supports 2 independent video streams

One TDM channel with support for up to 4 stereo pairs

Up to 3000 Mbps sustained downstream link bandwidth

Up to 187.5 Mbps upstream link bandwidth

Media independent interface (MII), serial port interface (SPI),

I<sup>2</sup>C, and GPIO interfaces for sideband communication

LVDS receiver (OpenLDI)

85 MHz maximum clock frequency

Maximum resolution supported is WXGA

Supports receiving video in both 24-bit mode over 4 differential pairs, and 18-bit mode over 3 differential pairs

Dual MIPI CSI 2.0 transmitters

uai Miri C3i 2.0 transinitters

MIPI-A: clock and 4 data lanes

MIPI-B: clock and 2 data lanes

Video processing

**Color space conversion** 

4:2:2 to 4:4:4 interpolation

Software driver

MISRA-C compliant software driver for automotive acceptability General

**Qualified for automotive applications** 

-40°C to +85°C temperature grade

100-ball, 9 mm × 9 mm, RoHS-compliant CSP BGA package

#### **APPLICATIONS**

Automotive high end head unit Automotive infotainment

Portable devices

The approved use of the ADV7782 device is limited to use cases where the ADV7782 data output is directly input to a processing unit

#### **GENERAL DESCRIPTION**

The ADV7782 is a receiver that is compatible with an APIX® or APIX2® serial data stream. The ADV7782 performs limited processing (color space conversion and interpolation 4:2:2 to 4:4:4), and forwards the data via MIPI® camera serial interface (CSI). Data from the LVDS input (OpenLDI) can also be routed through the same processing blocks. It supports a point-to-point connection topology, and supports HDCP repeater implementations with a key selection vector (KSV) list memory of 25 entries.

There are three primary video sources: LVDS OpenLDI, APIX Channel 0, and APIX Channel 1. These three primary video streams are input to a video switch matrix. Any two of the three streams can be selected and output from the switch matrix.

Of the two video channels output from the video switch matrix, one output channel is unprocessed, and the other output channel passes through a combination of an interpolation block (4:2:2 to 4:4:4) and a color space converter.

For more information about the ADV7782, including the complete data sheet, contact your local Analog Devices, Inc., sales office at www.analog.com/sales.

### **FUNCTIONAL BLOCK DIAGRAM**

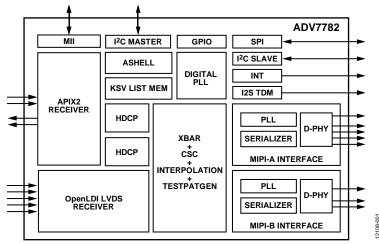


Figure 1.

ADV7782 Data Sheet

## **NOTES**

APIX® is a registered mark of INOVA Semiconductors GMbH.

 $I^2 C\ refers\ to\ a\ communications\ protocol\ originally\ developed\ by\ Philips\ Semiconductors\ (now\ NXP\ Semiconductors).$ 

