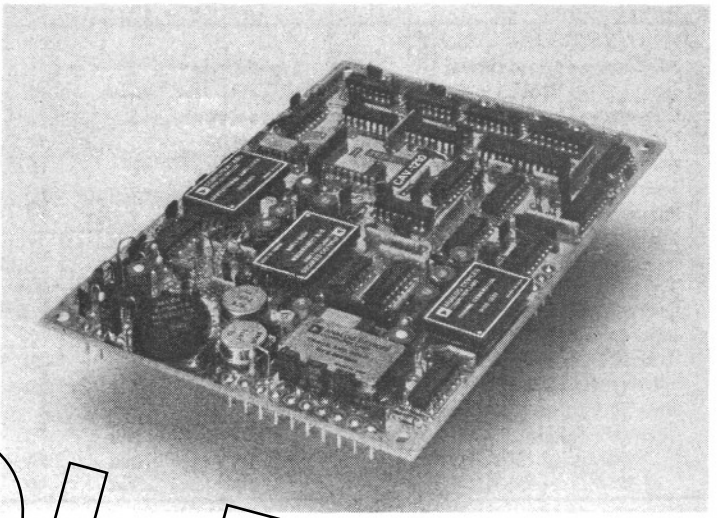
12-Bit Video Analog-to-Digital Converter

CAV-1210

FEATURES
- 12-Bit Resolution
- 10MHz Word Rate
- Single 35-In^2 PC Board
- ECL Compatible
- No External Circuits Required

APPLICATIONS
- Radar Digitizing
- Medical Instrumentation
- Digital Communications
- Spectrum Analysis



GENERAL DESCRIPTION

The Analog Devices model CAV-1210 A/D converter combines performance, size, and economy to achieve a remarkable solution for high-speed digitizing problems.

The unit is capable of 12 bits of resolution at word rates through 10MHz. It is a complete answer to the question of digitizing radar, video, and/or other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-1210 is a "system solution" for the designer who wants to avoid the need for combining the plethora of components necessary to make IC encoders operate as functional A/D converters.

The unit uses the unique digital correcting subranging (DCS) conversion technique, pioneered by Analog Devices, which virtually eliminates the errors normally associated with subranging A/D converters.

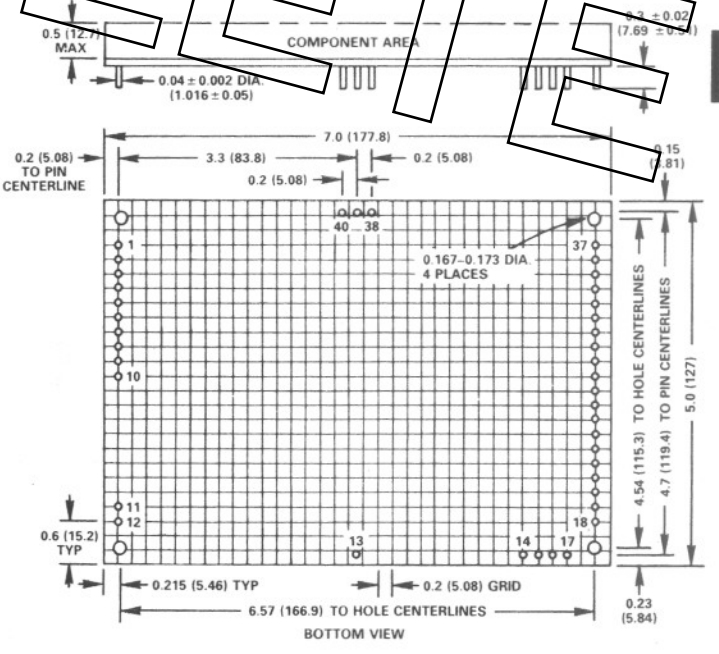
The CAV-1210 is constructed on a single PC board intended for mounting on a "mother" board in the user's system. Its small size makes it adaptable to a wide range of mother board sizes and allows room for including other (signal conditioning, processing, memory, etc.) circuits adjacent to the converter.

All inputs and outputs are ECL compatible; analog input impedance is 1000 ohms. The A/D requires only an encode command and external power supplies for operation.

Hybrid microcircuits, ICs and discrete components are combined in the design, to obtain the maximum benefits of all technologies. The CAV-1210 is repairable and backed by Analog Devices' limited one-year warranty.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

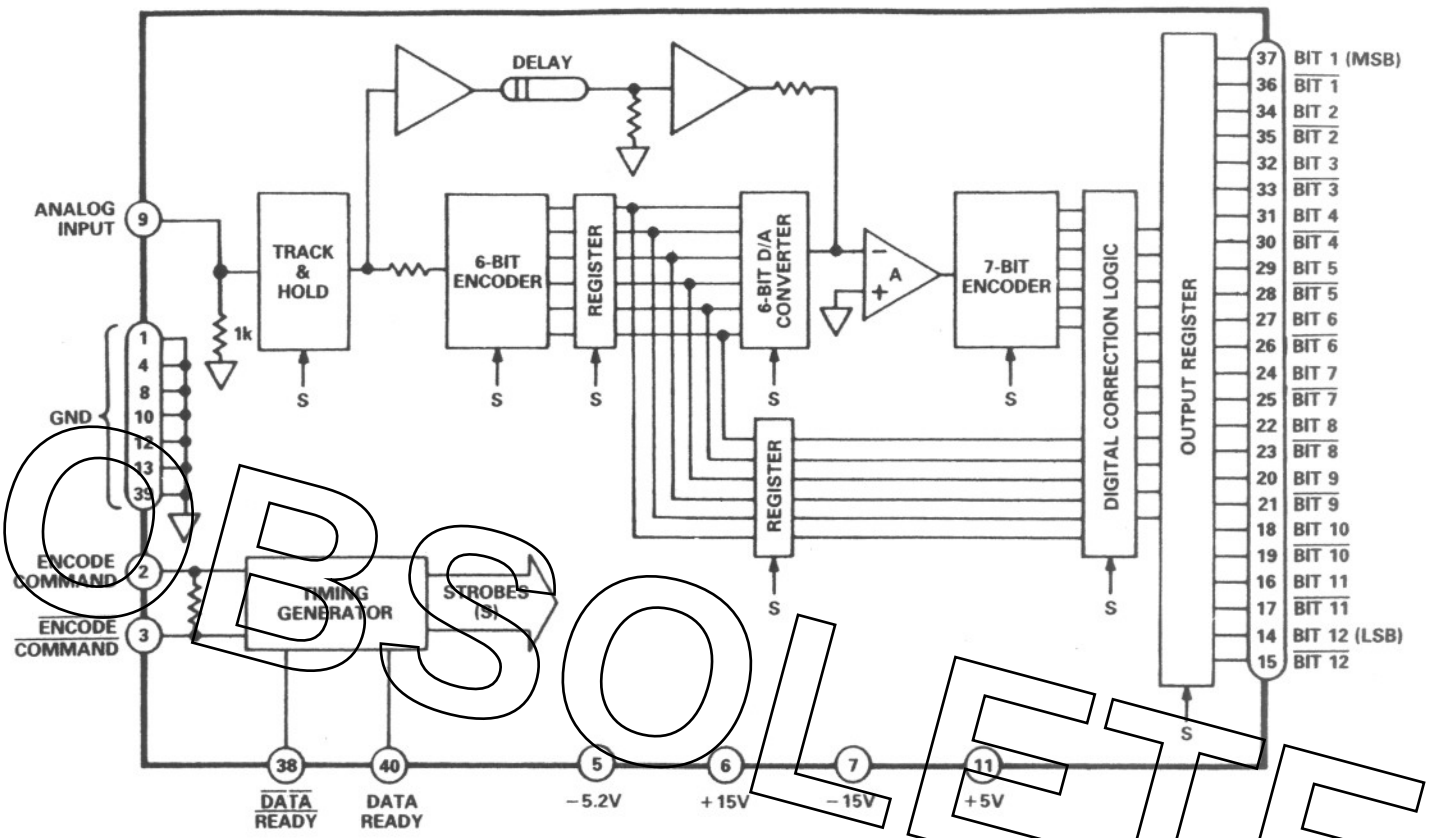


SPECIFICATIONS (typical at +25°C with nominal power supplies unless otherwise noted)

Model	Units	CAV-1210
RESOLUTION (FS = Full Scale)	Bits (% FS)	12 (0.024)
LSB WEIGHT	mV	0.5
ACCURACY		
(Including Linearity) @ dc	% FS ± 1/2LSB	0.0125
Monotonicity		Guaranteed 0 to +70°C
Nonlinearity vs. Temperature	% of FS/°C	0.000125
Gain vs. Temperature	% of FS/°C	0.005
DYNAMIC CHARACTERISTICS		
AC Linearity[1] (dc to 1MHz)	dB below FS	70
(1MHz to 5MHz)		65
Conversion Time[2]	ns (max)	225 (±20)
Conversion Rate[3]	MHz	10
Aperture Uncertainty (Jitter)	ps	±25
Aperture Time (Delay)	ns	6
Signal to Noise Ratio (SNR)[4]	dB	62
Signal to Noise Ratio (SNR)[5]	dB	71
Noise Power Ratio (NPR)[6]	dB (min)	53 (52)
Transient Response[7]	ns, max	100
Overvoltage Recovery[8]	ns, max	200
Input Bandwidth		
Small Signal, 3dB[9]	MHz	35
Large Signal, 3dB[10]	MHz	30
Two-Tone Linearity (@ Input Frequencies)		
(60kHz; 62kHz)	dB below FS, min	70
(2.498MHz; 2.500MHz)	dB below FS, min	65
(4.996MHz; 4.998MHz)	dB below FS, min	60
ANALOG INPUT		
Voltage Range	V, FS	±1
(+1V input = all "1s"; −1V input = all "0s")	V, max	±2
Input Type		Bipolar
Impedance	Ohms	1000
Offset		
Initial (Set at Factory)	mV, max	±1
vs. Temperature	% of FS/°C	0.02
ENCODE COMMAND INPUT[11]		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Input)		"1" = −0.9
Impedance	Ohms, max	100 Line-to-Line
Width		
Min	ns	10
Max	70% of Encode Command Period	
Frequency	MHz	10
(Calibration Frequency is Customer-Specified; See Ordering Information.)		
DIGITAL OUTPUT		
Format	Bits	12 Parallel; NRZ
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)		"1" = −0.9
Drive	Ohms, min	75, Line-To-Line
Time Skew	ns, max	5
Coding		Offset Binary (OBN); 2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)		"1" = −0.9
Drive	Ohms, min	75, Line-to-Line
Rise and Fall Time	ns, max	5
Duration	ns (max)	25 (±5)
POWER REQUREMENTS[12]		
+15V ±5%	mA (max)	185 (205)
−15V ±5%	mA (max)	240 (265)
+5V ±5%	mA (max)	120 (135)
−5.2V ±5%	A (max)	2.1 (2.3)
Power Consumption	W (max)	18 (19.7)
TEMPERATURE RANGE		
Operating[13]	°C	0 to +70
Storage	°C	−55 to +85
Cooling Air Requirements	LFPM	500
(Linear Feet Per Minute)		
MEAN TIME BETWEEN FAILURES[14]		
(MTBF)	Hours	1.06×10^5

NOTES
1 AC Linearity expressed in terms of spurious in-band signals generated at 10MHz encode rate at analog input frequencies shown in ( ).
[2] Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits.
[3] To be specified by customer. See Ordering Information.
[4] Rms signal to rms noise ratio with 500kHz analog input.
[5] Peak-to-peak signal to rms noise ratio with 500kHz analog input.
[6] DC to 4.1MHz white noise bandwidth with slot frequency of 3.886MHz; and encode rate of 10MHz.
[7] For full-scale step input, 12-bit accuracy attained in specified time.
[8] Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage.
[9] With analog input 40dB below FS.
[10] With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 5MHz.
[11] Transition from digital "0" to digital "1" initiates encoding.
[12] ±15V must be equal and opposite within 200mV and track over temperature.
[13] Some spec degradation may occur outside a "window" of 50° centered at +25°C.
[14] 25°Ambient.

Specifications subject to change without notice.



CAV-1210 Block Diagram

THEORY OF OPERATION

Refer to the block diagram of the CAV-1210.

The analog input signal to be digitized is applied first to a track-and-hold (T/H) amplifier, which is normally operated in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1210 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The leading edge of the encode command causes the track-and-hold circuit to switch momentarily to the "hold" mode of operation, "freezing" the analog input long enough to begin the digitizing process. The "held" value of the analog signal is applied to a 6-bit A/D encoder, and (through a buffer amplifier) to an analog delay circuit whose delay is equal to the time required for the first digitizing/reconstruction step of the encoding process.

The analog output of the T/H is now digitized and resolved to 6-bit accuracy and applied through registers to a 6-bit D/A converter, which has 12-bit accuracy. Via a second set of registers, the same 6-bit digitized signal is applied to the digital correction logic circuits. The value stored in the second bank of registers will ultimately represent Bits 1-6 of the final digital output of the CAV-1210.

The digitized signal applied to the fast-settling D/A converter is reconverted to an inverted analog signal and is applied with the delayed analog input to a wideband, fast-settling operational amplifier. The op amp output represents the residue signal which remains after a 6-bit representation of the analog input has been subtracted from that input.

This residue, or error, signal is digitized by a second encoder to a resolution of 7 bits and applied to the digital correction logic circuits along with Bits 1-6.

The correction circuits use a combination of the 6-bit and 7-bit signals to compensate for possible nonlinearities and other errors to assure the final 12-bit digital output will be 12-bit accurate.

Oversimplified, the digital correction circuits use the information contained in the 7-bit signal to determine whether or not Bits 1-6 need to be modified.

Basically, the correction circuits use the information contained in the MSB of the 7-bit byte to determine what action needs to be taken with regard to the first six bits. Depending upon its value, the circuits will pass the 6-bit information as it is, or add a value of binary "1" to it. Bits 2-7 of the 7-bit information become Bits 7-12 of the digital output of the CAV-1210.

This unique use of 13 bits to achieve an accurate 12 bits of resolution compensates for a multitude of potential errors which otherwise could be eliminated only by incorporating expensive, high precision parts into the design. Digitally corrected subranging (DCS) used in the CAV-1210 does not prevent such anomalies as gain error, track/hold droop error, linearity error, or offset error. But it obviates the effects of these problems and makes high-speed, high resolution digitizing an economic reality.

ORDERING INFORMATION

The CAV-1210 A/D converter will meet all specifications shown in the Specifications table of the data sheet at encode (word) rates through 10MHz.

For standard CAV-1210 units intended to operate with specified performance over the full range through 10MHz, order model number CAV-1210-100.

If desired, the customer can order the unit calibrated at the factory for optimum performance at some specified rate within this range for those applications in which the unit will generally be operated at the same word rate.

Order by model number CAV-1210-XXX; in this model number, XXX is specified by the customer to indicate the desired optimized word rate. The decimal place is assumed (but not shown) between the second and third places. CAV-1210-050, for example, indicates final calibration and, consequently, optimum performance at 5.0MHz; but the unit will operate through 10MHz.

Optimum performance will be achieved within a ±12% band of frequencies around the selected word rate, but the user must keep in mind the upper performance specification of 10MHz. "Optimum" final calibration at 9.8MHz, for example, is not meant to imply optimum performance at word rates above 10MHz. The unit will operate beyond 10MHz, but accuracy, NPR, SNR, and/or other specifications may be outside the limits shown on Specifications page.

If later applications require word rates outside the limits of the original optimum frequency, the unit can be returned to the factory for calibration at a new optimum; there is a nominal charge for this service.

Mating sockets for the CAV-1210 are model number MSB-2 (thru hole) or MSB-3 (closed end). These are individual solder-type pin sockets for mounting in PC boards; one is required for each of the 40 pins of the converter.

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	21	$\overline{\text{BIT 9}}$
2	ENCODE COMMAND	22	BIT 8
3	$\overline{\text{ENCODE COMMAND}}$	23	$\overline{\text{BIT 8}}$
4	GROUND	24	BIT 7
5	−5.2V	25	$\overline{\text{BIT 7}}$
6	+15V	26	$\overline{\text{BIT 6}}$
7	−15V	27	BIT 6
8	GROUND	28	$\overline{\text{BIT 5}}$
9	ANALOG INPUT	29	BIT 5
10	GROUND	30	$\overline{\text{BIT 4}}$
11	+5V	31	BIT 4
12	GROUND	32	BIT 3
13	GROUND	33	$\overline{\text{BIT 3}}$
14	BIT 12 (LSB)	34	BIT 2
15	$\overline{\text{BIT 12 (LSB)}}$	35	$\overline{\text{BIT 2}}$
16	BIT 11	36	$\overline{\text{BIT 1 (MSB)}}$
17	$\overline{\text{BIT 11}}$	37	BIT 1 (MSB)
18	BIT 10	38	$\overline{\text{DATA READY}}$
19	$\overline{\text{BIT 10}}$	39	GROUND
20	BIT 9	40	DATA READY

CAV-1210 Pin Designations